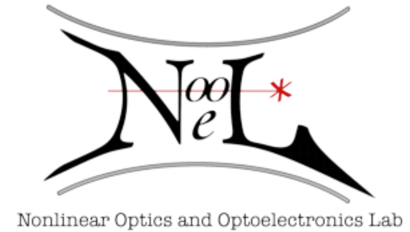
Investigations of Static And Dynamic Characteristics of Optically Controlled MOSFET



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Abstract

In recent years, scaling down the dimensions of electronic devices has driven dramatic improvements in the performance of electronic devices. With the increase in device speed and the introduction of exascale computing, the communication bottleneck has become one of the greatest challenge in both short and long distance communications. Traditional metal interconnects are efficient at short distances, but their excessive power dissipation and delay in global lines, makes them unsuitable for the ever-growing bandwidth demand. Currently, Optical interconnects (OIs) provides a solution to the communication bottleneck in long distance communications with their superiority in noise free, low loss, power efficiency and faster data transfer. However, in shorter distances, energy per bit is still higher compared to metal interconnects, due to the large power consumption by the receiver circuits. Since the receiver circuit after the photodetector, consumes most of the power, it is important to minimize the power consumption of the circuits, or if possible, to introduce receiver-less detection. Phototransistors, monolithically integrated to silicon electronics provides a possibility to replace power hungry receiver circuits in short distance (inter chip and intra-chip) communications. Although many phototransistors were reported with III-V compound semiconductors, it is still not easy and cost efficient to integrate them with the silicon photonics. In this context, Ge is becoming increasingly popular in silicon based photonic devices. Due to its strong absorption in the NIR region and its relative ease of integration with Si electronics, it is a promising candidate in fabricating CMOS compatible integrated photoreceivers.

In this work, an optically controlled field effect transistor (OCFET) with Ge as an NIR absorbing gate is designed simulated using ISE-TCAD. The static and dynamic charateristics of the OCFET are studied in terms of Ion/Ioff ratio, responsivity and bandwidth as functions of doping concentrations, channel length, optical power, Ge gate thickness, gate bias and Ge carrier lifetime. A maximum simulated responsivity of 100A/W and the fall time (t_{fall}) as

low as 100ps are obtained. The OCFET in different inverter configurations with parameters like load resistor, W/L ratio of the load MOSFET and CMOS configuration are investigated.

A proof of concept of OCFET is investigated by connecting a Ge-on-Si photodiode with the MOSFET gate terminal. The Ge-on-Si photodiode and the trench MOSFET designed and fabricated and OCFET concept is investigated under dark and illuminated conditions.

The final part of this thesis is dedicated to the design, fabrication and characterization of an optical JFET with 4μm and 8μm channel length and Ge thin film of 500nm as the gate. The current-voltage characteristics of the Optical JFET is investigated with open gate and applied gate bias. In the open gate configuration, the device exhibits a signal to noise ratio of 14dB at 0dBm (1mW) optical power compared to 3.7dB at -10dBm (100μW) optical power. The responsivity with floating gate was 5.3A/W, which decreases to 0.13A/W with applied gate bias of -1V.

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1

Introduction and Motivation

1.1 Introduction

The current age of information technology is in constant need for increased data transfer and data process capability. Nowadays, more advanced electronic systems are required with complex architectures that consist of ultra dense interconnected integrated circuits. Examples of such systems are computer servers and high-performance multiprocessor systems. The computational performance is mainly improved by advances in semiconductor industries. In the early stages of the CMOS technology, the performance of microprocessors was improved by both scaling the number of transistors per area [1] as well as the operating clock frequency [2]. The scaling approach provided a tremendous improvement in performance until the power consumption became an issue. It turned out that by scaling clock frequency, marginal improvement in processing performance was achieved with a significant increase power requirement [3]. As a result, designers employed a parallel computing approach through processors with multiple cores as shown in figure 1.1. In the near future processors are expected to have hundreds or even thousands of cores paving the way to exascale computing [4]. However, with the parallel computing, a number of drawbacks over single CPU based machines emerges. One major issue is the complexity of network interconnects to enable data transfer between the cores. In addition, with the increase in computing power, corresponding improvement in the inter-chip as well as on-chip communication bandwidth is needed.

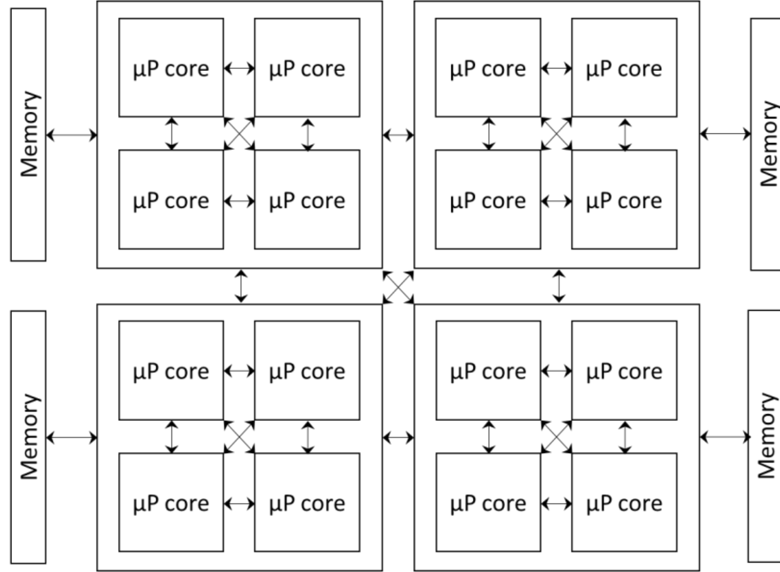


Figure 1.1 A high performance complex multicore processor

1.1.1 Electrical Interconnects

The most widespread interconnect technology used in on-chip and inter-chip interconnect networks is copper based electrical interconnects. The limitations of copper based interconnects (or any electrical) are becoming increasingly obvious as interconnect densities rise to keep pace with device scaling (on-chip) and increased bandwidth (inter-chip/board). The electrical interconnects are reaching their practical limits in terms of loss, dispersion, cross-talk and bandwidth. Because of the resistive loss in electrical lines, considering the case without repeating amplifiers, the bit rate on electrical lines limited by the cross sectional area (A) of the wiring and the length of the wires (L) according to [5];

$$B \leq B_0 \frac{A}{l^2} \tag{1.1}$$

with B_0 as a constant (10^{15} b/s for high performance strip lines and cables, and ~ 10^{16} b/s for small on-chip lines) for the resistive–capacitive lines. In case of on-chip interconnection, the number of connections scales geometrically with the number of cores, since each core needs a point-to-point connection to every other core. Therefore, the density of the network increases, forcing the individual connections to become smaller.

Unfortunately, down scaling of the wires used in electrical interconnects increases their resistance since the resistance of a current carrying wire is given by: $= \rho \frac{l}{A}$, where ρ is the resistivity of the wire material, l is the length and A and is the cross sectional area of the wire. At the same time, scaling down of the metal lines as well as the insulating layer between them implies reduction in capacitance. Therefore, the increase in the resistance and decrease in capacitance leaves the RC time constant unchanged [6]. However, as the wire cross sectional dimensions continue to scale downward and circuit speed continues to increase, several factors exacerbate the interconnect latency problem.

Latency is a measure of the time-delay between transmitting and receiving a signal. Electrical signals are limited by the drift velocity of the electrons inside a wire which in turn is dependent on the length of the wire (L), mobility of electrons (μ) in the material and the voltage drop (V) between its ends. In order to increase the speed that signals travel through an electrical wire, the voltage and/or the electron mobility must be increased. The fundamental limitation of speed occurs, since higher voltage can damage sensitive electronics and mobility is a function of material properties. In contrast, optical interconnects transfer the signals at the speed of light. This is the upper speed limit for the signals to be propagated and therefore optical interconnections intrinsically have the smallest possible latency.

When wire cross-sectional dimensions become smaller than the bulk copper electron's mean free path length, the separators surrounding a copper interconnect to prevent copper atoms' migration into the silicon become thicker than the copper interconnect itself. In addition, power dissipation causes increase in the wire temperatures. Finally, the high-speed operation creates a greater current density near the wires' periphery than in their central region. This so-called "skin effect" leads to greater electromigration effects, when the movement of conductor atoms under the influence of electron bombardments, resulting ultimately in the breaking of conductor lines [7].

The potential of optical interconnections like, a) the density of information that can be sent over relatively short/long distances, b) reducing the skin effect c) speed of transmission depending on the medium and d) the superior immunity to mutual and electromagnetic interference are of considerable interest in choosing optical interconnects over their electrical counterparts.

1.1.2. Optical Interconnects

Optical interconnects for microelectronic chips have been studied for a long time [5, 6] several investigation on the comparisons with the electrical interconnects have been made [11-20]. The capacity limitations, losses, cross talk and parasitics along with other disadvantages of electrical wires paved way to the optical interconnects. Already, all long distance communications now switched to optics. For medium distance communication, e.g. LAN, MAN, WAN, optical interconnects is gaining popularity specifically because only optics can support the high data rates required by these applications. At shorter distances (a few meters), primarily in data links, optics is rapidly gaining entry. Research is underway at even shorter distances (board and chip level) to use optics for communication purposes. Figure 1.2 shows the already used and future possibilities of optical interconnections.

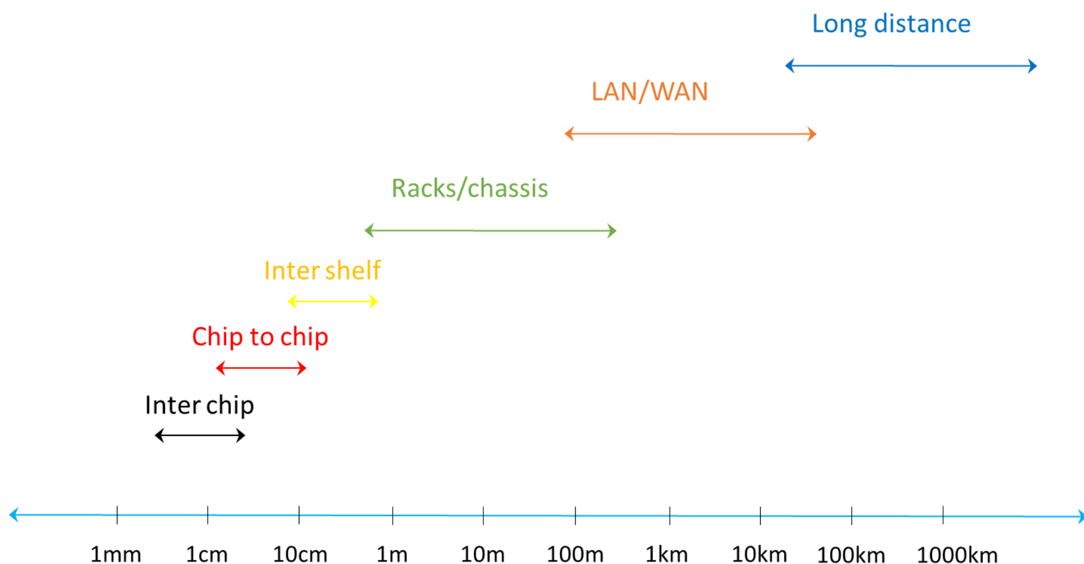


Figure 1.2. A categorization of optical links based on the distance.

Given the huge optical interconnect bandwidth needed (figure 1.3), it is unlikely that a single stream of data will meet the growth requirement. Instead, multiplexing techniques like, Time Division Multiplexing (TDM), Spacing Division Multiplexing (SDM) or Wavelength Division Multiplexing (WDM) can be used to tap in the vast available bandwidth of optical fiber [8], [22]. Optical interconnects with these techniques allows, not only higher bandwidth density for global interconnects, but also in board level [9] or chip level interconnects.

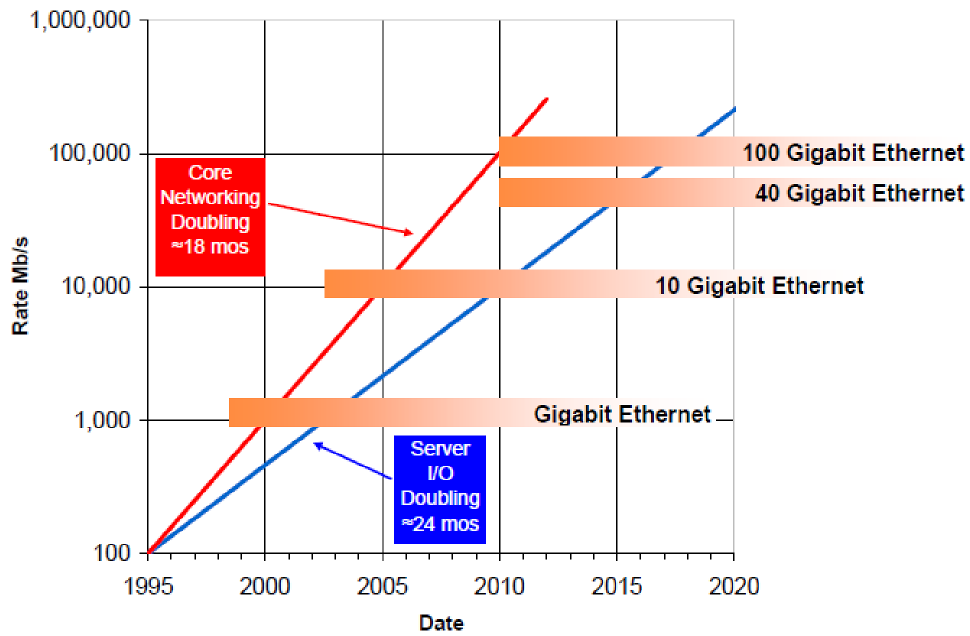


Figure 1.3. Bandwidth trend for server and networking I/O [10].

In short distance interconnections, the combination with voltage variable gratings, provides selective routing possibilities that can be used for radically different signal processing functions than those currently available. This provides the promise of dramatically increased bandwidth, even while reducing the number of connections necessary to carry all of the information [9].

Using optics provides a very high frequency carrier, at a very short wavelength and a large photon energy. The very high optical carrier frequency eliminates frequency dependent loss in the modulation band, and makes short pulse communication feasible. The short wavelength allows, low loss in waveguides, impedance matching with very low overhead, and wavelength division multiplexing (WDM) [14].

Other advantages of optics include, the density of interconnects. For off-chip or board-to-board interconnects, optics can offer very large densities. Optical devices can be made very small and 1000's of input/outputs (I/O) can be achieved on a chip. Optical interconnects can utilize the third dimension by being able to cross the beams. In free space, a few optical elements can easily handle a large number of beams, providing very high interconnect densities.

Most electrical lines are designed for 50Ω impedance, which requires a 50Ω termination to avoid reflections. A lot of power is absorbed in this termination. Optics exploits a potential advantage of impedance transformation that matches the high impedance of small devices to the low impedance associated with electromagnetic propagation [17]. A quarter-wavelength wide index matching material can match the impedance of two dissimilar materials to remove reflections. This is equivalent to the termination in electrical lines; in optics, though, there is virtually no power dissipation in this index matching material. In optics, a beam splitter can be used to tap the optical signal for monitoring, with small or negligible reflections. A similar tap in electrical lines needs to be very well designed to minimize the impedance discontinuities.

With optics, a complete electrical isolation is possible [21], since the voltages on either sides need not be related to each other. This provides noise immunity from one side to the other. With scaling in electronics, the supply currents are increasing and so are resistive drops in dc supply and ground bounce effects. Hence this voltage isolation property of optics may become progressively more important for future generations.

1.1.3. Components of an Optical Interconnect System

In general, an optical interconnect system has three main components: a transmitter, the transmission medium, and a receiver. Binary data from the digital circuits, in the form of voltage levels, is fed to a transmitter driver, which converts these levels into the voltage or current signal required to drive the optical modulator device. The optical modulator converts these electrical signals into the modulation of light beams, which then travel through a propagation medium (optical fiber or waveguide) to destination. At the receiver side, the photodetector converts the optical signal into current, which is then converted into logic level by the receiver system. Figure 1.4 shows the general components of an optical interconnect system.

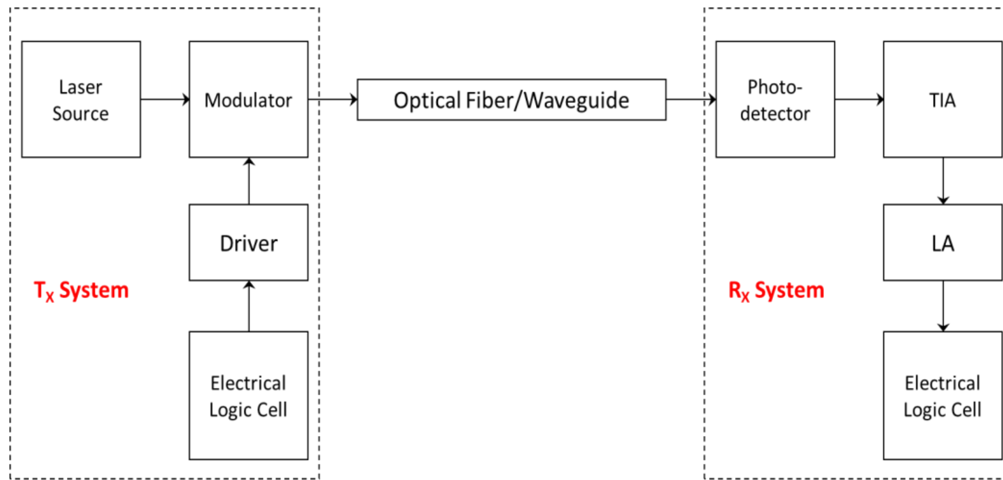


Figure 1.4. The components of an optical interconnect system.

Further, in this chapter, I briefly introduce the different options for optical source, modulators and transmission medium, with the main emphasis on the optical receivers. Since the receiver circuitry directly interfaces with the photodetectors, understanding the operation and characteristics of these devices is essential for an optimum design. However, the main concern of this thesis is on photodetectors, particularly on an optically controlled FET.

Laser Sources: Optical interconnect systems use either off-chip or on-chip laser sources. One of the main candidate for an optical source is the Vertical Cavity Surface Emitting Lasers (VCSELs) as they have improved significantly in the last few years. Oxide confined VCSELs can achieve very low threshold currents [23]. Sub-mA threshold currents are now easily achieved in VCSELs and optical interconnects with arrays of VCSELs have been already demonstrated [24-25]. But there are many issues like, uniformity of threshold current, wavelength stability and thermal issues that still need to be addressed for using large VCSEL arrays in optical interconnects [26]. Despite the advancements in on-chip sources, Off-chip laser sources are generally preferred due to several problems faced by directly modulating Lasers. Due to non-availability of an efficient and silicon compatible laser and since it is very hard to fabricate large number of lasers on a single chip at reduced cost. Moreover, the complexity of chip design increases significantly since optical source will be a part of the chip's power and heat budget. Such issues can be mitigated with off-chip light source that individually supply addressable effective source points, located at positions dictated by the interconnect topology, and using modulators and a coupling structure [27].

Optical Modulators: Optical modulation is one of the main required functionalities for any optical interconnect solution. The primary purpose of an optical modulator in a photonic network is to modulate the light source. This modulation can be done either directly or externally, but external modulation offers several advantages over direct modulation: the optical source can be relatively inexpensive and its operation does not need to be compromised by direct modulation, modulation speeds can be higher, and optical isolation and wavelength stabilization need to be performed only once for the entire system. Furthermore, a single light source can feed multiple channels via individual modulators, thus reducing the total power budget of the system [28]. There are various optical modulation techniques through which refractive index or absorption properties of optical medium are varied in accordance with the electrical signal. Current optical modulation techniques are based on Thermo Optic effect, Electro-optic effect, [29] Electro absorption effect and plasma dispersion effect. Another modulation mechanism is the electroabsorption effect involves the change in the absorption coefficient of the material with change in applied electric field. These techniques are more effective in III-IV semiconductors but the most effective method for changing the refractive index of the Silicon is carrier plasma dispersion technique [30]. Several researches are being carried out on optimizing device structures and developing integration techniques for the high speed and low power modulators compatible with current CMOS technologies [28] [31-35].

Optical Channels: Optical channels are similar to electrical links for data transmission. The two optical channels relevant for long/short distance communications are optical fibers and optical waveguides. These optical channels offer potential performance advantages over electrical channels in terms of loss, cross talk, and both physical interconnect and information density.

Optical fiber based systems provide alignment and routing edibility for chip-to-chip interconnect applications. As shown in Figure 1.3, an optical fiber confines light between a higher index core and a lower index fiber cladding via total internal reflection. Fibers are classified based on their ability to support single or multiple modes. Single-mode fibers with smaller core diameters (typically 8-10μm) only allow one propagating wave, and thus require careful alignment in order to avoid coupling loss. These fibers are optimized for long distance applications such as links between Internet routers spaced up to and exceeding 100km. In addition, Multi-mode fibers with large core diameters (typically 50μm) allow

several propagating modes, and therefore provide good coupling characteristics. These fibers are used in short and medium distance applications.

Another means optical communication is employing optical waveguide, mainly in short distance data transfer (like inter chip or intra chip). Similar to optical fibers, waveguides can either support multiple or single optical modes. Usually, to facilitate coupling and reducing assembly costs, multi-mode waveguides are favorable. The waveguide core is surrounded by a cladding layer with smaller refractive index to enable total internal reflection. Due to their large core area, they provide negligible coupling loss. In addition, the modal dispersion is fairly small as they are intended for short range board-level interconnection.

Receivers: The receiver can be divided into two sections, a photodetector that converts light into electrical signal followed by a receiver circuit that amplifies the analog electrical signal and matches to a digital voltage level. A simplified equivalent circuit model is shown in Figure 1.5. Optical receivers generally determine the overall optical link performance, as their sensitivity sets the maximum data rate and amount of tolerable loss in the channel.

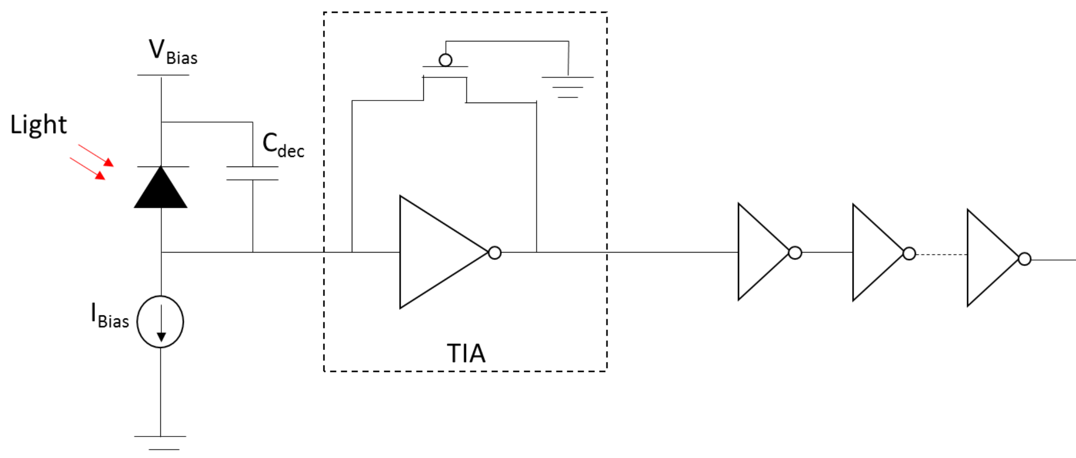


Figure 1.5. Circuit model of an optical receiver

For a better performance, the capacitance of the photodetector and the receiver circuit should be as low as possible. A smaller capacitance device requires fewer gain stages and offers noise immunity. To reduce the capacitance, monolithic detectors can be made in silicon. But silicon has a large absorption depth even at wavelengths near 850 nm (first window of optical communications), much deeper than junction depths in silicon MOS devices. Most photons are absorbed deep inside the substrate causing generated carriers

contributing to substrate noise. In order to obtain optical receivers operating at longer wavelengths (typically between 1.3 and 1.6 micrometer), considering compatibility with CMOS technology, a practical solution is to use SiGe or Ge photodetector. Eventhough Ge is an indirect bandgap material (Eg ~ 0.66 eV), it is a strong absorber at the near infrared due to its direct band transition at 0.8 eV, as shown in Fig. 1.6. In addition, the carrier mobility in Ge is higher than in Si, promising faster operation. The smaller bandgap results in somewhat higher thermally generated noise in Ge-based devices. The most attractive feature of Ge is its compatibility with Si processing and low temperature processing capability.

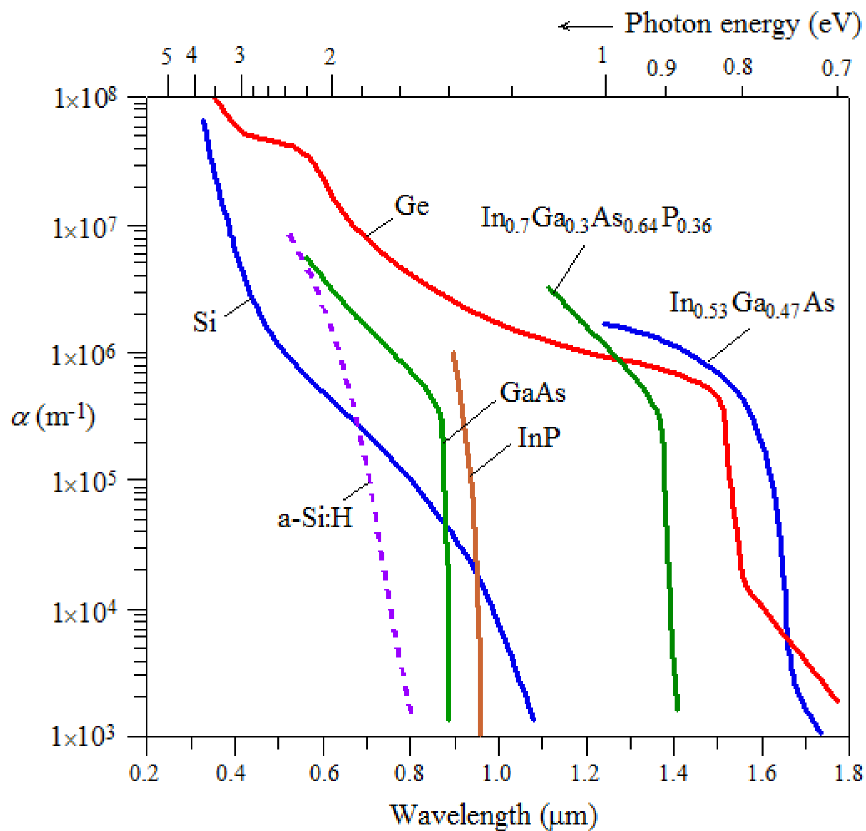


Figure 1.6. Absorption coefficient of various semiconductors vs wavelength

The works on this thesis are focused on using Ge absorbing layer on a conventional MOSFET at 1550nm to achieve receiverless detection. However, a brief introduction is given on receiving amplifiers and different types of photodetectors (photodiodes and phototransistors).

1.2. Receiver End

1.2.1. Photodetectors

In general, the semiconductor photodiode detector is a p-n junction structure that is also based on the internal photoeffect. Photons absorbed in the depletion layer generate electrons and holes which are separated by the local electric field. The two carriers drift in opposite directions. Such a transport process induces an electric current in the external circuit [36]. Some photodetectors (Avalanche photodetectors) incorporate internal gain mechanisms so that the photoelectron current can be physically amplified within the detector and thus make the signal more easily detectable. The main figures of merit of a photodetector are, responsivity (R), quantum efficiency (η) and response time.

The quantum efficiency is an important parameter representing the capability of the photodetector to convert a photon in an electron-hole pair; if η is 1, every single photon generates a carrier pair. If we consider a photoconductor of thickness d, neglecting reflections at the interface, the quantum efficiency can be expressed in function of the absorption coefficient (α) as:

$$\eta = \eta_c(1 - e^{-\alpha d}) \tag{1.2}$$

where η_c is the collection efficiency, i.e. the percentage of carriers generated and contributing to the photocurrent, and generally can be considered close to 1. The quantum efficiency is a function of wavelength, principally because the absorption coefficient (α) depends on wavelength (as shown in fig. 1.6).

The responsivity of a photodetector indicates how efficiently light is converted in to photocurrent and, is given by, the ratio between the photocurrent I_{ph} flowing in the photodetector divided by the incident optical power P_{in}:

$$R = \frac{I_{ph}}{P_{in}} \tag{1.3}$$

The responsivity decreases with large optical power. This condition, which is called detector saturation, limits the detector's linear dynamic range, which is the range over which it responds linearly with the incident optical power.

1.2.1.1. Junction Photodiodes

A simple form of a junction photodiode is a p-n junction detector, whose reverse current increases when photon are absorbed. Consider a reverse biased pn-junction as shown in fig. 1.7. Photons are absorbed all over the diode with absorption coefficient α. Whenever a photon is absorbed, an electron-hole pair is generated, but only where an electric field is present the charge carriers can be transported in a particular direction. Since a pn junction can support an electric field only in the space charge region, photocarriers are desirably generated in this region. The photocurrent is associated with two fundamental mechanisms: drift and diffusion. The main contribution is the drift current associated to the carriers generated in the space-charge region. Here the generated electrons and holes are swept and transported by the electric field to the neutral regions where they recombine with majority carriers from the electrodes. The reverse bias to the diode helps to increase both the absorption efficiency and the collection efficiency. Therefore, the photocurrent in the drift regime increases with reverse voltage. Photons absorbed in the neutral regions also generate photocarriers that partially contribute to the photocurrent. In fact, the absence of electric field allows the generated carriers to recombine without affecting the charge neutrality. Only the photocarriers generated in the proximity of the space charge region (about one diffusion length) can contribute to the photocurrent. This current represents the diffusion contribution to the photocurrent and, as it is not affected by the electric field, it is constant with the reverse bias.

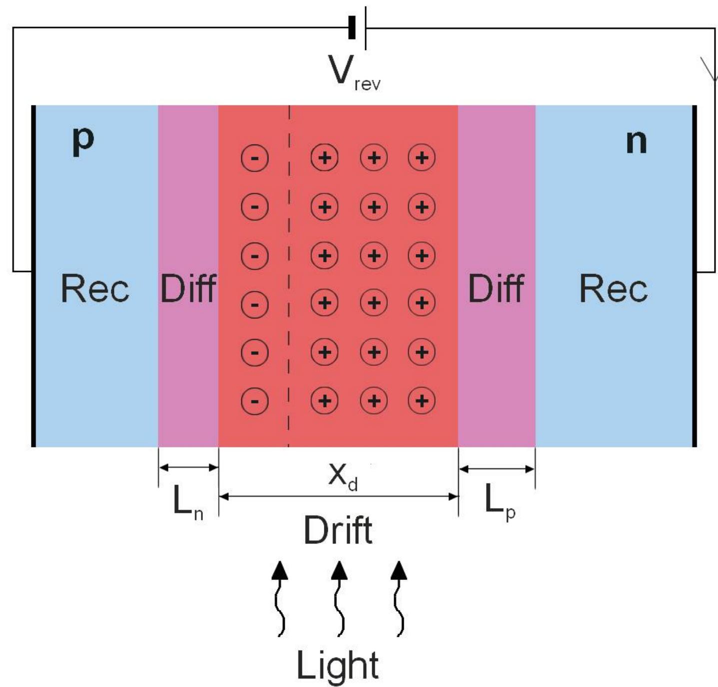


Figure 1.7. A reverse biased pn-junction diode illuminated by photons. The drift and diffusion regions are indicated.

Although drift and diffusion currents contribute to the photocurrent, it is important to minimize the diffusion current for a high performance photodetector. The transit time of the carriers drifting across the depletion region play a role in the response time of the detectors. In photodiodes there is an additional contribution to the response time arising from diffusion. Carriers generated outside the depletion layer, but sufficiently close to it, take time to diffuse into it. This is a relatively slow process in comparison with drift mechanism. The typical times allowed for this process are the carrier lifetimes (τ_p for electrons in the p region and τ_n for holes in the n region). This effect of diffusion time can be decreased by using a p-i-n diode.

As a detector, a p-i-n photodiode has a number of advantages over a p-n photodiode. A p-i-n diode is a p-n junction with an intrinsic (undoped or lightly doped) layer sandwiched between the p and n layers. Figure 1.8 shows the schematic of a p-i-n photodiode. This structure serves to extend the width of the region supporting an electric field, in effect widening the depletion layer. This electric field drives the electrons and holes generated by the incident photons in the intrinsic region to the n and p terminals, respectively. The result

is a current proportional to the number of photons absorbed per second, which is called photocurrent. In the p-i-n diode, a reverse-bias across the diode ensures a strong field in the intrinsic region and a very small current in the absence of light, which is referred to as dark current.

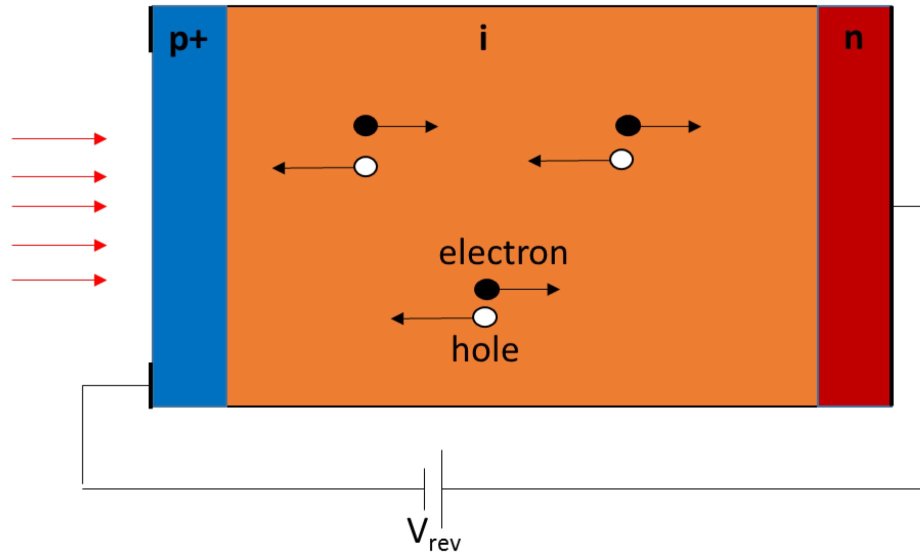


Figure 1.8. Schematic illustration of a p-i-n photodiode

Photodiodes with the p-i-n structure offer the following advantages,

- Increasing the width of the depletion layer (where the generated carriers can be transported by drift) increases the volume available for capturing light.
- Increasing the width of the depletion layer reduces the junction capacitance and thereby the RC time constant. On the other hand, the transit time increases with depletion layer width.
- Reducing the ratio between the diffusion length and the drift length of the device results in a greater proportion of the generated current being carried by the drift mechanism.

Furthermore, the depletion-layer width W in a p-i-n diode does not vary significantly with bias voltage but is essentially fixed by the thickness of the intrinsic region. The capacitance has a simpler expression, mainly dependent on the i -layer width w,

$$C_j = \frac{\varepsilon_0 \varepsilon_r}{w} \quad (1.4)$$

The series resistance Rs depends on the resistance of the neutral regions and the contact resistance of the metal/semiconductor contacts. Since at increasing reverse biases the depletion region widens, the contribution of the neutral regions becomes less important at higher reverse voltages, approaching zero when the punch through condition is reached. Typical values of Rs are of the order of a few Ohms. The p-i-n photodiodes exhibit better performance with respect to the p-n junction diodes. In fact, in p-n photodetectors it is very important to properly tune the doping levels to achieve a better trade-off between neutral region resistivity and depletion region width. In p-i-n photodiodes, this is less crucial because it is possible to act on p and n doping without affecting the depletion region, which is restricted to the i-layer width.

The two serious limitations on the speed of a p-i-n photodiode are, the transit time through the depletion region and the charging/discharging time of the diode capacitance [37]. The other limitations like diffusion time and charge trapping can be minimized by detector design. The transit time is directly related to the depletion width (L) and it is governed by the speed of slower carriers (holes) generated at the opposite end of the depletion region. So the transit time can be approximated as, $\tau_{Tr} = L/v_h$, where v_h is the hole velocity. This suggests that a high speed can be achieved with thinner intrinsic layer, but at the expense of increased capacitance. Further the efficiency of a p-i-n photodetector with a thin absorbing layer is proportional to the thickness as $\eta \propto \alpha L$, where α is the absorption coefficient. So the bandwidth efficiency product of a p-i-n detector limited by its intrinsic material properties.

1.2.1.2. Heterojunction Photodiodes

Heterojunction photodetectors are photodiodes with different materials in the junction, i.e. with unequal bandgap energies (E_g). The heterojunctions allows more design flexibility and better performance. For example, consider a normal incidence p-n detector in which the top layer has $E_{g1} > E_{g2}$. Photons with energy $E_{g1} > h\nu > E_{g2}$ can pass through the top layer without absorption while are absorbed in the bottom material minimising the diffusion photocurrent from the top neutral region and improving the temporal response. Another important advantage is the possibility to realize photodetectors at certain wavelengths with the substrate being transparent in that spectrum. In realizing a heterojunction detectors, the main method is to grow thin films on a bulk substrate. Even though it could be possible to

deposit any material on any semiconductor, a successful heteroepitaxy (in terms of crystal quality) is attained if two materials have the similar crystal structure and lattice parameters. Fig. 1.9 shows the lattice constants of the most relevant semiconductors (used in different combinations) used for photodetection versus bandgap energy and cutoff wavelength.

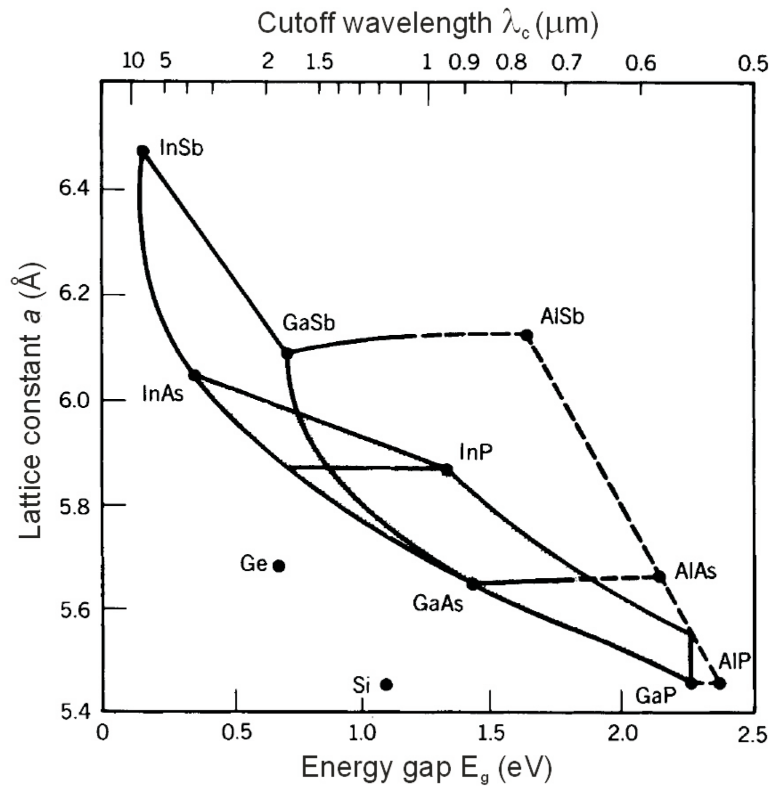


Figure 1.9. Lattice constants of some frequently used semiconductors versus energy bandgap and cutoff wavelength. Dots refer to elementary materials and curves to compounds, where solid and dashed lines represent direct and indirect bandgap compounds respectively.

Considering the fact, that the electric and optical properties of the heterostructure directly depends on the crystalline quality, it is necessary to choose the less mismatched material-substrate combination to obtain the least defected heteroepitaxial layer.

As the optical communication window is in the range of 1.3 to 1.6 μm (C-band), photodetectors in this particular range of wavelengths are discussed. It is evident from figure 1.6, ternary and quaternary compounds based on III-V semiconductors such as Gallium Arsenide (GaAs), Indium Arsenide (InAs) and Indium Phosphide (InP) are better suitable materials for this spectral range. Alloy such as InGaAsP [39] allow extreme flexibility with variable cutoff wavelengths in the range 1 μm to 1.8 μm depending on composition. For

third-window applications, the best solution is represented by lattice matched InGaAs on InP heterojunctions with cutoff wavelengths at 1.65 μm [40]. III-V photodetectors are widely used in near-infra red detection thanks to their superior performance in terms of sensitivity and speed. Unfortunately, this superiority comes with a drawback: the lattice mismatch prevents the deposition of III-V thin films on Si substrates; therefore, it is necessary to use the more expensive InP substrates. This incompatibility prevents the monolithic integration of III-V devices with standard Si electronics. Thus, signal processing requires either the monolithic integration of detectors on expensive III-V electronics, or the hybrid integration of III-V devices on Si electronics by means of sophisticated techniques like for example, wafer bonding. There are several researches being carried out on hybrid opto-electronic integrated circuits (OEIC). However, monolithic integration on Si would sensibly reduce costs of NIR optoelectronics taking advantage of the well-established Si CMOS technology [41].

As Si is transparent to wavelengths longer than 1.1 μm (E_g = 1.11 eV), several solutions have been investigated to integrate NIR absorbing semiconductors with Si in order to realize integrated Si-based NIR detectors. Germanium has been recognized as a main candidate for Si based NIR photodetectors [42, 43]. Thanks to its lower bandgap (0.66 eV) corresponding to an absorption cutoff wavelength ($\lambda_c = \frac{hc}{E_g}$) up to 1.8 μm (Fig. 1.8). Germanium, a group IV material the same as Si, avoids the cross contamination issue. Its direct bandgap of 0.8 eV is only 140meV above the dominant indirect bandgap. As a result, Ge offers much higher optical absorption in 1.3μm-1.55 μm wavelength range, thus making Ge-based photodetectors promising candidates for Si photonics integration. However, the 4% lattice mismatch between Ge and Si places challenging obstacle towards monolithic integration of high-quality low dislocation density devices through Ge on Si heteroepitaxy. Nevertheless, single crystalline device grade Ge films have been demonstrated by many groups with high performance Ge photodetectors. At the starting stage of Ge-on-Si photodetector development for Si photonics applications, normal incidence Ge photodetectors were first fabricated and comprehensively studied. In 2000 Colace et.al. [44] demonstrated a Ge-on-Si heterojunction photodetector fabricated by UHV-CVD with responsivities of 550mA/W at 1.32 μm and 250 mA/W at 1.55 μm and time responses shorter than 850 ps. Later, Famà et.al, demonstrated a p-i-n photodetector [45], with 0.89 A/W and

0.75 A/W at 1.32 μm and 1.55 μm respectively, and a response time of <200ps. Dosunmu et.al, fabricated a resonant cavity enhanced Ge- Schottky photodetectors with bandwidth up to 12 GHz at 1540nm [46]. Jutzi et al. [47] fabricated a normal incidence Ge-on-Si photodetectors by molecular beam epitaxy (MBE) with responsivity as high as 0.73 A/W at 1.55 μm and a remarkable bandwidth of 39 GHz. Among the reported NIR photodetectors, Klinger et al. [48] reported the highest bandwidth of 49 GHz for Ge-based photodetectors. The Ge p-i-n photodiode was fabricated in Ge grown by MBE two-step Ge growth. The reported responsivity at 1.55 μm is ~0.05 A/W limited by small device footprint and relatively large density of defects in the Ge layer.

In order to reach a higher responsivity, a thick Ge absorption layer is needed. The highest reported value at 1.55 μm wavelength for normal incidence NIR photodetector is 0.75 A/W [45]. As the Ge growth technique becomes mature and the characteristics of Ge-Si devices have been studied in detail, research has been gradually redirected to the integration of Ge photodetectors on Si waveguides to decouple the trade-off between bandwidth and efficiency. To date, a number waveguided Ge photodetectors have been demonstrated [49-56]. Both PIN and MSM structures are reported in these waveguide photodetectors with comparable performance and high speeds of around 40 GBit/s. A waveguided photodetector with the responsivity approaching the theoretical limits were demostrated by Yin et al. [51]. They demonstrated Ge-on-Si n-i-p waveguide photodetectors with responsivity as high as 1.16 A/W at 1.55 μm, operating at 30 GHz.

For a photodetector to be used in Si photonics integrated circuits, a next level pre-amplifier is necessary to further transform the current signal into a voltage signal for further processing. Avalanche photodetectors offers much lower signal-to-noise ratio compared to PIN or MSM structures. Ge-on-Si avalanche photodetectors were also investigated with remarkable results [52,57,58]. A Ge based APD was first reported by, Kang et al [57]. The reported Ge-on-Si avalanche photodetectors operating at 1.3 μm, with an excellent gain-bandwidth product of 340 GHz and a sensitivity as good as -28 dBm at 10 Gb/s.

1.2.1.3. Phototransistors

Phototransistors are another form of photodetectors, which have internal gain added with responsivity, besides APDs. Combining a detector and a transistor into a single device is an excellent approach towards realizing the receiver-less detection (Section 1.3) which is desired in chip-level optical interconnects. Such a device should be easily integrated into the existing process technologies and can be readily scaled down to obtain extremely low device capacitance. The additional gain mechanism in phototransistors, also helps to relieve input light requirement which would otherwise be quite stringent with only primary photoresponsivity. The first demonstration of a phototransistor was carried out by Bell Labs [59-61]. Figure 1.10 shows a common phototransistor, it differs from a standard bipolar transistor by omitting the base contact, and have a much larger base and collector areas compared to the emitter.

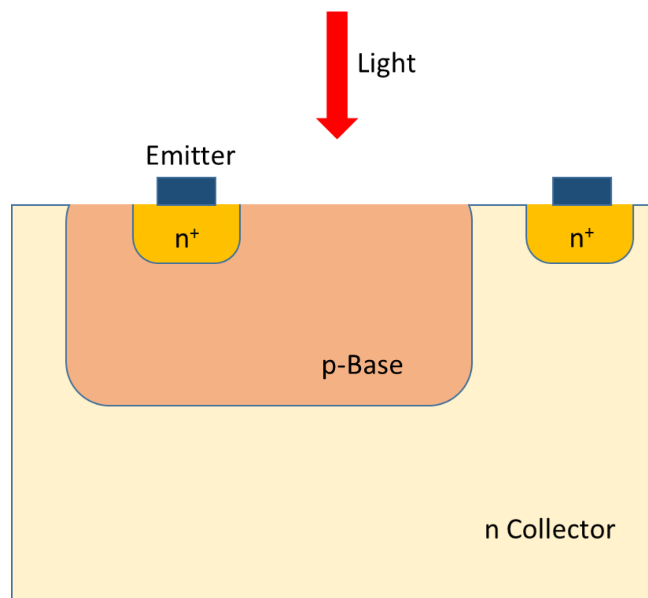


Figure 1.10. Schematic of a common phototransistor

The performance of the phototransistor later improved (high current amplification factor) using heterojunctions, with emitter being wide bandgap than the base [62]. The homojunction transistors requires a lightly doped base and a heavily doped emitter for efficient injection from the emitter to the base, whereas the barrier at emitter-base heterojunction of the HPTs (Heterojunction Phototransistors) alone can prevent reverse

injection from the base. Hence, a heavily doped base can be used to reduce the base resistance and a lightly-doped emitter can be utilized to decrease the base emitter capacitance. Further better characteristics were achieved by taking advantage of the avalanche multiplication in the base-collector junction of the phototransistor to enhance current amplification [63, 64].

Despite the improvements in performance, the gain-bandwidth products achieved from the phototransistors were limited and not exceeding that of APDs. In addition, heterojunction phototransistors are considered too costly to be commercially feasible. Hence, the research on phototransistors was then taken over by other photodetector technologies like APDs. However, since the current research trends in optical interconnects requires integrated photodetectors, there is now a revival of research interests on phototransistors. Furthermore, the improved technologies of growing germanium on silicon wafers permits the heterojunction phototransistors to be built on Ge/Si stacks and thus solving the problems with compound semiconductor (III-V) technologies which lack the vital cost-effective integration capacity with advanced silicon VLSI technology.

Historically, the bipolar structures attracted most of the interest in the research on phototransistors. But from late 80's, a great deal of interest was shown towards the photosensitivity of field-effect transistors (FET). The photosensitive FET covers a class of FETs including JFETs, MESFETs, and MOSFETs that combine high-impedance amplifiers with built-in photodetectors [65-74]. The advantages of FET photo-transistors that combine high-impedance amplifiers with built-in photodetectors are believed to have very fast response and high optical gain. A first demonstration FET photodetector was done by Baack et al with GaAs MESFET. They abserved a rise time of 46ns compared to 74ns for a APD [65].

The FET-photodetectors based on compound semiconductor technologies lacks the vital cost-effective integration capacity with advanced Si VLSI technology. Germanium being a group IV semiconductor provides advantages in cost effective integration with silicon and avoiding cross contamination issues. In this work, I study an optically controlled field effect transistor replacing the MOSFET gate with Ge as an absorbing layer.

1.2.2. Receiver Front End

The task of an optical receiver front-end is to convert the current from the photodiode into a voltage and amplify the signals in order to be accepted by CMOS logic stages (fig 1.4). A transimpedance amplifier (TIA) is mainly used instead of a simple resistor. The strong trade-off between the bandwidth and SNR of a front-end with a simple resistor makes it impractical for many applications. The effective input resistance of the front-end can be reduced significantly by adding an active component to the design, resulting in a transimpedance architecture. A transimpedance amplifier (TIA) is an analog front-end with reduced input impedance and a relatively high current-to-voltage gain.

The transimpedance amplifier stage, consumes most of the power, and it is typically followed by several buffer/amplifier stages. In order to minimize the power consumption at the transimpedance amplifier stage, we need to minimize the output capacitance of the photodetector. However, if the output capacitance of the photodetector is still too high, the power consumption of the receiver circuit can easily exceed the power requirement of optical interconnects. Integrated front-ends have been demonstrated to reduce the power consumption and area of the front-end by eliminating the need for TIAs [124]. The main advantage of this technique is that it mainly employs digital circuitry that allows for achieving considerable power saving by scaling to advance technology nodes. Another advantage associated with this technique is that, it reduces receiver sensitivity to common-mode interferences

1.3. Receiver-Less Detection

A receiver-less optical receiver circuit (Fig.1.11-a), which includes a pair of photodetectors, has been proposed to eliminate the power inefficient transimpedance amplifier stage. The top diode, connected to the supply, injects a rising edge. The bottom diode, connected to ground, resets the voltage back to its initial ground state. Both diodes limit the swing of the node in the middle. By alternating pulses on both detectors, a precise square wave can be injected to the next stage. If the input optical power is high enough to charge and discharge the input node close to V_{dd} and GND in less than a bit-time, a simple inverter can recover a full swing voltage and resolve the received data. The required input modulation optical power for a full voltage swing is proportional to the photodiode responsivity. The minimum optical power is proportional to the total capacitance, requiring

very small photodiode capacitances as well as the small voltage buffer that follows it. However, this configuration requires two optical signals (direct and inverted), precisely separated in time, arrive at the detectors.

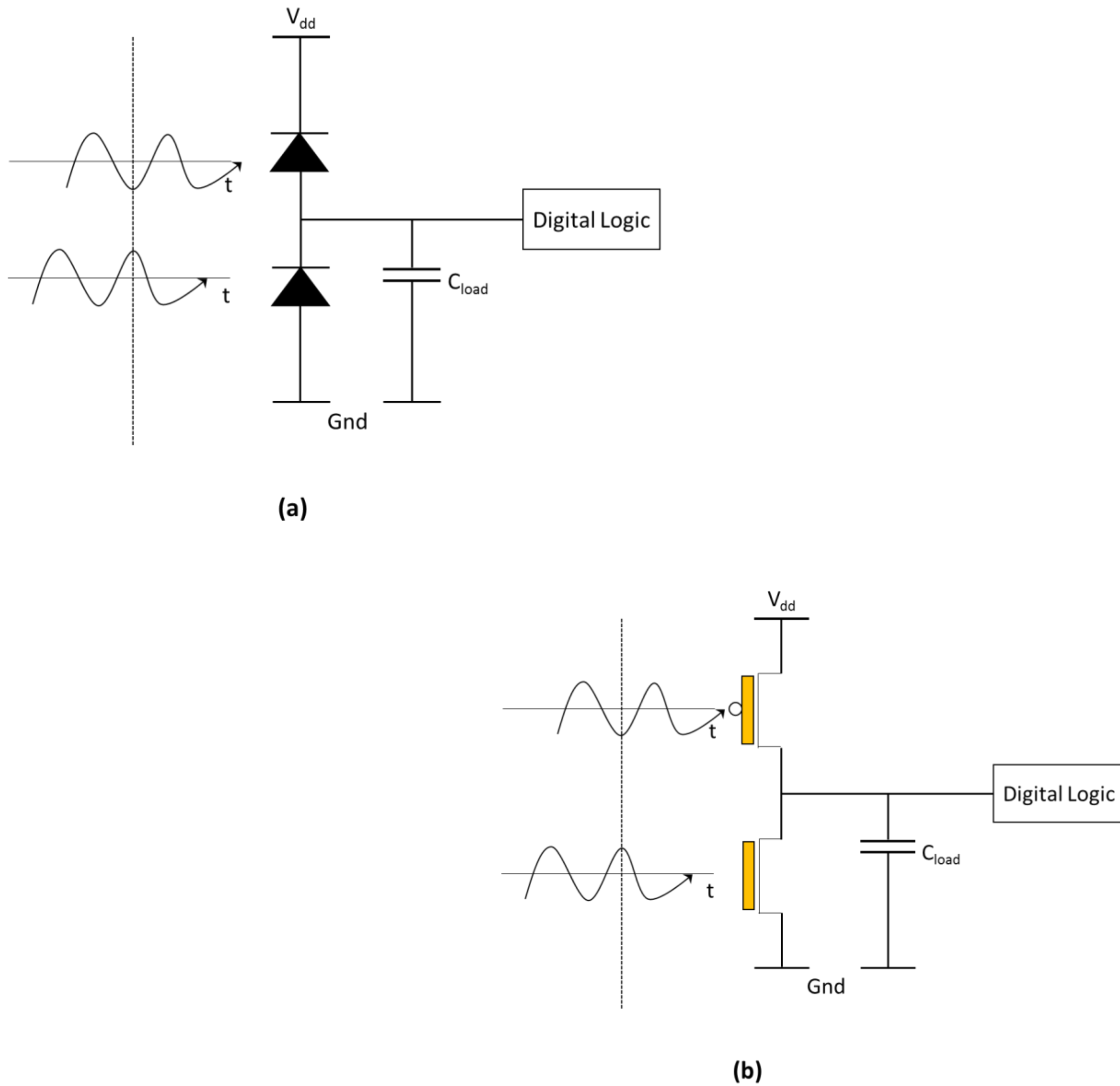


Fig 1.11. (a) A receiver-less circuit stage with two photodetectors connected in totem pole configuration [75] and (b) A receiver-less circuit stage with a pair of complementary phototransistors connected in totem pole configuration.

A pair of complementary phototransistors can be connected in totem-pole configurations (fig. 1.11-b), replacing the photodiodes. Phototransistors are a unique optical detector in which light detection (photodiodes) and electrical signal amplification

(transistors) are combined in a single device and thus have minor issues of noise increments, high voltages and high cost.

An important example is discussed in this thesis, that is the simulation and investigation of Ge gate MOSFETs on Silicon substrates, studying the above configuration, with complementary OCFETs (Optically Controlled FETs).

1.4. Organization

The following Chapter 2 provides a background information on the simulation software (ISE-TCAD) used for the investigation of the characteristics of optically controlled FET. This chapter also explains the physical models used in this study along with the changes in Ge material parameters. The simulation of the OCFET structure and its static and dynamic characteristics are described in chapter 3. In this chapter, inverter configurations like resistive load and active load inverters using OCFET as driver transistor and as a load transistor as well in the CMOS configuration are investigated. A set of parameters are identified for both high responsivity (Ion/Ioff ratio) and high speed operations of the OCFET. Chapter 3 also provides the design and simulation of an Optical-JFET and its characteristics.

Chapter 4, describes the fabrication and characterization of a Ge-on-Si heterojunction photodiode and a Trench-MOSFET. The OCFET concept is verified by connecting the Ge photodetector to the trench-MOSFET gate and its current-voltage characteristics are investigated in this chapter. Chapter 5, describe the design and the fabrication of a Ge gate heterojunction FET (JFET). The Current-Voltage characteristics of this Optical-JFET are investigated in this chapter.

2

Simulation Tools

This chapter gives an overview of tools of ISE-TCAD, which are used to generate and simulate an optically controlled FET (OCFET). Technology Computer Aided Design is a software dedicated to the design and simulation of semiconductor devices for various applications. ISE-TCAD software package provides a selection of tools to solve fundamental, physical partial differential equations, such as diffusion and transport equations, to model the structural properties and electrical behavior of a semiconductor device.

2.1 GENESISe Workbench

GENESISe is the front-end graphical user interface framework for managing projects, simulation tools and analyzing simulation results [76]. It provides a flexible environment to perform multiple simulations on a single device by parameterizing the structural and physical properties to study the device characteristic variations depending on the values of some parameters in a single project as different experiments. It automatically passes the output file of one tool (for eg. MESH) to the next tool (for eg. DESSIS) in the queue removing the need of a manual control by the user.

The ISE-TCAD package includes following tools,

- DESSIS
- DIOS
- LIGAMENT
- MDRAW
- MESH
- PROSIT
- EMLAB
- SOLIDIS
- ISEXTRACT
- OPTIK
- INSPECT
- TECPLOT

2.1.1. MESH

The mesh generator tool is used to define 1D-3D structures with boundary description and complex grid of the device to be studied. In the boundary file (msh.bnd), the device is defined as a list of geometrical figures that defines the structure. After all the bulk materials are in place, contacts are defined as 1D structure to the surfaces or defined regions. These are used to apply external voltage and calculate the current flow through them.

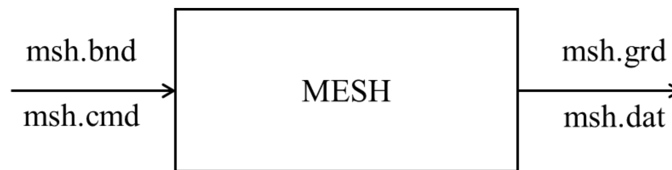


Figure 2.1. MESH design flow

The MESH command file (msh.cmd) contains informations about type, level and distribution of doping for each region as well as the refinement specifications of particular part of the grid. Beside the constant doping concentration in the bulk, doping profiles can be set with the shape of a gaussian or an error function. Before the mesh is finally generated, regions of interest can be defined, in which the mesh points are narrowed down, e.g. in regions with a large change in the doping concentration. The output contains two files namely msh.grd and msh.dat containing the structure of the grid generated and doping information for all grid points respectively. The device structure, generated grids and refinements can be viewed in TECPLOT.

2.1.2. DESSIS

The DESSIS tool provides numerical simulation of the electrical behavior of a single semiconductor device or several devices in a circuit. Numerous physical device models provides a close approximation of semiconductor devices to the real behavior of devices.

These features of dessis can be summarized as [77]:

- A general support for different possible device geometries (1D, 2D, 3D, and 2D cylindrical).
- An extensive set of models for device physics (drift-diffusion, thermodynamic, and hydrodynamic models) and effects in semiconductor devices (optical generation, interface physics, and traps).
- A broad set of non-linear solvers.
- A mixed mode support of electrothermal netlists with mesh-based device models and Spice circuit models
- Possibility of analyzing DC, AC, noise and transient responses.

The MESH output files (msh.dat and msh.grd) along with dessis parameter file (.par) and command file (des.cmd) forms the input of the DESSIS tool. The physical models describing carrier distribution and conduction mechanisms are solved for numerical outputs (voltage, current and charges) of the device. The processing technology and device simulation can be described as schematically shown in fig.2.2,

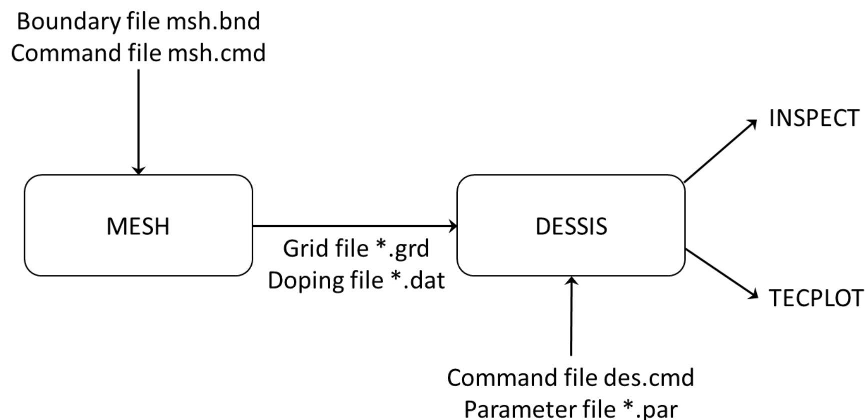


Fig.2.2. Simulation process flow

2.1.3. TECPLOT

Tecplot is a software program dedicated to graphical visualization of simulated 2D and 3D structures and the results of the simulations. It can also export physical quantities, mentioned in the plot section of the dessis file at a cross section of the device. This extracted data in .plt format is an input file for Inspect.

2.1.4. INSPECT

INSPECT is a tool for viewing and analysing graphs of currents, voltages and charges on the electrodes of the device or even at specific points on the grid. It supports DF-ISE and XGRAPH input data formats and export data in either formats. The input files be (.plt) generated by dessis or data of specific parts of the device extracted from Tecplot either in the form of .plt or .xy.

2.2. Models and Parameters

ISE-TCAD uses a set of default parameters for each material, which can be modified either in the physics section of dessis command program or in the material parameter file (.par). Usually these parameter files are available as material.par in the default location. The path of the parameter file can be changed to current project folder by specifying “Parameter = Material.par”, in the file section of the dessis program. In this case any parameter for each material used can be modified by the user. Since this work is focused on germanium (Ge) with 1.55µm wavelength optical source, other materials like Silicon, and SiO_2 are left unchanged. The file section of the dessis.cmd is modified as below to redirect the germanium parameter file path to current directory.

```
File {
Grid = "@grid@"
Doping = "@doping@"
Parameter = "Germanium.par"
}
```

2.2.1. Parameters

Permittivity ε_r: The default value for Germanium in ISE-TCAD is 15.8 [77]. Other closer value for ε_r is 16.0 [78] and [79]. In other university databases like Ioffe Institute [80] and in [81] ε_r =16.2 is found. The default value of ε_r is used in the simulations. The default values of permitivity for Silicon (11.7) and SiO_2 (3.9) are used.

Refractive Index: The refractive index can be defined as,

- A constant in dessis input file
- A dependence on the mole fraction and temperature in dessis parameter file
- A table based optical property that depends on photon energy (eV) can be entered in the DESSIS parameter file.

In this study, the third step is followed to define refractive index (n) along with the extinction coefficient (κ) as a function of wavelength (λ).

The absorption coefficient is computed from the table format of Optik database (TableODB) from the real refractive index (n), extinction coefficient (κ) and wavelength (λ) by,

$$\alpha(\lambda) = \frac{4\pi\kappa}{\lambda} \tag{2.1}$$

The TableODB is defined as follows for absorption coefficient =1000 cm^{-1}[82]

```
TableODB
{ *Table format of the Optik DataBase
*WAVELEN   n        k
#absorption coefficient = 1000 cm^-1
1.54    4.3      0.0123;
1.55    4.3      0.0123;
1.56    4.3      0.0123;
1.57    4.3      0.0123;
}
```

Thermal Conductivity: Temperature dependent thermal conductivity is defined by,

```
Kappa
{ *  Lattice thermal conductivity
  * Formula = 1:
  * kappa() = kappa + kappa_b * T + kappa_c * T^2
        kappa  = 1.66667       # [W/(K cm)]
        kappa_b        = 0.0000e+00# [W/(K^2 cm)]
        kappa_c        = 0.0000e+00# [W/(K^3 cm)]
}
```

The default value in ISE is 1.6667 $W.K^{-1}.cm^{-1}$ which is for 125°K. In this study kappa=0.60 W. $K^{-1}.cm^{-1}$ is used for 300°K [83]. Since the temperature dependence is not studied extensively in this project, this model is rarely used.

*Bandgap E_g and Electron Affinity χ_0***:** ISE-TCAD uses Eg = 0.74 eV (0°K)as the default value. This can be found also in several books on semiconductors, e.g. [78]. The default value from Synopsys Sentaurus as well as the values from the semiconductor books is χ_0 = 4.0 eV [78]. Default values are used for both parameters.

Recombination: The doping dependence of the Shockley–Read–Hall lifetimes is modeled in DESSIS with the Scharfetter relation:

$$\tau_{dop}(N_i) = \tau_{min} + \frac{\tau_{max} - \tau_{min}}{1 + \left(\frac{N_i}{N_{ref}}\right)^{\gamma}} \qquad (2.2)$$

The Scharfetter relation is used when Doping Dependence is specified in SRH recombination. In this study, several values of τ_{max} and τ_{min} are used to vary the recombination time of the carriers.

2.2.2. Physical Models

In ISE-TCAD a number of physical models are provided to describe the device physics as closely as possible to the real device. These models deal with the behavior of the carrier

in combined effects of various boundary conditions like lattice temperature, electrostatic potentials and fields, external forces, band gap variations and quantum effects. Such models, depending on the type of device and operating conditions, have to be included in the model to perform simulations and provide reliable predictions about the device characteristics. The models, which are used in the simulation, are stated in the Physics section of the simulation command file. In this section, the models used for this study are explained. In this study different models are used for individual materials like Silicon and Germanium.

2.2.2.1. Band Gap Narrowing

In device simulation, energy band gap, intrinsic carrier concentration, band edge density of states and carrier effective masses are some of the most crucial properties of a semiconductor material. Band gap narrowing is turned on by default in DESSIS. The effective intrinsic density model can be chosen in the EffectiveIntrinsicDensity statement in the Physics section of the command file. For example to activate Slotboom in band gap narrowing,

```
Physics{
        EffectiveIntrinsicDensity (BandGapNarrowing ( Slotboom ))
    }
```

The variation of the intrinsic silicon band gap with temperature can be expressed by,

$$E_g(T) = E_g(0) - \frac{\alpha T^2}{(T + \beta)} \tag{2.3}$$

where T is the lattice temperature, $E_g(0)$ is the band gap at 0K, α and β are empirical material constants. The temperature variation of the band gap is equally distributed between the conduction and valence bands. Each EffectiveIntrinsicDensity model has a different default value for $E_g(0)$. To support this variation, a correction term $\delta E_{g,0}$ is introduced and the following modification to Eg(0) is applied,

$$E_g(0) = E_{g,0} + \delta E_{g,0} \tag{2.4}$$

2.2.2.2. Effective Intrinsic Density

The intrinsic carrier density $N_i(T)$ of undoped semiconductor is provided by,

$$n_i(T) = \sqrt{N_c(T)N_v(T)e^{-\frac{E_g(T)}{2kT}}} \tag{2.5}$$

Considering the effect of band gap narrowing, the effective intrinsic density is defined as,

$$n_{i,eff} = n_i \gamma_{BGN} \tag{2.6}$$

where, the factor γ_{BGN} is,

$$\gamma_{BGN} = exp\left(-\frac{\Delta E_g}{2kT}\right) \tag{2.7}$$

2.2.2.3. Transport Models:

ISE-TCAD offers a number of transport models for various deigns and requirements. Depending on the type of material and desired level of accuracy, we can select four different transport models: Drift-diffusion (DD), Thermodynamic (TD), Hydrodynamic (HD) and Monte Carlo modes. In this study, drift-diffusion model is used to model the current transport.

The drift-diffusion model is used as default for the simulation of carrier transport in semiconductors and is defined by the formulated set of basic semiconductor equations. The current densities under this model for the electrons and holes are given by [77]:

$$J_n = -nq\mu_n \nabla\phi_n \tag{2.8}$$

$$J_p = -pq\mu_p \nabla\phi_p \tag{2.9}$$

where μ_n and μ_p are the electron and hole mobility, Φ_n and Φ_p are the electron and hole quasi Fermi levels respectively.

2.2.2.4. Mobility Models

Several mobility models available for the charge carriers. The simplest mobility model is the constant mobility, in which the mobility is just a function of lattice temperature. For doped materials, the carriers scatter with the impurities which leads to a degradation of the mobility. This is addressed by using doping dependent mobility model. In other cases, the mobility degrades in interfaces like silicon/oxide in the channel region of MOSFET, where Enormal mobility model is used. When the velocity saturates to a finite speed V_{sat} and the carrier drift velocity is no longer proportional to the electric field strength, high field saturation mobility model is used. The mobility models are selected in the Physics section as arguments of the Mobility keyword:

Physics {Mobility (<arguments>)…}

2.2.2.5. Doping Dependent Mobility Model

In doped semiconductors, scattering of the carriers by charged impurity ions leads to degradation of the carrier mobility. DESSIS supports two models for doping dependent mobility namely, Masetti and Arora models. The selection of the default models for each material may also be controlled by the variable formula, which is accessible in the DopingDependence section of the parameter file:

```
DopingDependence:
{
  formula= 1 , 1# [1]
}
```

In this study, Masetti model [84] is selected in Germanium parameter file for doping dependent mobility degradation.

$$\mu_{dop} = \mu_{min1} exp\left(-\frac{P_c}{N_i}\right) + \frac{\mu_{const} - \mu_{min2}}{1 + \left(\frac{N_i}{C_r}\right)^{\alpha}} - \frac{\mu_1}{1 + \left(\frac{C_s}{N_i}\right)^{\beta}} \qquad (2.10)$$

where, $N_i = N_D + N_A$ denotes the total concentration of ionized impurities. The reference mobilities, μ_{min1}, μ_{min2} and μ_1, the reference doping concentrations P_c, C_r and C_s and the exponents α and β are accessible in the parameter file in the section.

2.2.2.6. Mobility Degradation at Interfaces

The Lombardi model is activated in two ways depending on the method required to compute the transverse field $F_{\perp}$. To select the calculation of field perpendicular to the semiconductor –insulator interface, specify the keyword Enormal in the mobility statement:

Physics { Mobility (Enormal ...) ...}

In the channel region of a MOSFET, the high transverse electric field forces carriers to interact strongly with the semiconductor–insulator interface. Carriers are subjected to scattering by acoustic surface phonons and surface roughness. The Lombardi model describes the mobility degradation caused by these effects. DESSIS enhances standard Lombardi model with an additional equation to include a free carrier and doping dependence in an exponent [85]. The keyword Enormal is specified in the mobility statement to activate the Lombardi model with normal to the interface method of computing.

2.2.2.7. High Field Saturation

In high electric fields the carrier drift velocity is no longer proportional to the electric field strength, instead the velocity saturates to a finite speed vsat. DESSIS supports Canali model, Transfered-Electron model and Meinerzhagen-Engl models. The high field saturation models are activated by specifying the HighFieldSaturation argument in the Mobility keyword:

Physics { Mobility (HighFieldSaturation (<arguments> ...) ...}

The Canali model originates from the Caughey–Thomas formula, but has temperature dependent parameters, which were fitted up to 430 K by Canali et al.

$$\mu(F) = \frac{\mu_{low}}{\left[1 + \left(\frac{\mu_{low}F}{v_{sat}}\right)^{\beta}\right]^{1/\beta}} \tag{2.11}$$

where μ_{low} denotes the low field mobility. Dessis supports two velocity saturation models, model 1 which is a part of Canali model is used in this study.

$$v_{sat} = v_{sat,0}\left(\frac{T_0}{T}\right)^{v_{sat,exp}} \tag{2.12}$$

where T denotes the lattice temperature and T_0 = 300 K. This model is recommended for silicon. The silicon defaults are given in table 2.1,

Symbol	Parameter	Electron	Hole	Unit
V_{sat0}	vsat0	$1.07x10^7$	$8.37x10^6$	cm/s
$V_{sat,exp}$	vsatexp	0.87	0.52	1

Table 2.1. Default parameters for Silicon.

2.2.2.8. Recombination Models

Recombination via deep levels in the gap is usually labeled Shockley–Read–Hall (SRH) recombination. In DESSIS, the following form is implemented:

$$R_{net}^{SRH} = \frac{np - n_{i,eff}^2}{\tau_p(n + n_1) + \tau_n(p + p_1)} \tag{2.13}$$

with,

$$n_1 = n_{i,eff} e^{\frac{E_{trap}}{kT}} \quad (2.14)$$

and

$$p_1 = n_{i,eff} e^{\frac{-E_{trap}}{kT}} \quad (2.15)$$

where E_{trap} is the difference between the defect level and the intrinsic level. The variable E_{trap} is accessible in the parameter file. The Shockley–Read–Hall model is activated by specifying the SRH argument:

Physics { Recombination (SRH ...) ...}

The doping dependence of SRH recombination is explained in the previous section with the minimum and maximum carrier life times. In this study, the SRH recombination with doping dependence is used only for Germanium. A list of parameters used in the models are shown in table 2.2.

Parameters	Ge	Si
E_{g0}	0.744	1.16
χ_0	4.0	4.05
ε_r	15.8	11.7
n	4.3	3.45
k	0.0123	--

Table 2.2. Parameters used for Si and Ge

3

OCFET Design and Simulations

3.1. Device Structure

The OCFET structure in many aspects is comparable to a traditional MOSFET, with a germanium absorption layer as gate in order to make the device sensitive to near infra-red light. In the optically controlled FET, the input light modulates the channel conductivity in silicon with optically induced electric field in the germanium gate.

For our studies, we adopted a standard 0.18 μm n-MOSFET structure with source/drain extensions (SDE) and retrograde well (RW) [86] provided with a 0.2 μm n-type Ge layer between the channel oxide and the metal gate, later to be used to bias the device at a suitable operating point. The device physical parameters are modified to study the device characteristics. The parameters used in the simulations are listed in the table 3.1 and the device width W was fixed at 1 μm. The simulated OCFET is a normal incidence device for simplicity and I have used 1550nm wavelength light for the entire simulation work.

During the simulations, I modeled the photo-generation in the Ge layer employing a photo-generation model with an optical absorption coefficient of 1000cm^{-1} at 1.55μm [82]. In such

condition, the photo-generation rate along the Ge layer is simply described by the following equation:

$$G(z,t) = \phi(t)\alpha e^{-\alpha(z-z_0)} \tag{3.1}$$

where $\phi(t)$ is the time dependent incident photon flux, α is the optical absorption coefficient and z_0 is the coordinate of the top Germanium surface. Device simulations are focused on the dark and illuminated drain current ratio Ion/Ioff and the turn-off time following an optical pulse.

Parameters	Doping [cm^{-3}]	Thickness [nm]
Substrate p-Si	$2x10^{17}$	200
Source/Drain n+ Si	$2x10^{20}$	100
SDE n+ Si	$2x10^{20}$	40
Retrograde well	$5x10^{17}$	150
t_{ox}	--	4
Gate n-Ge	$10^{16} – 10^{18}$	200

Table.3.1. List of device parameters used in the simulations

In all simulations the bulk Ge model has been suitably modified in order to take into account the quality of the material. In particular the Schockley-Read-Hall (SRH) recombination model with different carrier lifetimes has been used to model a wide range of crystal quality. A 3D representation of the simulated device structure of the OCFET is shown in fig.3.1.

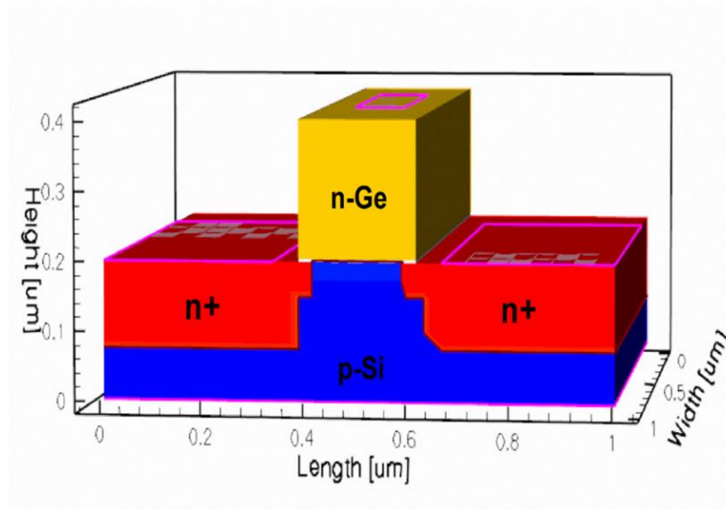


Fig.3.1. Schematic 3D representation of Optically controlled FET

3.2. Operation

The principle of operation of the OCFET is based on the modulation of the Si channel conductivity by applying an electric field on the gate terminal. This electric field is optically induced much like a photovoltaic device [78] i.e. by charge separation in the Ge film on the top of the gate oxide. In the presence of NIR light, absorption occurs only in Ge layer [87]; photo-generated carriers are separated by the electric field, electrons towards the gate contact, and holes towards the Ge/SiO_2 interface. This results in a net photovoltage across the absorption region adding to the applied offset gate bias. The drain current (I_D) can be calculated by considering the OCFET as a conventional MOSFET with added photovoltage to the gate.

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}\left(V_{GS} - V_{th} - V_{ph}\right)^2 \qquad (3.2)$$

where, μ_n is the electron mobility, C_{ox} is oxide capacitance, W is the gate width, L is gate length, V_{th} is the device threshold voltage and V_{ph} is the photovoltage. The optically induced voltage (V_{ph}) is proportional to the logarithm of the optical power, similar to the open circuit voltage [78] of an illuminated pn junction. So the drain current depends on both gate bias (V_G) and photovoltage (V_{ph}) with,

$$V_{ph} \propto ln(P_{opt}) \tag{3.3}$$

The OCFET simulated with the parameters in table 3.1 exhibits a threshold voltage of 0.7V. Since the external voltage is fixed, the positive charge accumulated at the oxide interface induces a migration of electrons in the Si side towards the oxide thus inducing a band bending. The energy band diagram at V_{GS}= 0V and V_{GS}= 0.6V are shown in the fig. 3.2 (a) and (b) respectively, calculated at the center of the device both in dark and under 10 μW illumination.

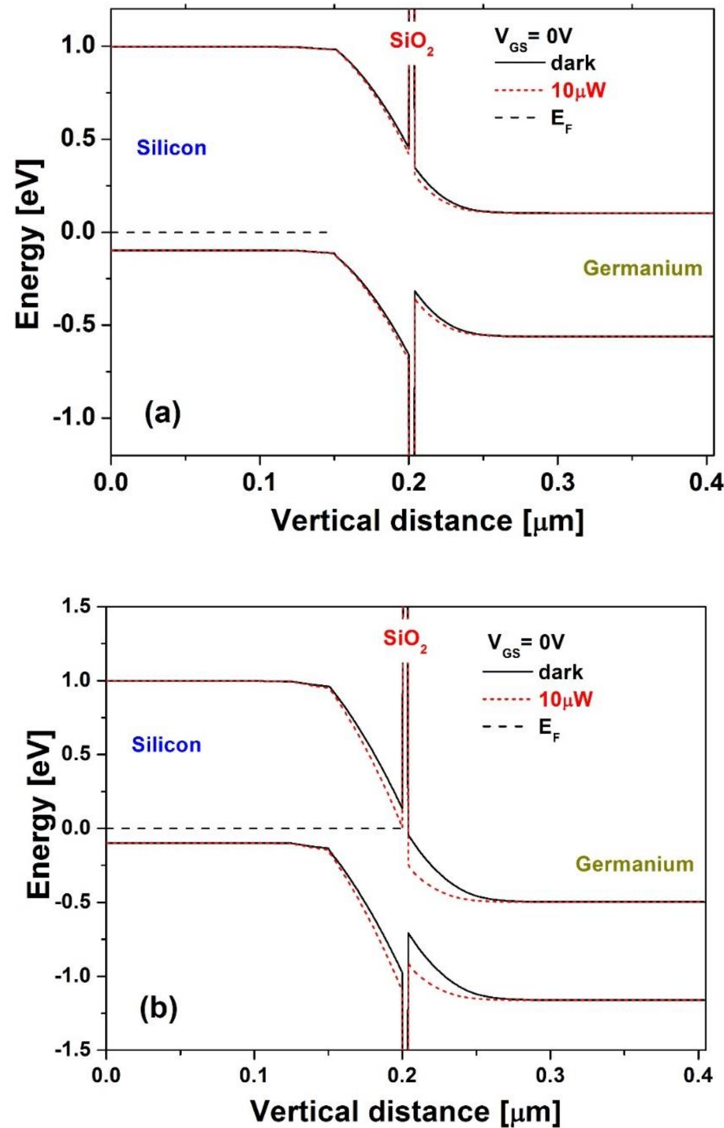


Fig. 3.2 Energy band diagrams (a) without offset gate bias in dark and 10μW optical input and (b) with offset gate bias of 0.6V in dark and 10 μW optical input.

To this extent, a built-in potential should stand in the Ge film in order to promote photo-carriers moving towards the oxide interface. When no external voltage is applied to the gate terminal, the 10 μW optical signal induces a bending of about 50 mV in the Si conduction band (CB). This value is far from the 0.7 V threshold voltage. Therefore, a V_{GS} offset near the threshold is needed to ensure channel inversion by the optical signal. Such gate bias enhances the electric field in the Ge layer thus improving photo-carrier separation and inducing a larger band bending. With a 0.6 V gate bias, the 10μW signal induces a Si CB bend of about 0.15 V, which allows for strong inversion and OCFET switching to conduction.

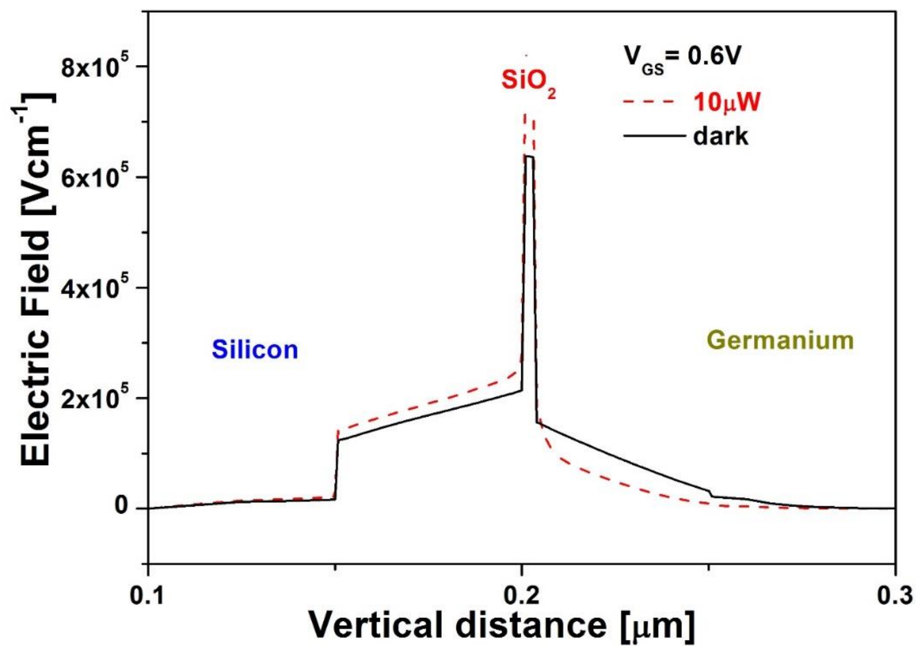


Fig. 3.3. The electric field across the vertical cross section of the device in dark (solid) and illuminated with 10μW optical input (dashed) with a offset gate bias V_G=0.6V.

Fig. 3.3 shows the electric field distribution of the Ge-oxide-Si cross section at the center of the device under both dark and 10μW illumination at 1.55μm and a gate bias V_{GS}=0.6V applied between the gate and the body. The figure shows the increased electric field in the silicon channel region. This facilitates the image charge formation in the Si channel region at the oxide interface to ensure charge neutrality, thus modulating the channel conductivity due to increased carrier density. The change in electron and hole density at

V_G=0.6V with dark and 10μW optical power in Silicon channel and Germanium layer is shown in fig. 3.4 (a) and (b) respectively. The solid lines shows the electron and hole density under dark condition, with the gate biased at 0.6V. When illuminated, the hole density at Ge side increases from ~$2e^{17}$ cm^{-3} to ~$6e^{18}$ cm^{-3}, whereas at the Si, channel inversion takes place with increased electron density from ~$6e^{15}$ cm^{-3} to ~$3e^{17}$ cm^{-3} thus turning the transistor on.

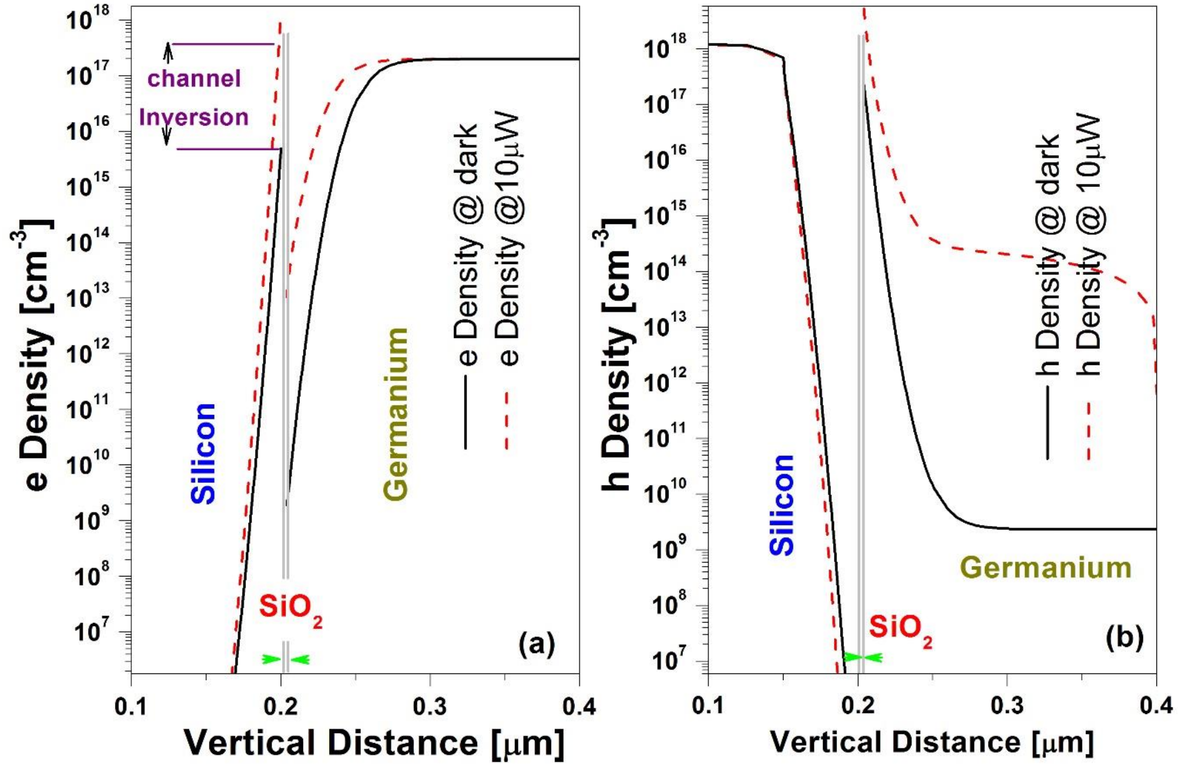


Figure 3.4. Electron (a) and Hole (b) densities at Germanium gate and Si channel regions with gate bias V_G=0.6V in dark (solid) and 10μW optical input power.

3.3. Current Voltage Characteristics:

Device performance are strictly related to the built-in potential distribution across the Ge-oxide-Si gate structure, which depends on Ge and Si doping, oxide thickness as well as gate bias V_G. As anticipated, Ge doping concentration balances the potential distribution across the structure. The simulated device exhibits best results when Germanium doping matches the Silicon doping concentration. Figure 3.5 (a) shows the drain current vs gate voltage of the device when the photosensitive gate is illuminated with optical power varying from 1nW to 10μW and an offset gate bias of 0.6V. With the offset gate bias, the OCFET

behaves similar to the conventional MOSFET even in dark conditions. It is evident from the figure that the input light generates additional gate voltage causing a shift in the threshold voltage. The dark threshold voltage (Vth) is 0.7V and it decreases with increased optical input.

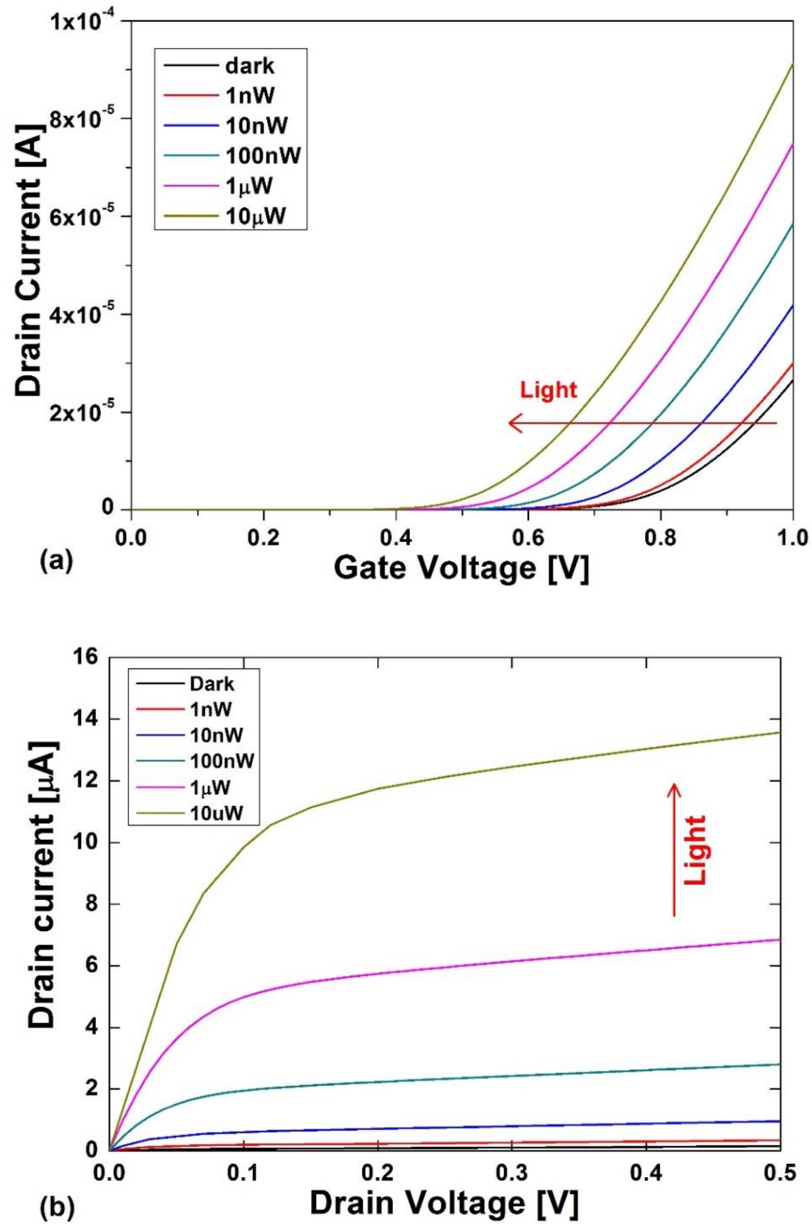


Figure 3.5. (a) Drain current vs Gate voltage with a drain voltage V_{DS}=0.5V (b) Drain current vs Drain voltage of 0.18μm channel length device with the parameters shown in table 3.1. The input optical power is varied from 1nW to 10μW.

Figure 3.5 (b) shows the drain current vs drain voltage with optical power varying from 1nW to 10µW for V_G = 0.6V. In dark condition the drain current is about 90nA at V_{DS}=0.5V while increases above 13µA at the same drain voltage for 10µW optical power thus allowing an on/off ratio of about 100:1. Simulations are in good agreement with a simple model that takes into account the quadratic behavior of the drain current with the gate voltage (Eqn. 3.2). Figure 3.11 (shown in the next paragraph) plots the drain current dependence on optical power.

The p-Silicon and n-Germanium doping concentration are kept equal at $2x10^{17}cm^{-3}$. More studies have been conducted with varying Ge and Si doping and will be explained later in this chapter.

Another important parameter is the gate oxide thickness because it affects the reciprocal influence of Germanium and Silicon and their band bending. The depletion effects occur in gate near the oxide interface which acts to reduce the gate capacitance and inversion-charge density for a given gate drive [88]. Fig. 3.6 shows the Ion/Ioff ratio versus oxide thickness at 10µW optical power with V_G=0.6V and V_G optimized for higher Ion/Ioff ratio. In the same figure, the threshold voltage as a function of oxide thickness is plotted. The drain voltage for these simulations are constant at 0.5V unless specified otherwise.

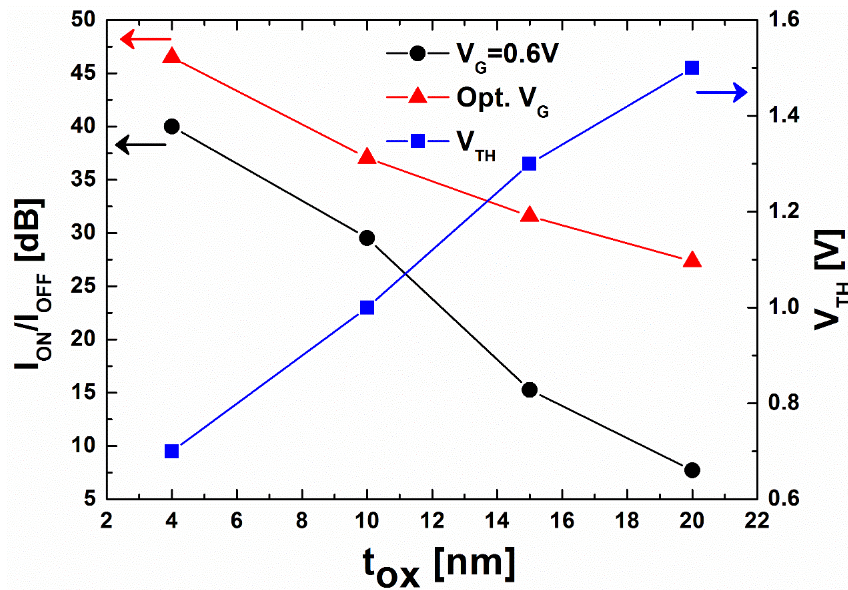


Figure 3.6 I_{on}/I_{off} ratio and threshold voltage V_{th} versus oxide thickness t_{ox}, at 10µW optical power at constant (circles) and optimized V_G (triangles) for higher ratio.

Thicker oxides increase the threshold because a larger voltage drops across the oxide thus reducing the channel modulation effect. This effect limits the I_{on}/I_{off} ratio as expected in traditional MOSFET. This effect can be partially avoided selecting the optimum V_G (triangles) or applying the same scaling to the gate length (discussed later in the chapter).

3.3.1 Doping Dependence

To ensure the channel formation, a suitable band bending must be obtained in the germanium film acting on the doping type and concentration of Ge and Si as in pn junctions. Ge doping must be of opposite type with respect to the Si channel doping, e.g. n-Ge for n-channel FET (p-type Si body).

For constant channel doping and gate voltage, if the Ge doping increases, the space charge region shortens [89, 90], thus reducing the achievable photo-voltage and, limiting the channel modulation effect. On the other hand, a lower Ge doping with respect to Si reduces the potential drop in the Ge gate reducing the charge separation and providing a smaller equivalent voltage drop on the gate oxide; therefore more light is required to achieve carrier inversion.

The doping dependence of the OCFET I_{on}/I_{off} ratio is shown in fig.3.7. The squares shows the I_{on}/I_{off} ratio versus Ge doping when a 10μW beam illuminates the OCFET with 4nm gate oxide, $2x10^{17}cm^{-3}$ Si doping and constant V_G at 0.6V. As expected, the device exhibits best results when Ge doping matches the Si doping. Simulations also show (circles) that by changing V_G, I_{on}/I_{off} can be optimized and ratios exceeding 70dB (3160:1) can be obtained [91].

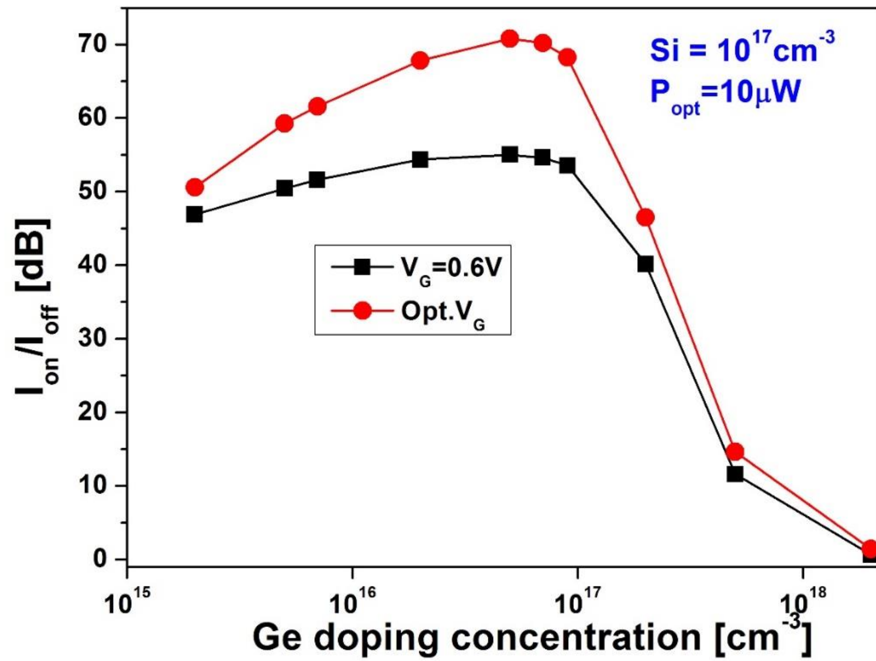


Figure 3.7 Ion/Ioff ratio vs Germanium doping concentration with constant Silicon doping of 10^{17}cm^{-3} for constant gate bias (0.6V) and optimized gate bias for higher ratio. The input optical power is 10μW

Therefore, a trade-off must be found between channel doping and Ge doping. The doping of the Silicon body in the 0.18μm technology is of the order of 10^{17} cm^{-3}, therefore, a suitable Germanium gate doping would be around 10^{17}cm^{-3}. Fig.3.8 shows the I_{on}/I_{off} ratio at 10μW optical power when Silicon and Germanium doping concentration are changed simultaneously (N_{Ge}=N_{Si}) at constant V_G (squares) and optimized V_G (circles) for higher I_{on}/I_{off} ratio. Larger I_{on}/I_{off} ratio is obtained with increased doping up to about 10^{17}cm^{-3}. This increase in Ion/Ioff ratio can be attributed to the increased photovoltage in the gate region.

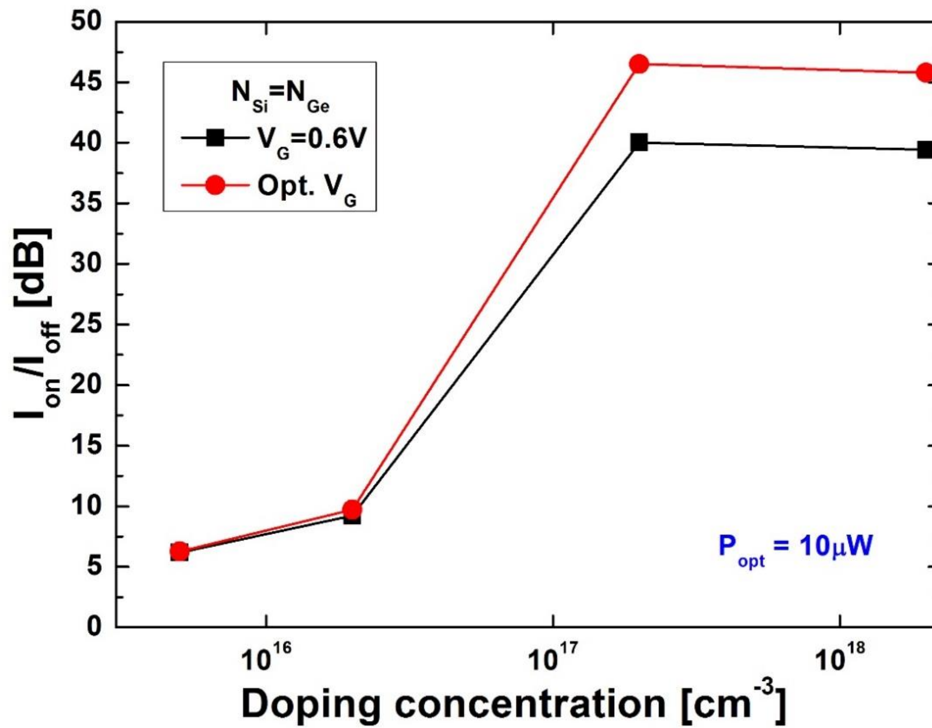


Figure 3.8. Ion/Ioff ratio vs symmetric Silicon and Germanium doping concentrations with constant gate bias (0.6V) and optimized V_G for maximum Ion/Ioff ratio.

3.3.2. Gate Voltage Dependence

The gate bias V_G here is an offset voltage in order to promote the charge separation in the absorption region. It must be noted that the drain current depends on the gate bias as well as the generated photovoltage. So the gate bias can be used to improve the gain of the device up to a certain point. The drain current (I_D) at different gate voltage and optical power (P_{opt}) is shown in figure 3.9. It is clear that the drain current increases with gate bias (V_G), but the change is not completely linear when the gate voltage is increased beyond the threshold voltage of the device. The ratio between the dark and light current tends to decrease as the dark current increases with gate voltage. This is shown in fig. 3.10, where the ratio between dark and light current (Ion/Ioff) is plotted at increasing gate bias.

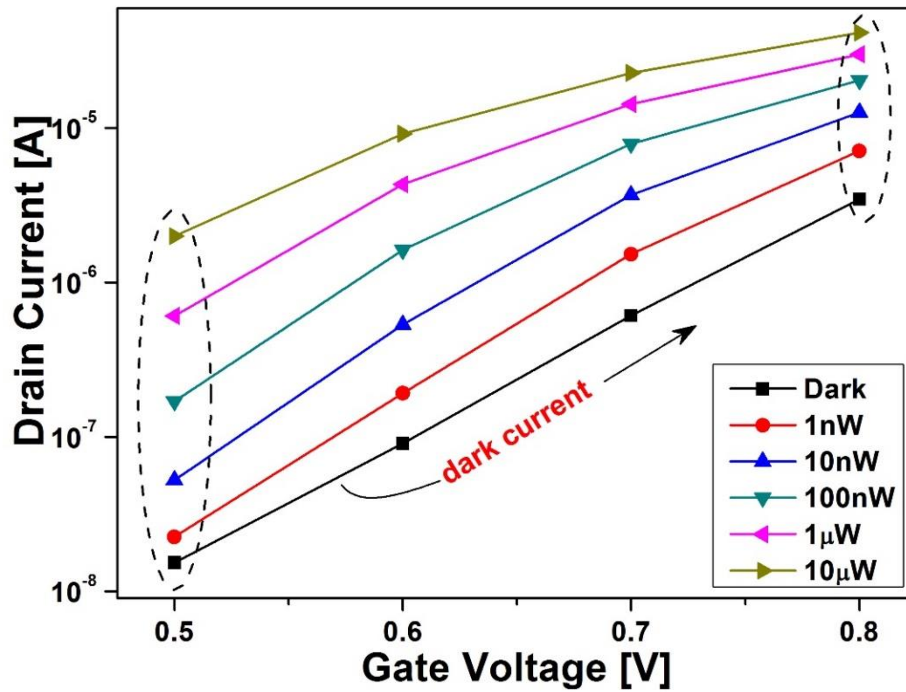


Figure 3.9 Drain current vs the gate voltage at optical power varying from 1nW to 10μW. The drain voltage was kept constant at 0.5V.

The optical power is varied from 1nW to 10μW at different gate voltage (V_G). At V_G=0.5V the Ion/Ioff ratio increase from 3dB to 40dB when the optical power is varied from 1nW to 10μW. However, at higher gate voltage (V_G=0.8V) the increase in Ion/Ioff ratio is minimum (between 6dB to 21dB) for the same range of optical power, even when the absolute Ion increases consistently. When V_G is further increased, the ratio decreases due to the larger dark current with the gate bias approaching the device threshold voltage.

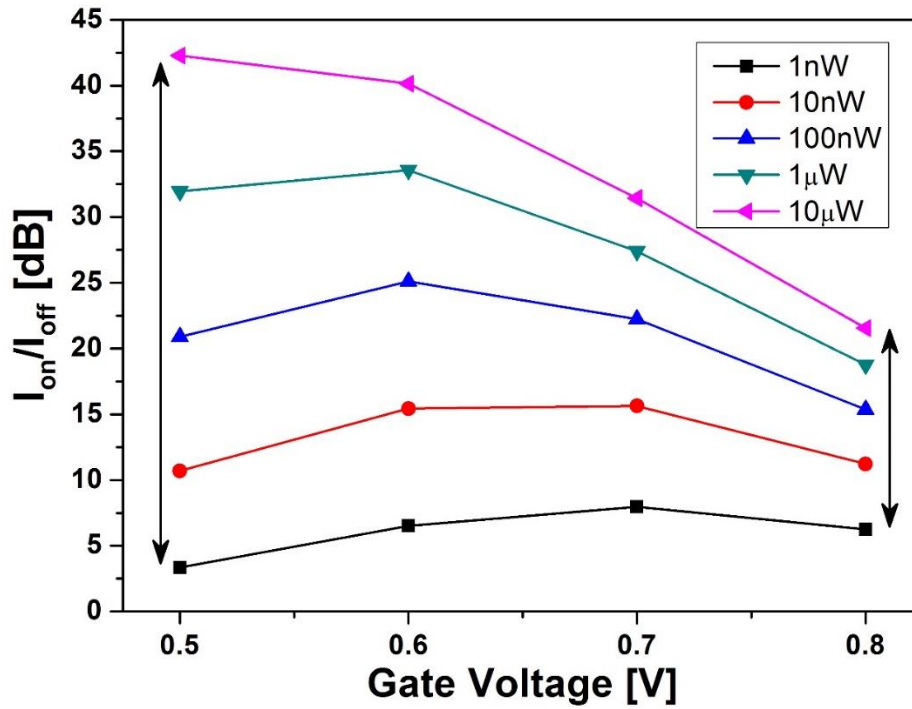


Figure 3.10 Ion/Ioff ratio vs the gate voltage at optical power varying from 1nW to 10μW.

3.3.3. Optical Power Dependence

From equations (3.2) and (3.3), the drain current has a quadratic dependence on gate voltage and a squared logarithmic dependence on input optical power. Figure 3.11 shows the photocurrent (squares) and responsivity (triangles) at different optical powers (P_{opt}) with a gate bias (V_G) of 0.6V. The current scales less than linearly with the optical power, therefore, device responsivity at lower optical power is higher with respect to larger optical signals.

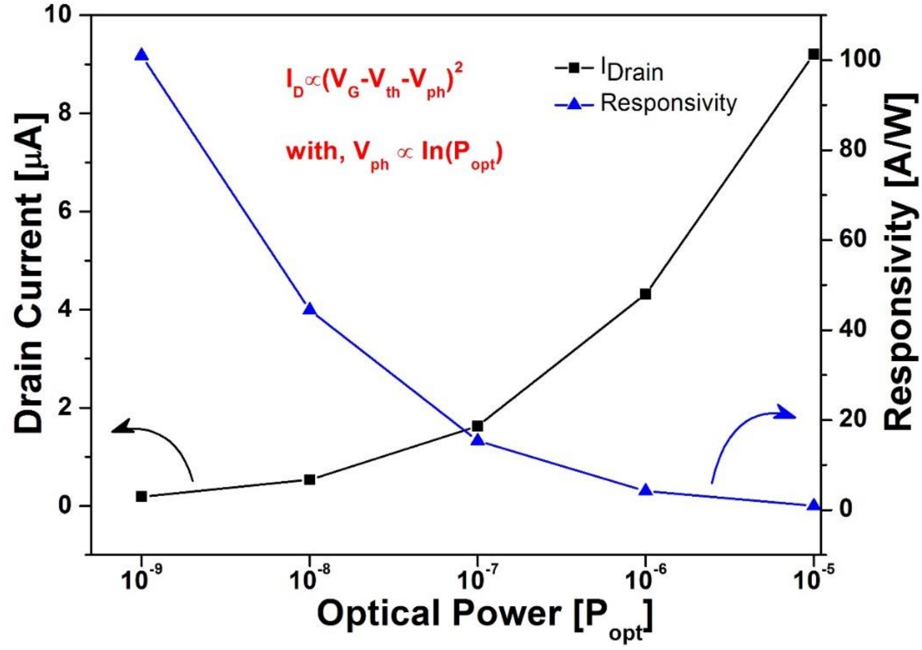


Figure 3.11 Drain current (squares) and Responsivity (triangles) depending on the input optical power (Popt). The input gate bias V_G=0.6V.

In terms of responsivity (drain current over input optical power), from Fig.3.11, I obtained a maximum responsivity of 100A/W, corresponding 1nW optical input light and it decreases to 4A/W for 1μW and 0.9A/W when the optical input is increased to 10μW. It must be noted that in all simulations the 1.55μm optical power is the incident power at normal incidence. In such conditions, the 200nm thick Ge active layer absorbs less than 2%, since the used optical power is scaled by,

$$Absorbed\ Intensity = 1 - \exp(-\alpha * d) \tag{3.4}$$

where, α is absorption coefficient, which depends on extinction coefficient k and d is the thickness of absorbing layer. When the responsivity is scaled for effective absorption, it yields 5000A/W at 1nW optical power. The absorption coefficient used here is 1000cm^{-1} with the extinction coefficient k=0.0123. A much more efficient use of the input power could be obtained in waveguided geometry as suggested in [92]. By increasing the input optical power P_{opt}, the modulation current (I_{on}-I_{off}) was saturated. If the current modulation was due to the photocurrent in the FET channel, the modulation current would have increased linearly

by increasing the irradiated light power. However, the modulation current was saturated even by increasing the input light power. This saturation characteristic is one of the proofs that this device was controlled by the electric-field change due to the field-screening effect of photogenerated carriers in the FET gate. Of course, absorption saturation in the Ge region determined the saturation point of irradiated light power [93].

3.3.4 Channel Length Dependence

In order to investigate the possibilities and benefits of scaling, OCFET devices with different effective channel length (L_{eff}) are simulated applying constant field scaling [78]. The three factors that determine the speed of this device are the cut-off frequency of the FET region, the RC time constant of the reverse-biased absorption region, and the drift velocity of the photogenerated carriers in the absorption region. The cut-off frequency of the FET region is given by $f_T(v) = v/2\pi L$. The cut-off frequency of the FET region increases by shortening the channel length.

In this study gate oxide, doping concentrations, junction depth and gate length are scaled by a factor k. The 1μm channel width and drain bias (V_{DS}) were kept constant for all the devices. Since there is a change in threshold voltage, the gate bias (V_G) is varied accordingly and kept just below its threshold voltage. Figure 3.12 shows the net photocurrent (I_{on}-I_{off}) and the corresponding responsivity versus channel length (0.09μm to 0.35μm) for 10μW input optical power with V_{DS}=0.5V.

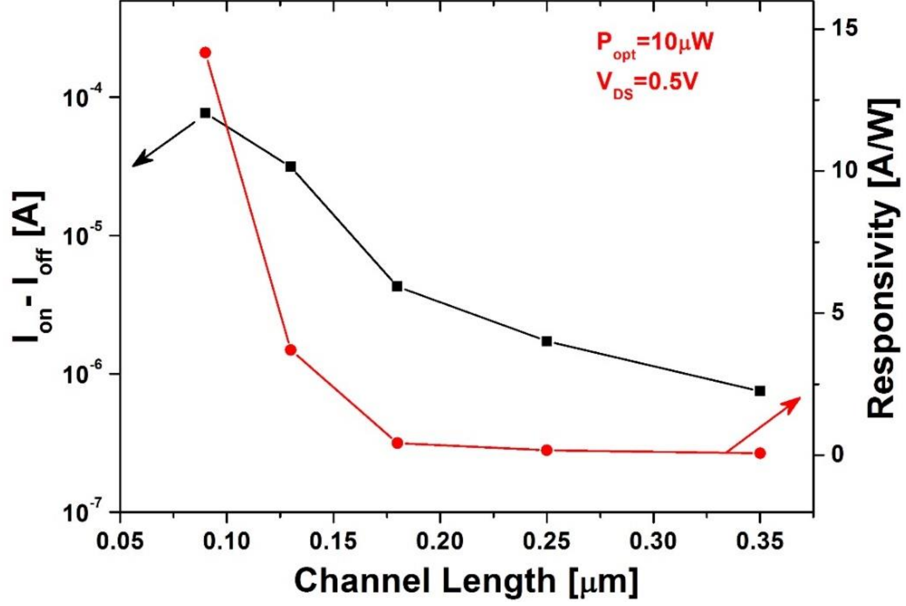


Figure 3.12 Responsivity vs channel length (0.09 μm to 0.35 μm) at 10μW input optical power of wavelength 1.55μm. The channel width and drain voltage are kept constant at 1μm and 0.5V respectively.

As expected, the modulation current (I_{on}-I_{off}) increases by shortening the gate length, thus increasing the responsivity of the devices. With a scaling factor of 3.8, a 100x increase in modulation current was observed from 0.35μm to 0.09μm channel length. This is due to the increase in photovoltage by shrinking the gate area, which in turn increases the drain current of the scaled down device. The increase in responsivity with reduced channel length is in agreement with the scaling rule [93].

3.3.5 Gate Thickness Dependence

The responsivity of a photodetector depends on the absorption coefficient (α), internal quantum efficiency η_{int}, surface reflection losses and absorption layer thickness as shown below in eq. (3.5),

$$\Re = (e\lambda/hc)\left(1 - R_{refl}\right)[1 - exp(-\alpha_{Ge}t_{Ge})](\eta_{int}) \qquad (3.5)$$

In a normal incidence device, the responsivity increases with absorption layer thickness [94] and [95] with a trade-off in device bandwidth, which will be discussed later

in this chapter. Figure 3.13 shows the OCFET drain current with various Germanium layer thickness under dark condition and at 1µW and 10µW optical power. The gate voltage (V_G) is kept constant (0.6V) for all the devices and the thickness is varied from 50nm to 400nm. Throughout, the dark current remains relatively similar, since there is no change in channel formation for the applied gate bias. The Germanium layer thickness is dictated by a trade-off between efficiency and bandwidth.

The drain current of the device with 50nm Germanium layer increases from around 100nA to 3.5µA for 10µW optical power and maximum change in drain current is observed for 400nm Germanium layer from around 100nA (dark) to 16µA for 10µW optical power thus increasing the responsivity. This corresponds to an increase in Ion/Ioff ratio from 35 to 160 associated to the increase in Ge layer thickness.

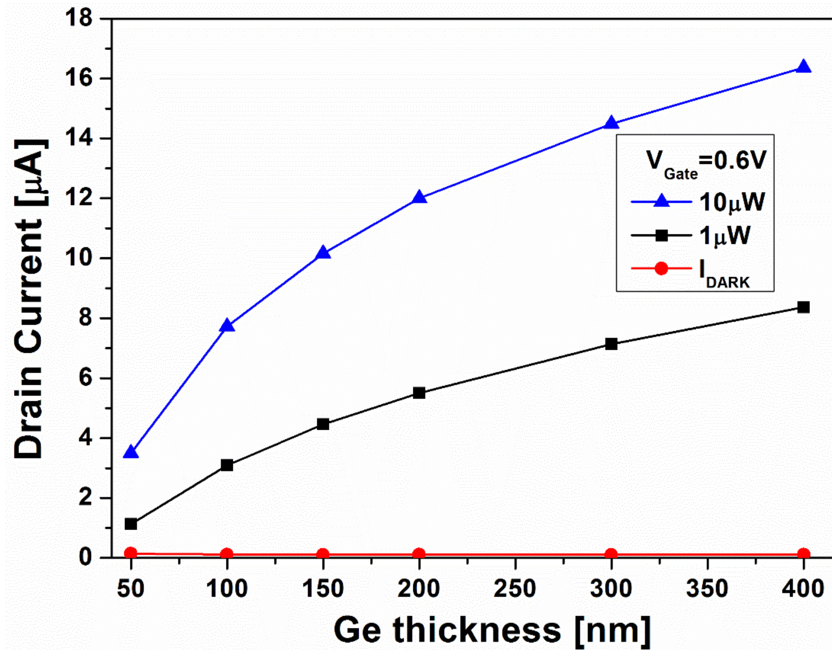


Figure 3.13. The drain current as a function of Germanium layer thickness at dark conditions and at 1µW and 10µW optical power. The gate bias is constant at 0.6V

The increase in drain current in devices with thicker Germanium layer is due to the increased photon absorption. The smaller drain current in thinner Germanium devices can be attributed to incomplete absorption of photons. From figure 3.13, the responsivity of OCFET with 50nm Ge layer was 1.1 A/W at 1nW optical power, which increases to 8.3 A/W for 400nm thick Ge layer at same optical power.

3.4. Dynamic Characteristics

The OCFET time response depends on the intrinsic transistor cutoff frequency $f_{T,}$ the transport in the Ge layer governing the accumulation and removal of carriers at the oxide interface and the RC time constant of the Germanium layer. In particular, the oxide capacitance, the channel dimensions and the carrier mobility determines the OCFET f_T. Therefore, it is related to the employed technology and it can be increased by shortening the channel length and using higher mobility materials in the channel. We have evaluated a f_T as high as 25GHz for the modeled device (in agreement with the typical f_T of the 0.18µm node) corresponding to time response in the order of 10 ps. The dimension of the Germanium layer and the carrier lifetime dictates the RC time constant, which limits the cutoff frequency in short channel devices.

The RC time constant can be reduced by decreasing the Ge layer dimensions. Concerning the transport in Germanium layer, as photocarriers recombine mainly by SRH recombination, we expect a strong dependence of the time response on the Ge minority carrier lifetime. The recombination depends mainly on material quality and doping concentration.

3.4.1 Carrier Lifetime Dependence

Since there is no TCAD model available for the polycrystalline Germanium, I made few changes in the default parameters in the Germanium material model. I have introduced optical extinction coefficient and refractive index for Germanium at 1.55µm wavelength. In this study, I have also used SRH recombination model as a main recombination mechanism with doping dependance with Scharfetter relation to modify the material property. The changes made in Germanium material parameters and physical models are described in Chapter 2. With the Scarfetter relation, I have used mainly τ_{min}=0 in most of the simulations to keep the doping dependent Shockley–Read–Hall life time fixed. A schematic representation of the simulated circuit to study the transient response of the OCFET is shown in fig. 3.14.

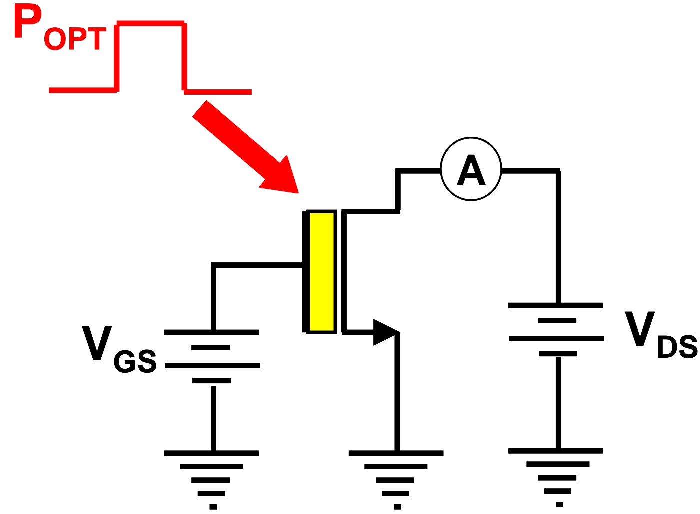


Figure 3.14 Schematic representation of the simulated circuit for temporal response

From the continuity equations under low injection, the following simple expressions for the gate voltage change (photovoltage) during the rise and fall transient can be derived [7]:

$$\Delta V_G^{rise}(t) = \frac{kT}{q} ln\left(\frac{\alpha\tau I}{p_0}\left(1 - e^{-\frac{t}{\tau}}\right)\right) \quad (3.6)$$

$$\Delta V_G^{fall}(t) = \frac{kT}{q} ln\frac{\alpha\tau I}{p_0} - \frac{kT}{q}\frac{t}{\tau} \quad (3.7)$$

where, k is the Boltzmann constant, T the temperature, q the electron charge, α the optical absorption coefficient, τ the Germanium carrier lifetime, I the photon density and p_0 the hole concentration at equilibrium. The equations predict $t_{rise} \ll t_{fall}$ and both t_{fall} and I_{on} decreasing as τ decreases. The absorption coefficient α is calculated from the optical database table in the Ge parameter file from refractive index and extiction coefficient.

Fig.3.15 shows the normalized drain current versus time when the gate is excited by a 10μW light pulse of 4ns with V_G=0.6V for different Germanium carrier lifetimes ranging from 1μs to 1ps. The normalization was performed to properly compare the decays since the drain current amplitude depends on the carrier lifetime. The actual drain current without

normalization for various carrier lifetime is shown in the inset to compare the change in drain current as a function of carrier lifetime.

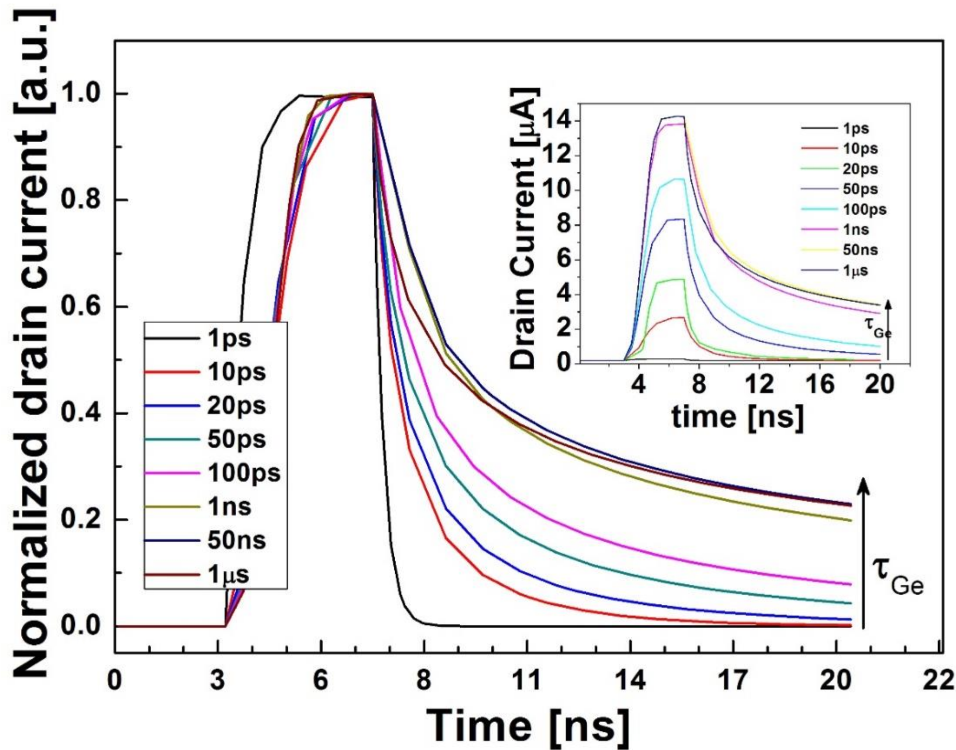


Figure 3.15 Transient response of OCFET with normalized drain current vs time as a funcion of carrier lifetime. Actual drain current vs time without normalization is shown in the inset.

As expected, we observed very fast rise time and much slower fall time for increasing Germanium carrier lifetime (rise and fall times are defined as the time interval between 10% and 90% of the signal swing). The fall time obtained by simulations is much larger than calculations. This is probably due to the effect of the potential near the oxide interface. When the input light is turned-off, the minority carriers in the germanium side must recombine to reduce the photovoltage present in the gate. This recombination lifetime correlates directly to the amount of photovoltage generated for a given amount of incidence light. Figure 3.16 shows the Ion/Ioff ratio, rise time and fall time of OCFET extracted from fig.3.15 against the time. The Ion/Ioff ratio and t_{fall} increases steadily and almost saturates when carrier lifetime increased beyond 10ns.

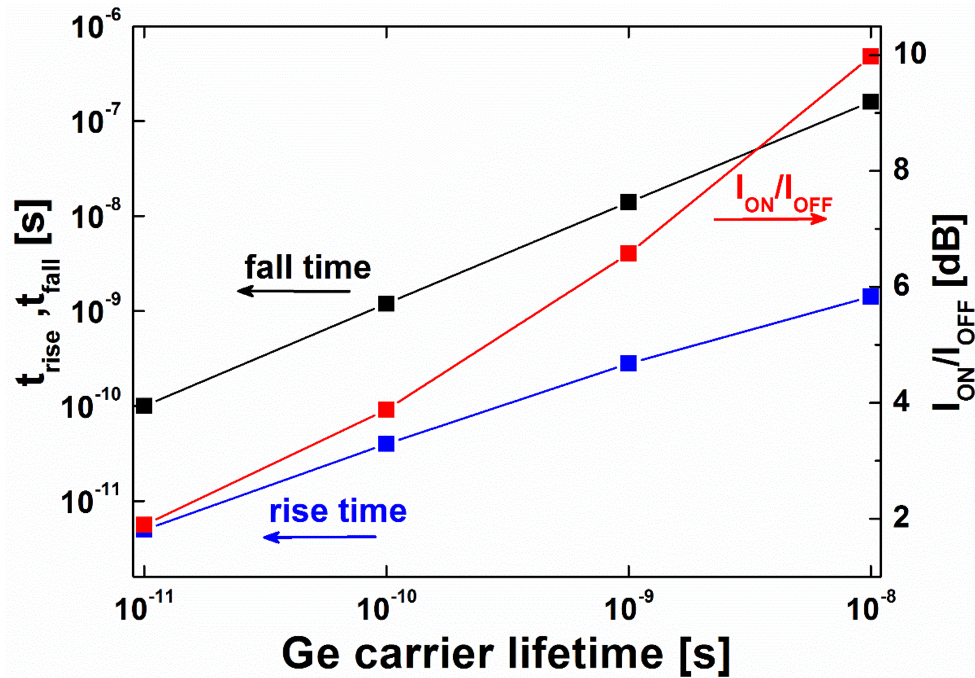


Figure 3.16 Ion/Ioff ratio, rise time(t_{rise}) and fall time (t_{fall}) extracted from the figure 3.15

In order to reduce the fall time it is necessary to act on the electric field distribution in the Germanium film. This can be accomplished tuning different parameters, mainly optical power, gate bias and Germanium doping.

3.4.3. Optical Power and Gate Voltage Dependence

Figure 3.17 shows the normalized drain current versus time with gate voltage V_G=0.6V and 100ps Ge carrier lifetime. The input optical power is between 1 μW and 100μW. Both rise time (t_{rise}) and fall time (t_{fall}) decreases with increase in optical power. This can be related to a larger photogeneration rate that induces higher injection thus reducing the carrier lifetimes and enhancing the OCFET speed (it is a possibility but we did not get evidence of this. Probably the observed decrease is related to a power dependent potential distribution). Nevertheless, the fall time is still too long even for 100 μW optical power.

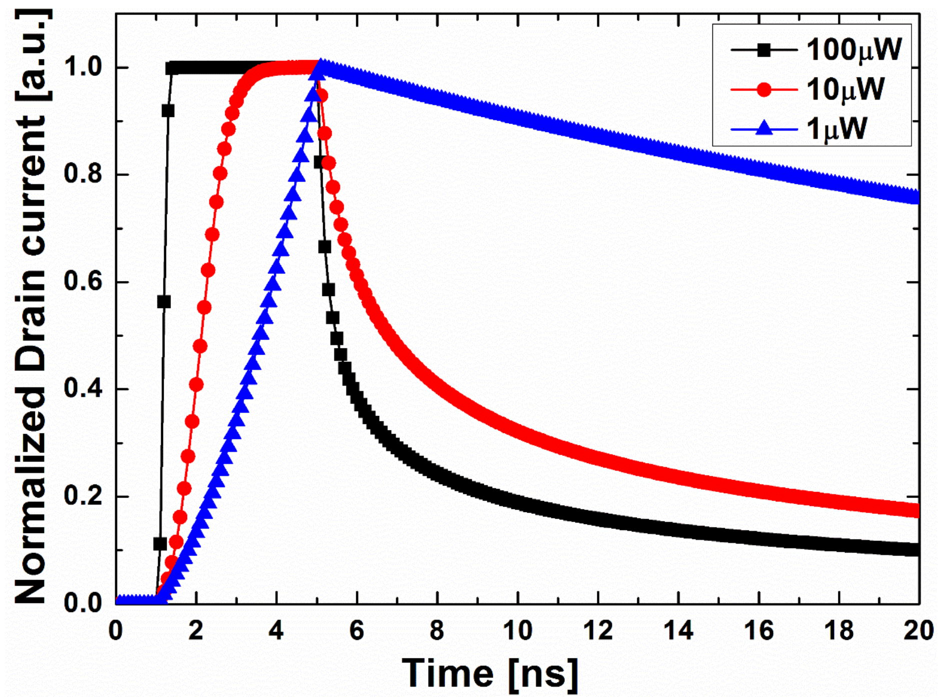


Figure 3.17 Normalized drain current vs time as a function of optical power from 1µW to 100 µW with constant gate voltage (V_G=0.6V).

Fig.3.18 shows the normalized drain current time response at different gate voltages with 100µW optical pulse power and 100ps Ge carrier lifetime. The improved device turn-off at lower gate bias is due to a lower electric field that allows photocarriers moving faster away from the oxide interface. However, the gate bias fixes the operating point and cannot be arbitrarily reduced further without changing the doping concentrations. The normalization is performed to study the change in fall time of the device, since the drain current varies with gate voltage similarly to figure 3.17.

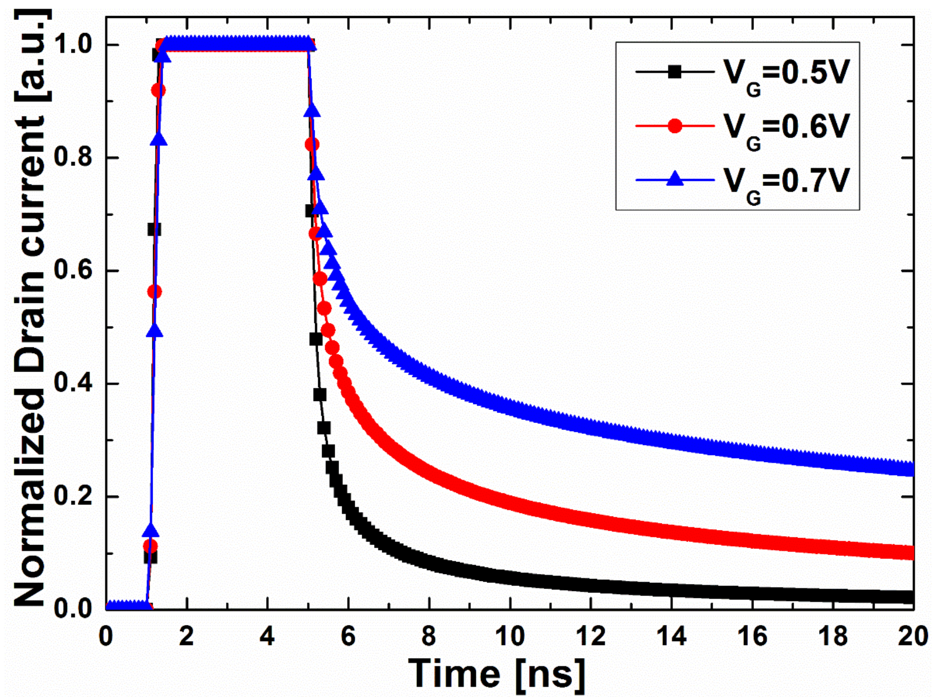


Figure 3.18 Transient response of OCFET with normalized drain current vs time as a function of gate voltage (V_G=0.5V, 0.6V and 0.7V). The optical power and carrier lifetime are kept constant at 100µW and 100ps, respectively.

3.4.4. Doping Dependence

Fig. 3.19 shows the normalized drain current time response at V_{DS}=0.5V, 100µW optical pulse power and 100ps Ge carrier lifetime at different symmetric Ge and Si doping concentrations. As the OCFET threshold voltage varies with Germanium and Silicon doping, V_G is optimized accordingly as shown in the figure legend. Since gate voltage and doping concentrations are varied simultaneously, normalization is necessary to observe the fall time. The actual pulse response without normalizing the drain current is shown in the inset.

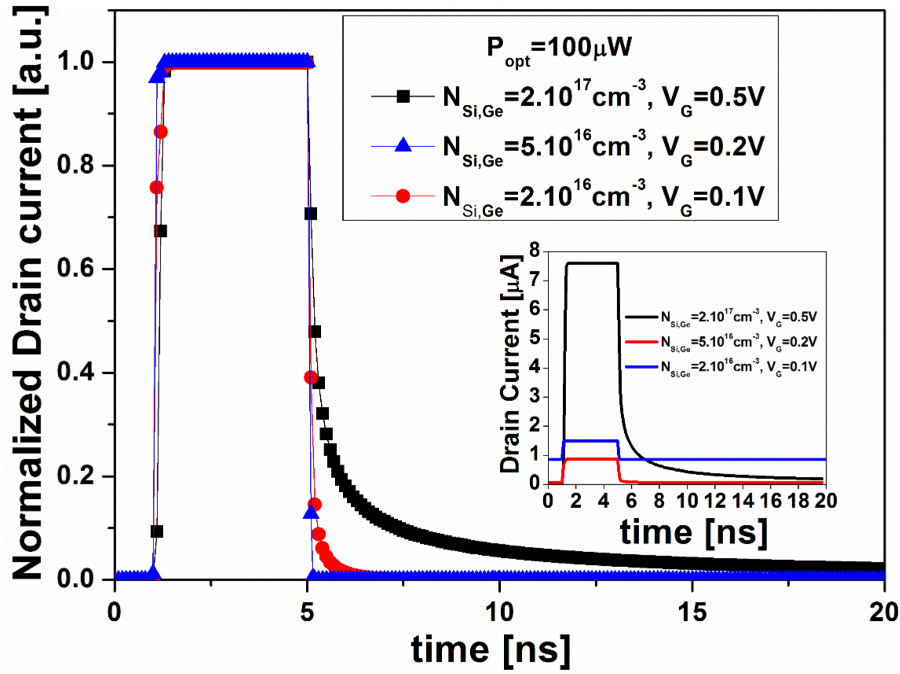


Figure 3.19 Normalized drain current vs time as a function of Silicon and Germanium doping concentrations. In the inset, actual drain current is shown vs time. The doping concentrations are varied between $10^{16}cm^{-3}$ and 10^{17} cm^{-3} along with the gate bias.

The device speed is improved with the fall time reduced below 100ps (now close to τ). Unfortunately, such improvement corresponds to a dramatic reduction in the Ion/Ioff ratio that become slightly larger than 2dB indicating an important trade-off between speed and sensitivity. In the proposed geometry, the device exhibits an intrinsic slow turn-off mechanism due to the electric insulation of the Ge gate. The accumulated photocarriers at the Ge-oxide interface must move away or recombine, with the presence of electric field distribution in order to turn-off the device.

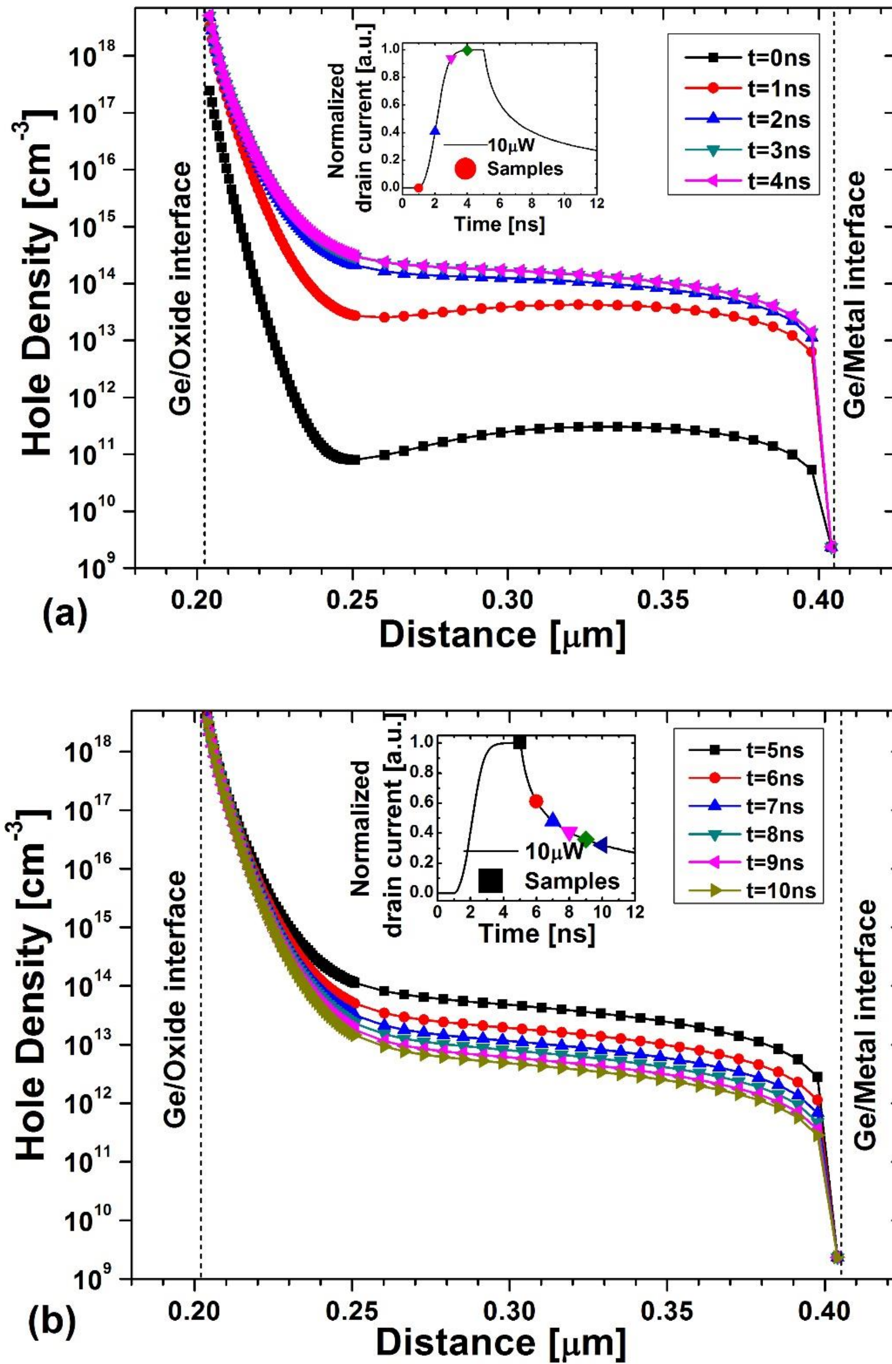


Figure 3.20 (a) Hole density in the Germanium layer during turn on pulse for 4ns and (b)Hole density during turn off. The samples are taken from 1ns-4ns for turn on and from 5ns to 10ns after the pulse is turned off.

The hole distribution along the Germanium film at different times during the transients is analyzed to understand this effect. Fig 3.20. (a) and (b) show the hole spatial distribution during the rise (turn-on) and fall (turn-off) edge respectively. The reference pulse and the

sampling times are reported in the inset. During the rise or turn-on, the transient charges rapidly accumulate at the oxide interface inducing the channel inversion in the Silicon channel and turning the device on. In this phase the electric field is directed towards the Ge-oxide interface promoting the photogenerated holes to move in the expected direction. When light is turned off, the accumulated holes must diffuse away from the oxide to restore the equilibrium.

However, even after the pulse is turned off, the electric field induced by the gate bias hinder the carrier diffusion by maintaining the accumulated carrier distribution along the Ge-oxide interface for a long time. In such condition the resulting fall time depends on the competition between diffusion and field-induced separation. This may be due to the presence of gate bias even after the light is turned off. This effect of the gate voltage on the electric field can be minimized by applying the gate voltage as a pulse only during the optical input.

3.4.5 Channel Length and Gate Thickness Dependence

As discussed in section 3.3.4, the scaling of the OCFET is performed at constant field with a scaling factor k. Scaling down the device not only increases the drain current, but improves the device speed too. As we shrink the channel length, the gate length shrinks too, decreasing the volume for absorption, thus reducing the total absorbed light. Even though the drain current increases with shrinking the channel length, the I_{on}/I_{off} ratio decreases compared to longer channel devices in contrary to its static characteristics. Figure 3.21 shows the normalized drain current against time as a function of channel length from 90nm to 350nm. It is evident that the rise time decreases (from 4ns for L=350nm to 1ns for L=90nm) with decreasing the channel length and the reduction in fall time is minimum. Meanwhile the Ion/Ioff ratio is reduced (around 50dB for L=350nm to 4dB for L=90nm) when channel length is reduced. The I_{on}/I_{off} ratio in dB calculated from the drain current is shown in the inset. This decrease in I_{on}/I_{off} ratio may be due to the faster recombination of photogenerated carriers before contributing to the channel modulation.

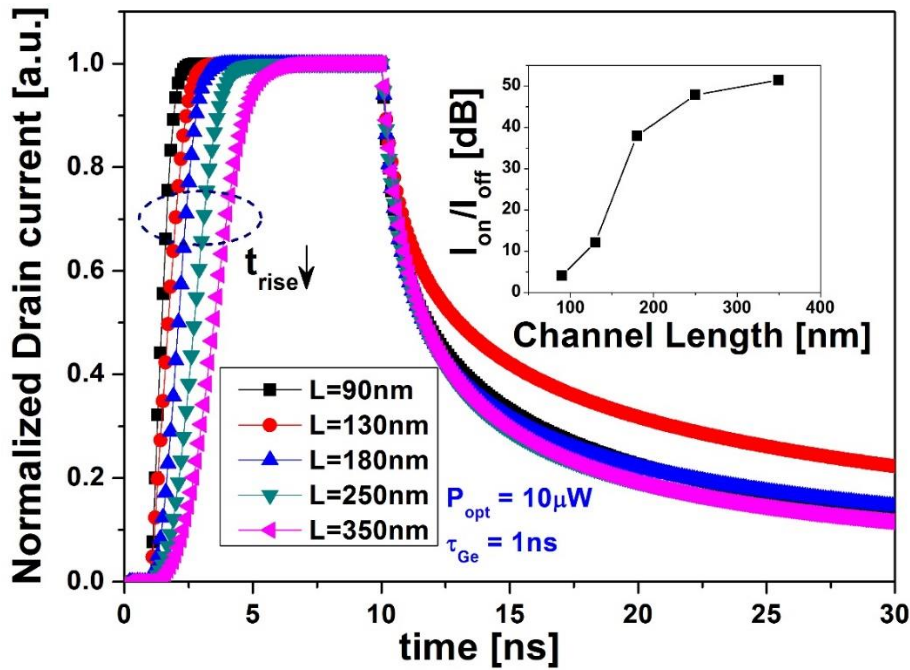


Figure 3.21 Normalized drain current vs time as a function of channel length, with optical power P_{opt}=10μW and carrier lifetime τ_{Ge} = 1ns.

Similarly, the device speed can be increased by reducing the Germanium absorption layer thickness, but accepting a reduced sensitivity (I_{on}/I_{off}). To increase the sensitivity a thick absorption layer is required to increase the photon absorption. However, a thick absorption layer would increase the response time because the photocarriers would require a longer transit time. Figure 3.22 shows the drain current time response, as a function of Ge layer thickness. The optical power P_{opt}=10 μW, the Ge carrier lifetime τ_{Ge}=1ns and the gate bias V_G=0.6V are kept constant. Ge layer thickness is varied from 50nm to 400nm. The increased sensitivity in thicker Ge layer can be attributed to increased photocurrent due to increased absorption but the device exhibits increased fall time due to slower removal of photoexcited carriers. The devices with thinner absorption layer have lower sensitivity due to the incomplete absorption of photons, but decrease in fall time due to faster removal of photoexcited carriers.

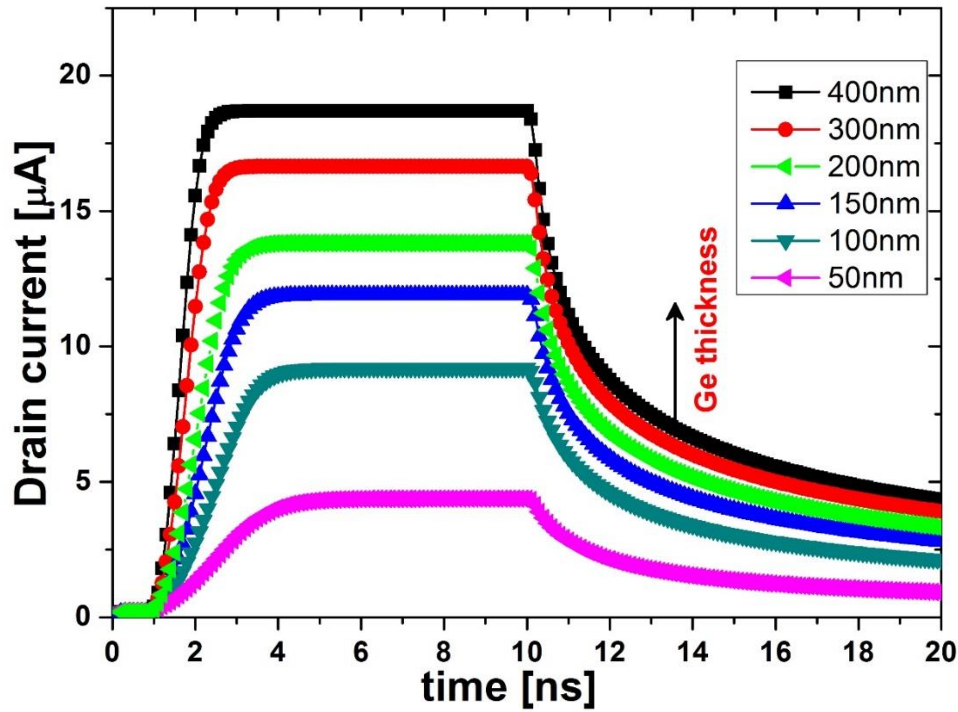


Figure 3.22 Drain current vs time, as a function of Germanium layer thickness, with optical input of 10μW, gate bias V_G=0.6V and Ge carrier lifetime of 1ns.

Figure 3.23 shows the extracted Ion/Ioff ratio and fall time from figure 3.22, as a function of the Ge layer thickness. The results demonstrate that devices with thinner absorption layer exhibit faster fall time but reduced sensitivity. The device with 50nm Ge layer provides Ion/Ioff ratio of 25 and fall time of 18ns. The longer fall time for this thinner Ge layer is due to the lower optical power of 10 μW and higher carrier lifetime of 1ns. The deivce with 400nm Ge layer shows an Ion/Ioff ratio of 40 but the fall time increases significantly up to 38ns. This performance can be improved only by using higher optical power, and the use of lower carrier lifetime or gate voltage will result in a severe trade-off with sensitivity.

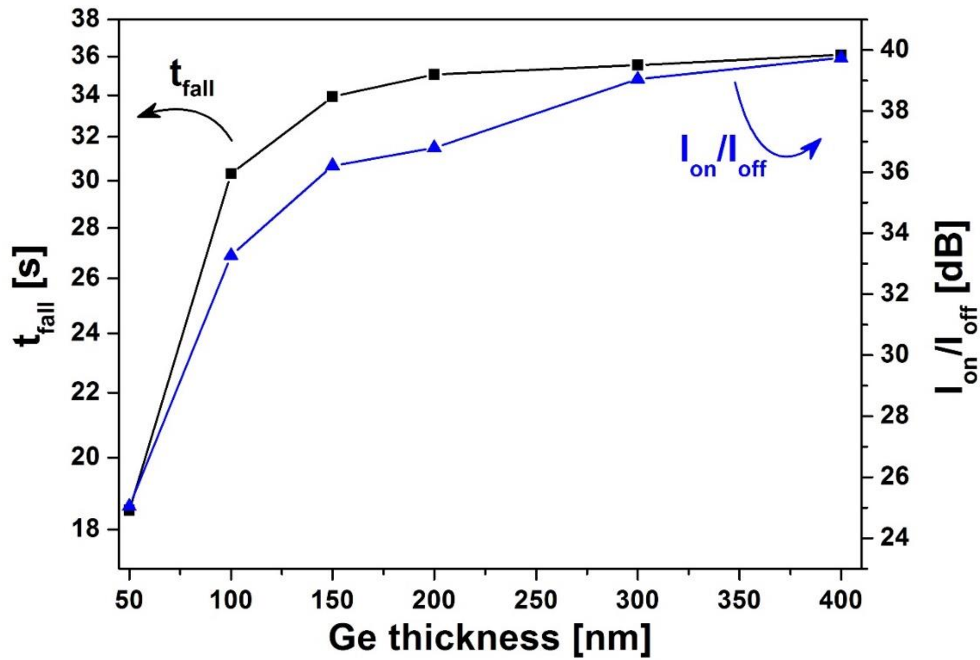


Figure 3.23 Ion/Ioff ratio and fall time of OCFET extracted from the transient response plot as a function of Ge thickness.

In this section, I have discussed the structure and the operation of the optically controlled FET (OCFET) and its DC and AC charateristics. The parameters like doping concentrations, gate bias, optical power, gate dimensions, and recombination mechanisms affecting the performance of the OCFET have been discussed. The turn-off mechanism can be controlled by carrier lifetimes and thickness of the gate region as well as the applied gate bias by keeping the trade-off in to account. Figure 3.24 shows the summary of the overall characteristics of the OCFET device under different combinations of device parameters. The trade-off is clearly visible as the empty area (upper left side of the graph) corresponding to short fall times and large Ion/Ioff ratios.

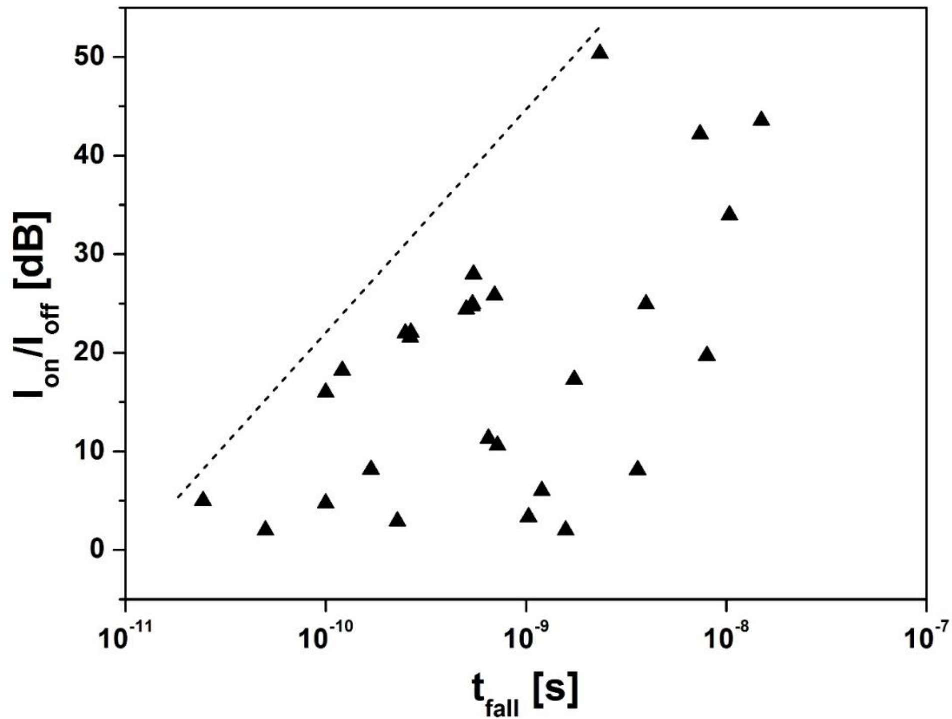


Figure 3.24 Ion/Ioff ratio and fall time of OCFET obtained using different combinations of device parameters.

The dashed line can be crossed only if larger optical power is used. When the device is properly optimized, the device speed is limited by the Ge carrier lifetime. Even if τ smaller then 100ps are realistic, simulations show that the sensitivity will be severely affected. Since we have shown that the slow device turn-off is determined by the amplitude and direction of the electric field, we believe that different device structures should be tailored for a more efficient photogenerated carrier removal. The trade-off between sensitivity and bandwidth should be choosen according to the application. With the help of the simulated results, possible parameters for fast and high responsivity device are given in table 3.2.

Parameters	Sensitivity	Bandwidth
Ge thickness [nm]	300	100
Tox [nm]	4	4
Doping Concentrations [cm^{-3}]	10^{17}-10^{18}	10^{16}
Channel length [nm]	>250	≤180
Ge carrier lifetime [s]	>1ns	<1ns

Table 3.2. Suggested device parameters for high responsivity and higher bandwidth OCFET.

3.5 OCFET Inverters

MOS interters are the fundamental building blocks of digital circuits. The inverter is the most fundamental logic gate that performs a Boolean operation on a single input variable. The inverter operation is such that, for a low input voltage level the output voltage V_{out} is equal to a high value V_{OH} (output high voltage). In this case, the nMOS (driver) device is in Cut-off and hence conducts no current. The use of n-channel MOSFETs as drivers can be justified by the greater mobility of electrons, thus exhibiting low channel resistance. An enhancement mode device ensures direct coupling to next stage without a coupling capacitor. In this section, we discuss the use of n-channel enhancement mode OCFET as a driver transistor for different inverter designs, namely resistor load, saturated nmos load and complementary nMOS configurations.

As discussed in previous sections, the DC and transient characteristics of an OCFET depends on optical power, doping concentrations and Ge layer thickness. The inverter characteristics are studied while varying such parameters of the loads (load resistor values, W/L ratio of the load transistor in saturated load inverter and W/L ratio of p-channel OCFET in CMOS configuration). Transfer characteristics and transient response (fall time, rise time) are analyzed with various combinations of these parameters.

3.5.1 Inverters with Resistive Load

The inverter with a resistive load is the basic configuration, which are not used in traditional integrated circuits, because the resistors requires a too large area on the chip and introduce large RC time constants. Resistive load inverters are simulated here in order to analyze OCFET as a driver. The basic inverter circuit consists of an OCFET switching device designed to force V_{OH} to V_{OL} and a resistor load element to "pull" the output up toward the power supply V_{DD}. I have modeled the inverter with an OCFET (W=1µm and L=0.18 µm) as driver and a 100KΩ load resistor fed by 1V voltage source (V_{DD}) and the input voltage (V_{in}) varied from 0V to 1V. Figure 3.25 shows the voltage transfer characteristics of a basic n-OCFET inverter with a load resistor with the optical input varied from dark to 10µW. The circuit diagram is shown in the inset.

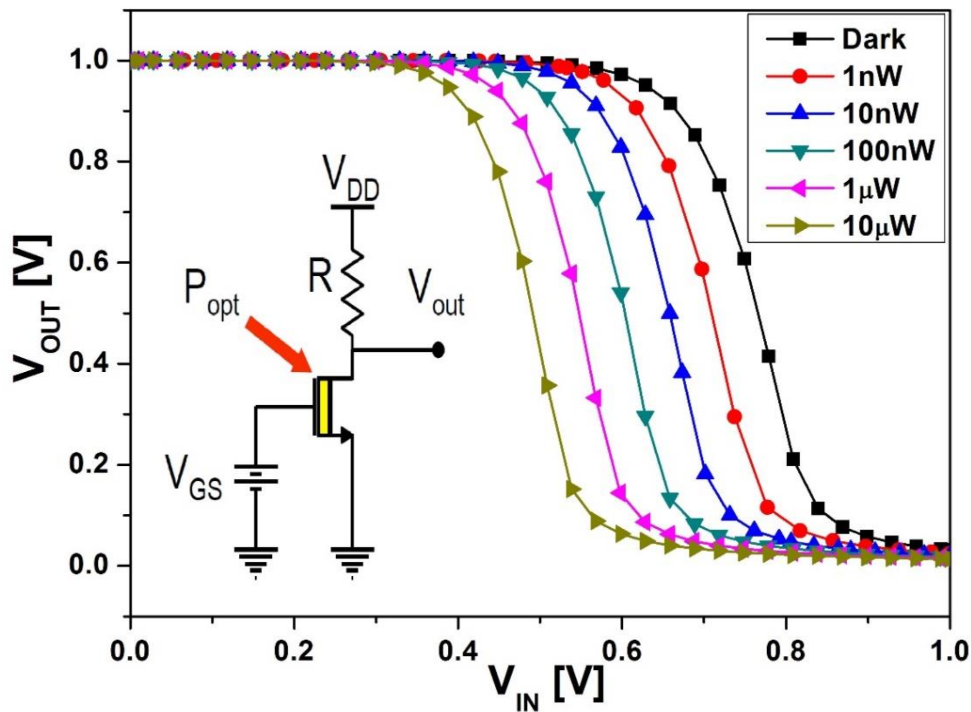


Figure 3.25 Voltage transfer characteristics of a resistive load inverter with dark to 10µW optical power and 100KΩ load resistor.

The operation of the inverter is similar to a conventional nMOS inverter, so the output voltage V_{out} can be written as,

$$V_{out} = V_{DS} = V_{DD} - I_D R_L \tag{3.8}$$

When there is no input optical power, the OCFET is in off state with I_D=0, the output V_O=V_{DD} and the output reaches V_{OL} with an applied optical power. The voltage transfer characteristics of the inverter shows a change in threshold voltage, similar to the OCFET device characteristics when the optical power is increased. From the figure, the threshold voltage in dark condition is around 0.72V and it is reduced to around 0.49V when the optical power is 10μW. The shape of the VTC can be further controlled by changing the load resistance. Figure 3.26 shows the dependence of the voltage transfer characteristics on K_nR_L. Since we use a single OCFET as driver, only the value of the load resistance is changed with K_n as constant.

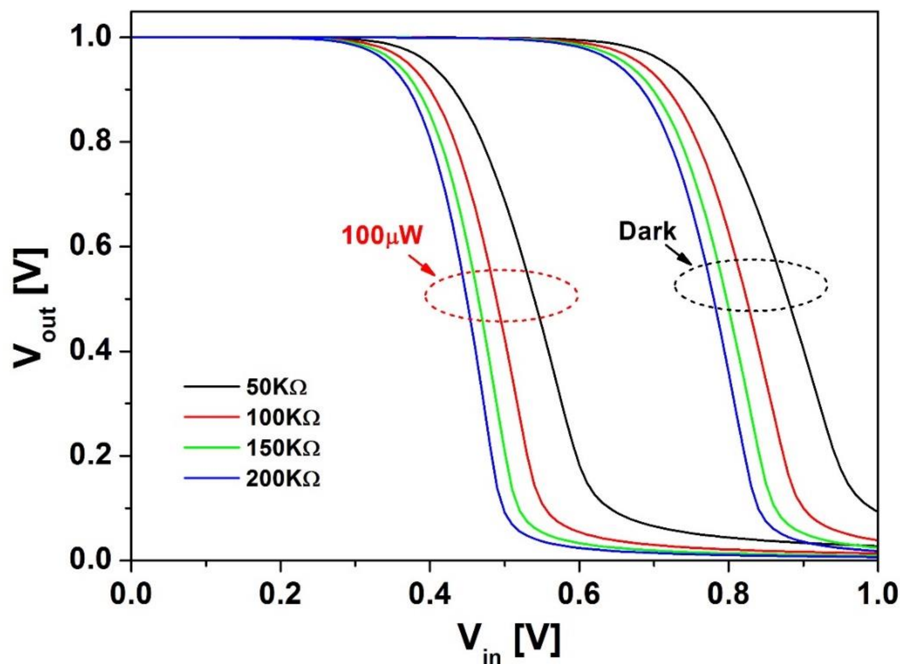


Figure 3.26 K_nR_L dependence of inverter static characteristics for. Load resistance varied from 50KΩ to 200KΩ in dark and 100μW optical power.

The term K_nR_L ($K_n = \mu_n C_{ox}\, W/L$) plays an important role in determining the shape of the voltage transfer characteristics. It appears as a critical parameter for V_{OL}, V_{IL} and V_{IH}. Primarily the supply voltage (V_{DD}) determines V_{OH} and the gate bias determines the dark current. The adjustment of the low output voltage (V_{OL}) receives primary attention than V_{IH} and V_{IL} and an increase in K_nR_L reduces the V_{OL} with larger transition slope. It is known that increasing the W/L ratio of the driver or decreasing the load resistor increases the power

consumption significantly. The W/L ratio can be reduced and load resistance can be increased only if the power consumption is the main concern. On the other hand the load resistance can be decreased if the area consumption is the main concern.

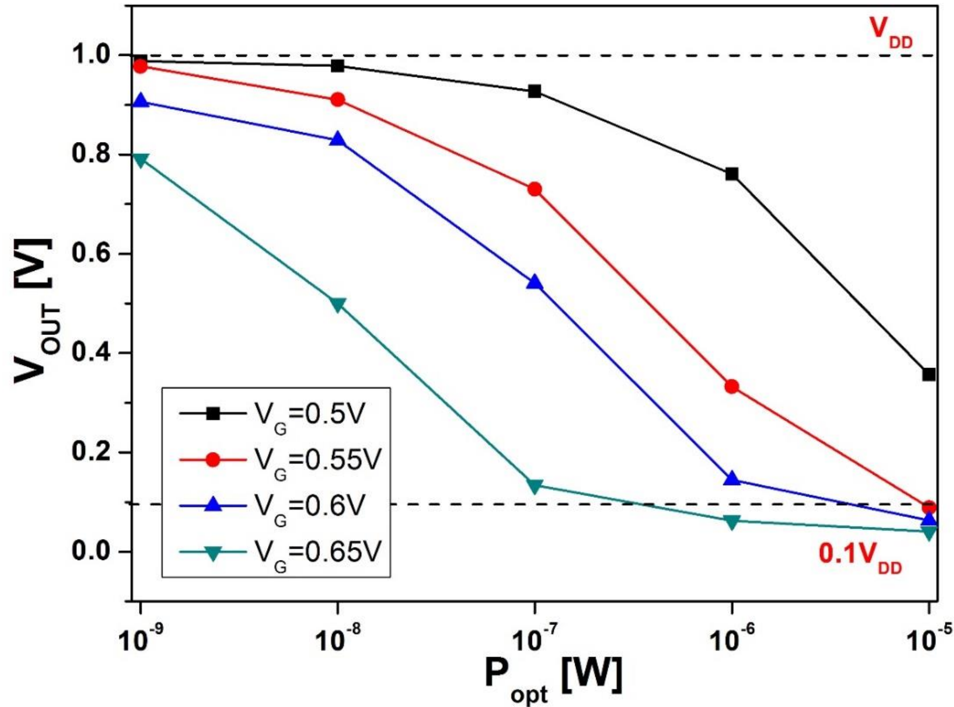


Figure 3.27 Inverter output voltage (V_{out}) vs optical power (upto 10µW) at differrent input voltage (V_{in}).

Figure 3.27 shows the output voltage (V_{out}) versus optical power at various input voltage (V_{in} or V_{GS}). In a digital circuit, the output “LOW” should be the lowest possible (0 V) and the output “HIGH” level the highest (i.e. the supply voltage V_{DD}). The former cannot be achieved using a resistive load inverter, the latter cannot be obtained since the dark current cannot be neglected due to the gate bias near the threshold. Therefore, we evaluated the inverter characteristics for an output signal swing between 10% and 90% of the supply. In such conditions, this inverter provides an optimal dynamic range from HIGH to LOW state for V_{GS} = 0.6 V and V_{GS} = 0.65 V with an optical signal of 1 µW and 10 µW.

Besides the static response, speed is an important figure in logic devices. The transient response of the inverter is studied with different optical power, load resistance and Germanium carrier lifetime. Figure 3.28 shows the transient response of a resistive load

inverter with load resistance values 50KΩ, 100 KΩ and 200 KΩ and input optical power of 10μW, V_{GS}= 0.6V and a Ge carrier lifetime of 100ps.

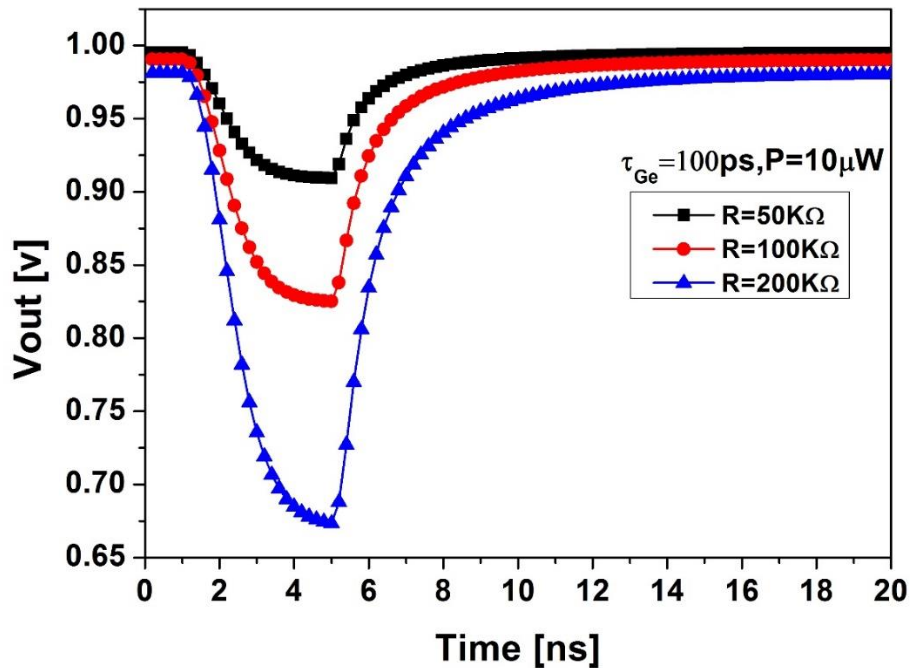


Figure 3.28 Transient response of resistive load inverter with different load resistors (50KΩ, 100 KΩ and 200 KΩ) for a 4ns optical pulse of 10 μW.

The figure shows the actual output of the inverter without normalization. The inverter with a lower load resistance exhibits poor noise margin with 1.8ns to reach from 90% to 10% of Vout (t_{fall}) and 2.8ns to reach 90% of the total output voltage (t_{rise}). It is clear that by increasing the load resistance, we can increase the output swing of the inverter but with a small increase in fall time (around 200 ps). The increase in rise time is around 100ps for 100kΩ load but it dramatically increases to around 10ns for a 200kΩ load.

In order to decrease the rise time (t_{rise}) and increase the output swing, we need to resort to higher optical power and lower Ge carrier lifetime. Figure 3.29 shows the transient response of the inverter with 100kΩ load resistor and Ge carrier lifetime of 10ps and 100ps at 100 μW optical power.

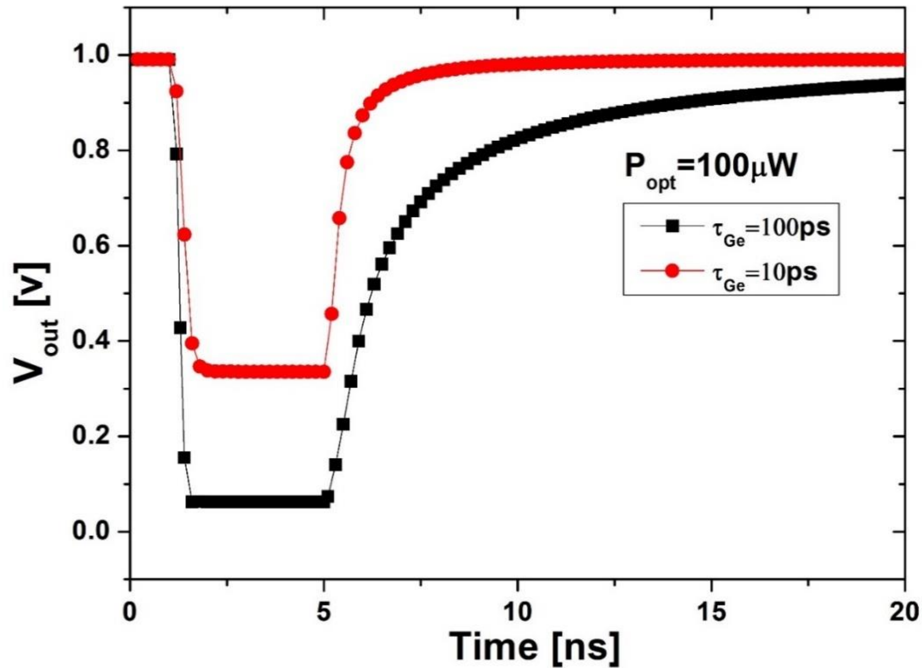


Figure 3.29 Vout vs time of resistive load inverter as a function of Germanium carrier lifetime with optical power of 100μW.

Larger optical powers provide better result with respect to larger load resistance, but shorter Ge carrier lifetime decreases the output swing of the inverter. This trade-off is due to the intrisic time delay of the OCFET associated to the transistor cut-off frequency and RC time constant of the Germanium layer.

The nOCFET inverter with a resistive load has been simulated to introduce the concepts associated with static logic gate design. Although a simple discrete component logic gate could be built using this circuit, integrated circuit realizations do not use resistive loads because the resistor would take up far too much area. The solution to this problem is to replace the load resistor with a transistor.

3.5.2 Inverters with Enhancement Load

When we replace the load resistor with a transistor, we are replacing the two terminal resistor with a four-terminal MOSFET, and we must decide where to connect the extra terminals. Current in the NMOS transistor goes from drain to source, so these terminals are connected to the same terminals where the resistor was removed. However, there are a number of possibilities for the gate terminal like connected to its drain terminal (saturated load) or connected to a separate power supply (linear load). When the transistor is forced to operate in saturation region, the drain current I_D is given by,

$$I_D = \frac{K_n'}{2}\left(\frac{W}{L}\right)_L (V_{GS} - V_{TNL})^2 \qquad (3.9)$$

Unfortunately, the use of the saturated load device has a detrimental effect on other characteristics of the logic gate. The value of V_{OH} will no longer be equal to V_{DD}. In order to understand this effect, it is helpful to imagine a capacitive load attached to the logic gate, at the output. Consider the inverter with no optical input (dark), so that OCFET is turned off. Now, load device charges capacitor until the current through the load becomes zero, which occurs when $V_{GS} = V_{TN}$. Thus, for the NMOS saturated load inverter, the output voltage reaches a maximum value equal to one threshold voltage drop below the supply voltage V_{DD}.

In this study we have used an enhancement mode nMOSFET operating in saturation region (V_{GS}=V_{DS}). The builtin MOSFET spice model is used as load in order to reduce the simulation time and since it is quite easier to modify the WidthXLength ratio. The Spice model parameters are changed as close as possible to the OCFET in order to vary only the W/L ratio of the MOSFET. Figure 3.30 shows the voltage transfer characteristics of a n-OCFET inverter with an enhancement mode diode connected mosfet as load transistor with different W/L ratios. The circuit is shown in the inset. The dimension (W/L ratio) of the load transistor is modified in order to change K_D/K_L ratio from 2.75 to 5.5 with the W/L ratio of the switching transistor (OCFET) being 5.55.

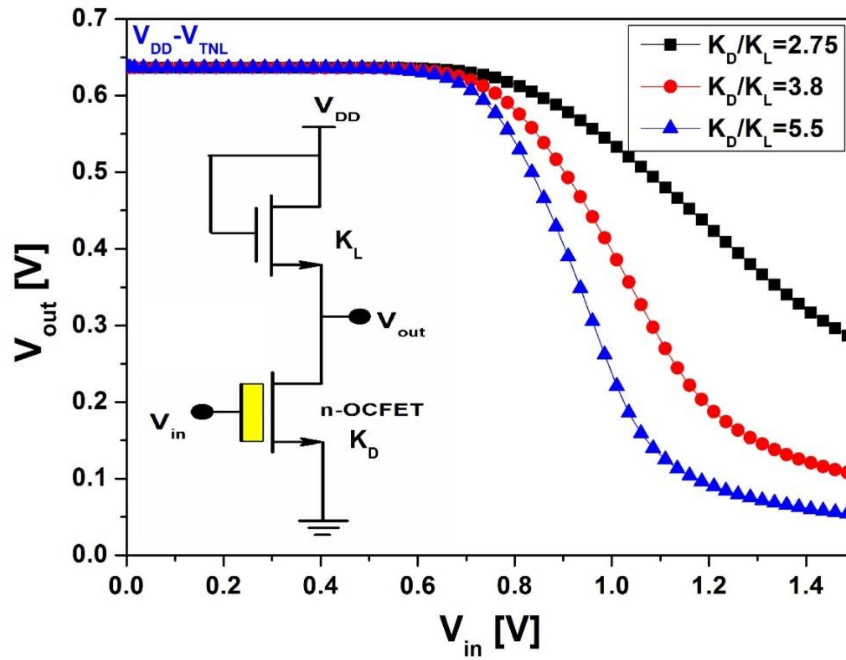


Figure 3.30 Static characteristics of a n-OCFET inverter with an enhancement mode, diode connected mosfet load with W/L ranging from 2.5 to 5.

The threshold voltage of the load MOSFET is chosen to be 0.8V, therefore the possible V_{OH} will be V_{DD}-V_{TNL}. In this case, with a V_{DD} of 1.5V, the output V_{OH} is around 0.65V. A small reduction in the output is noticed, which is due to the body effect of the load transistor. As the W/L ratio of the load decreases (K_D/K_L increases), the effective resistance increases and the V_{OL} of the inverter reduces with a larger transition slope similar to the resistive load inverter. For further studies, we used a K_D/K_L ratio of 5.5. Figure 3.31 shows the voltage transfer characteristics of n-OCFET inverter with $(W/L)_{driver}$ =5.55 and optical power varying from dark condition to 10μW. The change in the inverter threshold voltage can be attributed to the intrinsic OCFET characteristics, when additional gate voltage is generated with optical input. In comparison with the resistive load inverter, the V_{OH} is reduced by the threshold voltage of the load mosfet (V_{TNL}), whereas the output low V_{OL} is very similar because of the identical OCFET used.

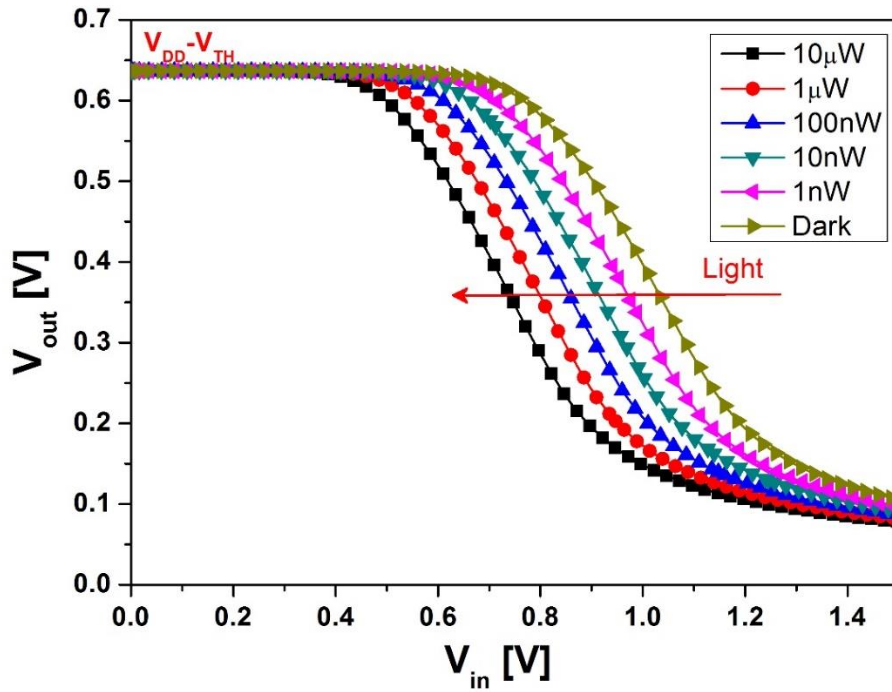


Figure 3.31 Voltage transfer characteristics of an active load inverter with (K_D/K_L) ratio of 5 at optical power upto 10µW and V_{DD}=V_{in}=1.5V.

The transient response of the inverter is studied while varying W/L ratio of the load, Ge carrier lifetime and input voltage (V_{GSD}). Figure 3.32 shows the transfer characteristics of an active load nOCFET inverter as a function of the input voltage of the OCFET. The optical power and the Ge carrier lifetime are kept constant at 10 µW and 1ns respectively. The gate voltage is varied from 0.55V to 0.65V. The inverter exhibits an increased output swing as well as the rise time (t_{rise}). The output V_{OH} is constant for all the input values, which apparently depends on V_{DD}. Instead, the V_{OL} decreases from 0.35V (for V_{GS}=0.55V) to 0.1V (for V_{GS}=0.65V) with an increase in V_{GS} or V_{IN}. The fall time (from High to Low) does not vary significantly, much like the resistive load inverter. However, the rise time (Low to High) increases from around 13ns (for V_{GS}=0.55V) to well above 20ns (for V_{GS}=0.65V). This characteristics is due to the intrinsic delay of the OCFET as discussed in the device characteristics section.

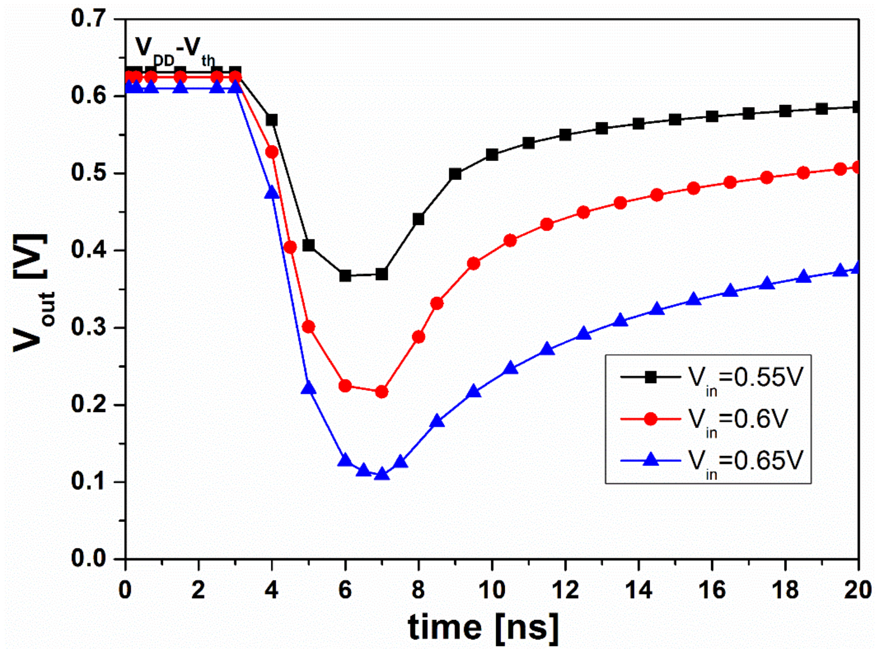


Figure 3.32 Transfer characteristics of an active load inverter for a 4ns optical pulse of 10µW as a function of V_{in} or V_{GS} (0.55V, 0.6V and 0.65V). The Ge carrier lifetime was kept constant at 1ns with V_{DD}=1.5V.

The change of other parameters like Ge carrier lifetime and K_R (K_D/K_L ratio) produces similar characteristics as the resistive load inverter (not shown). When the Ge carrier lifetime is reduced to 100ps and less, there was an apparent reduction of several ns in rise time (Low-High), but with a trade-off reduction in V_{OL}. This is due to the dependence of rise time solely on the carrier lifetime, but the output swing depends on both carrier lifetime and aspect ratio. This can be also attributed to the intrinsic limitations observed in OCFET device characteristics.

3.5.3 Complementary OCFET Inverters

Another important configuration designed to study the OCFET based inverters is the complementary inverter with p- and n-channel OCFETs. The main advantage of a CMOS inverter over many other solutions is that it is built exclusively out of transistors operating as switches, without any other passive elements. In this study both p- and n-channel OCFETs are enhancement mode devices. In the static response, optical input is applied simultaneously to both transistors with an offset gate bias. Voltage transfer characteristics depends on n-OCFET turing ON rather than the turn OFF of p-OCFET.

From Figure 3.33 (a) note that the pOCFET (pull-up transistor) is connected between V_{DD} and the output node, V_{OUT}, whereas the nOCFET (pull-down transistor) is connected between the output node, V_{OUT}, and the ground, GND. The circuit configuration (a) and Vdrain-Idrain characteristics (b) of p-OCFET and n-OCFET are shown in figure 3.33. It was observed that n-OCFET and p-OCFET comprise I_{off} =140nA and 2nA respectively.

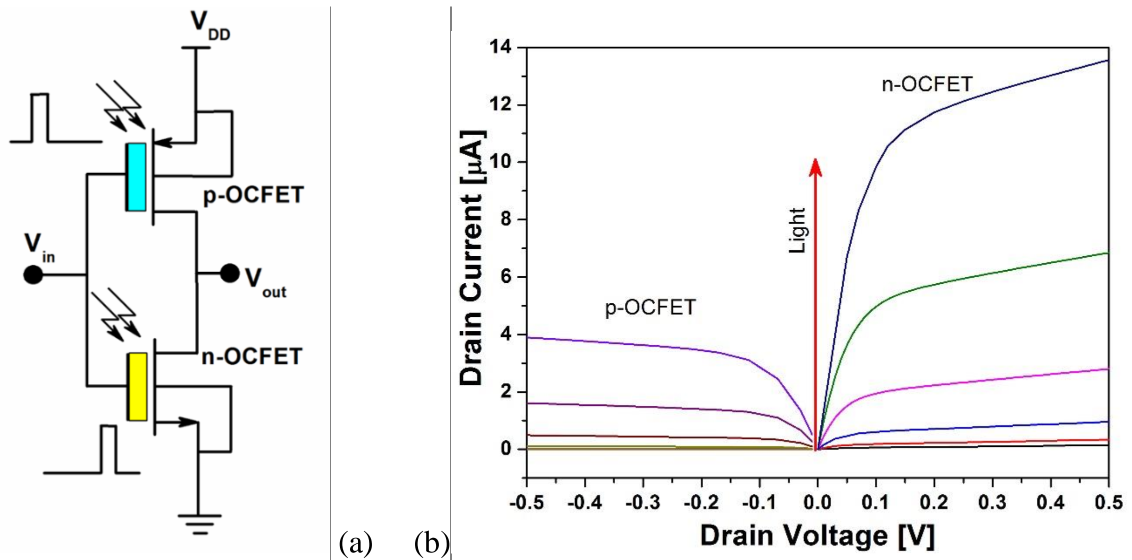


Figure 3.33. (a) Circuit schematic of p-OCFET and n-OCFET connected in CMOS configuration and current voltage characteristics of both transistors. The optical input was varied up to 1mW for p-OCFET and 10μW for n-OCFET.

The input voltage is applied to bias the inverter just below the threshold voltage. The optical input acts as the switching input of the inverter. Under dark conditions, with input voltage less than V_{THn} the nOCFET transistor is not conducting, whereas the pull-up pOCFET transistor is switched on and connects the output mode to V_{DD}. For large values of the input voltage, V_{IN}, the pull-down nMOS transistor is switched on and connects the output to GND = 0V. Figure 3.34 shows the voltage transfer characteristics of a complementary inverter with V_{DD} = 1V and optical input ranging from dark to 100μW. The channel length of both devices are similar and only the channel width is modified to change the P/N aspect ratio.

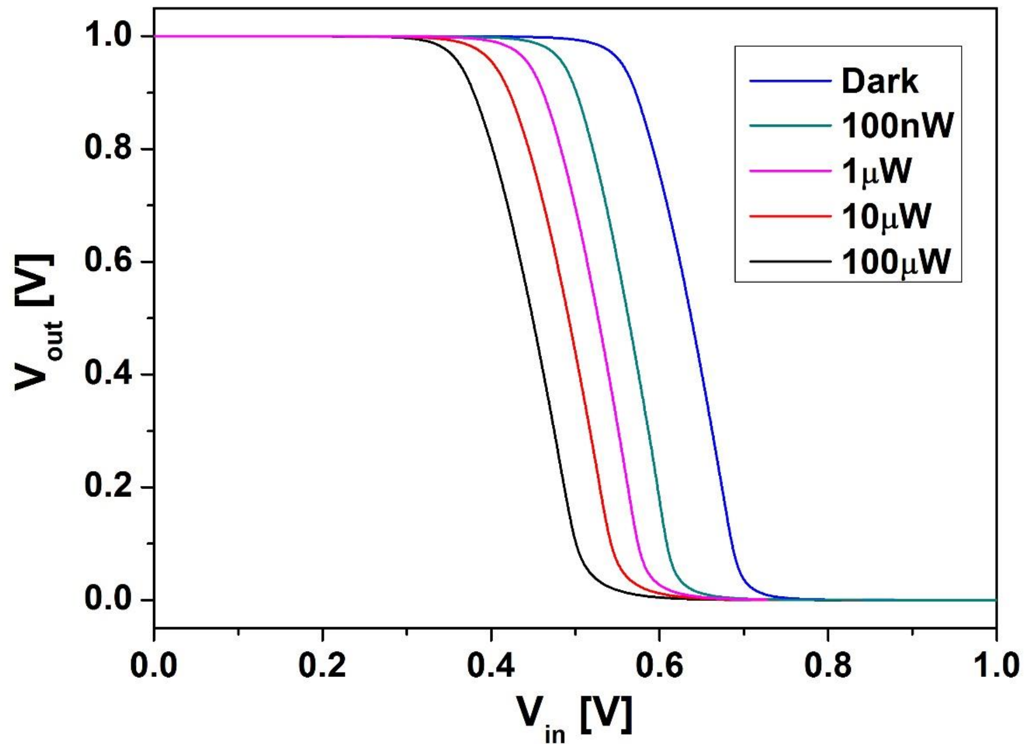


Figure 3.34 Static characteristics of a complementary OCFET inverter as a function of optical power (dark to 100µW) of 1.55µm wavelength and V_{DD}=1V.

Under dark conditions, with the input voltage swept to 1V, the n-OCFET turns ON at V_{THn} (0.7V) and V_{OUT} is pulled down to zero. When the inverter is irradiated with light (100nW to 100µW) the threshold voltage of the inverter decreases with the increase of the optical power due to the increased gate voltage (by photovoltage). The output voltage V_{OH} = V_{DD} and V_{OL} is almost zero with an optical input when n-OCFET is ON.

The temporal response of this inverter configuration is simulated by supplying short optical pulses alternatively to each OCFET. When an optical pulse is applied to p-OCFET, it is turned-on and charges the load capacitor and when the n-OCFET is turned on by a short pulse, the output switches from high to low. As the photoexcited carriers are removed (when n-OCFET is OFF and p-OCFET is ON) the pair recovers to initial state, charging C_L back to V_{DD}. Figure 3.35 shows the normalized output of the inverter depending on the input optical power, with constant Ge carrier lifetime for both transistors.

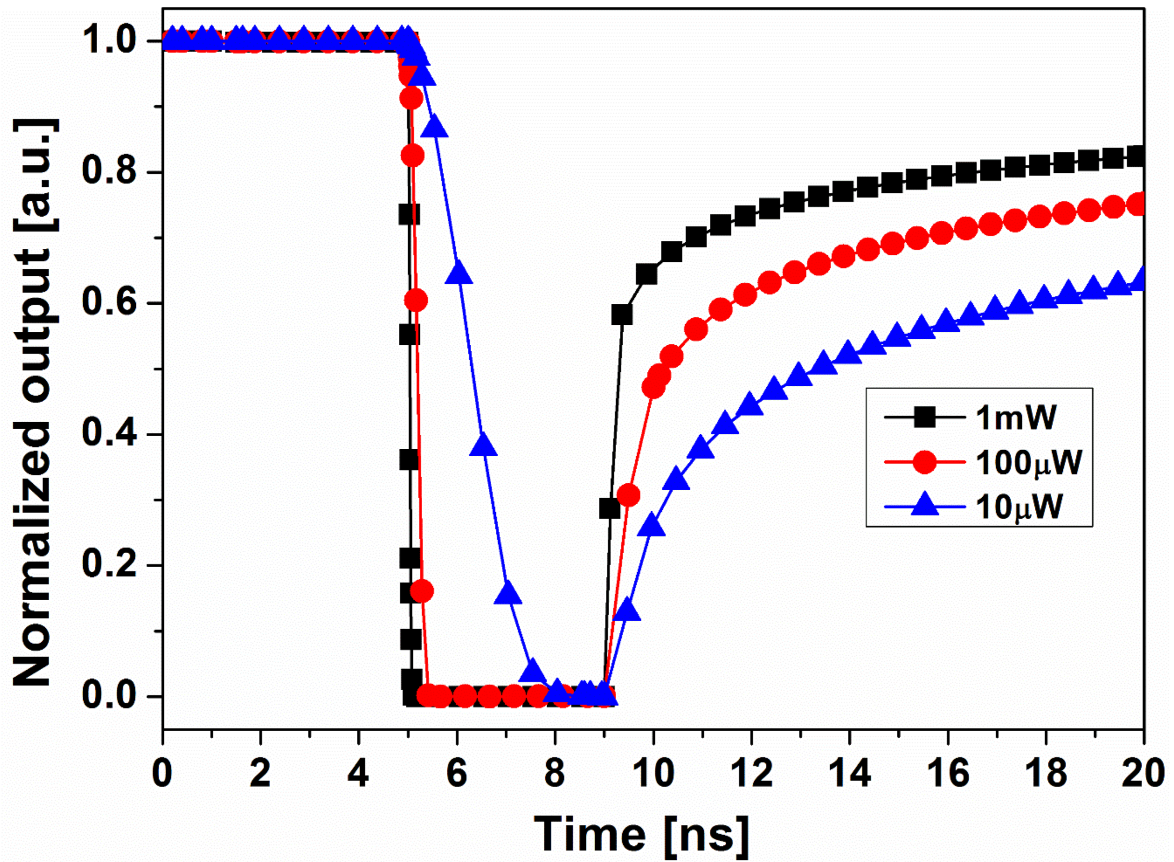


Figure 3.35 Normalized temporal response of a complementary OCFET inverter depending on the 4ns optical pulse of power 10μW to 1mW with Ge carrier lifetime of 1ns.

The normalization is necessary to understand the variation in the rise time (Low to High) due to the change in output swing of the inverter with the carrier lifetime. The decrease in fall time and rise time can be attributed to the larger photogeneration rate that induce higher injection thus reducing the carrier lifetime. The rise time decreases from greater than 30ns for 10μW optical power to around 18ns for 1mW. Nonetheless, still high risetime can be attributed to the Ge carrier lifetime of 1ns and the offset gate bias, a device characteristics explained in previous sections (optical power and gate voltage dependence).

Another way to decrease the rise time is to reduce the offset gate bias and Ge carrier lifetime with increased optical power. Figure 3.36 shows the transfer characteristics of the inverter with optical power of 10μW to 1mW and Ge carrier lifetime of 1ns. The normalized output voltage is shown in the inset to compare the rise time of the inverter.

The offset gate voltage is varied from 0.5V to 0.6V and V_{DD}=2V. The output swing of the inverter with 0.6V offset bias and 100 μW optical power is higher (from V_{DD} to 1.75V) than

the offset volatge of 0.5V (from V_{DD} to around 1.96V). But the rise time of the inverter with 0.5V offset and 100 μW power is 1ns, whereas the rise time for 0.6V offset is around than 10ns.

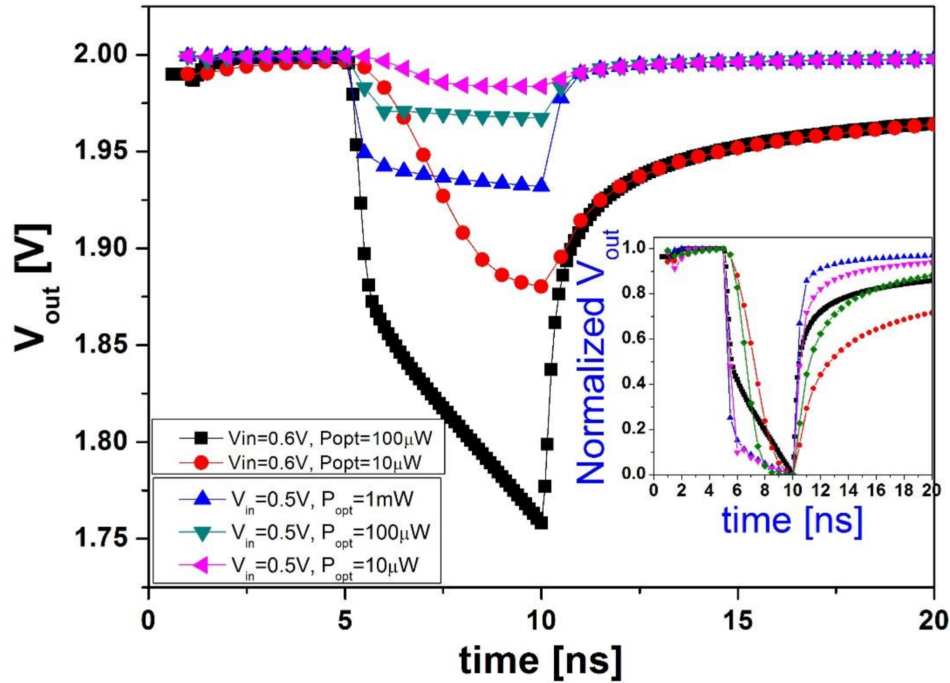


Figure 3.36 Temporal response of a complimentary OCFET inverter as a function of input gate voltage with Ge carrier lifetime of 1ns and 10μW to 1mW optical power of wavelength 1.55μm.

With increasing the offset gate bias, an increase in output swing was observed, with a trade-off in the inverter rise time. It is understood from these simulations, that the device limitations affects the inverter performance. The output swing can be further increased by increasing the gate voltage, with increasing rise time. This may be due to the continuous presence of gate bias even after the optical pulse is turned off. One possible solution for this is to cut-off the gate bias when the optical input is zero.

To summarize the study of inverter characteristics, figure 3.37 shows the rise time vs the output swing (Vmax/Vmin) of all the inverter configurations. The lowest rise time achieved was around 400ps but with very low output swing of 0.02dB. With the highest output swing of 30dB, the rise time was around 40ns. The characteristics of all these inverter

configurations are affected by intrinsic OCFET device limitations. The OCFET time response is expected to be limited by three factors: the transistor cutoff frequency f_T, the drift in the Ge layer and the RC time constant of the Ge layer. The carrier transport by drift within the 200 nm thick Ge gate introduces transit times on the order of few ps assuming carriers at the saturation speed ($v_{sat} = 6\times10^6$ cm^{-3}). The RC time constant is mainly due to the Ge capacitance, which should be relevant during the device turn off when the accumulated positive charge in Ge has to move away from the interface or recombine. The inverter risetime should therefore depend on the Ge minority carrier lifetime. With the clear tradeoff between the speed and sensitivity of the device as well as the circuits, a proper set of parameters should be chosen to satisfy the application need as shown in the table 3.2.

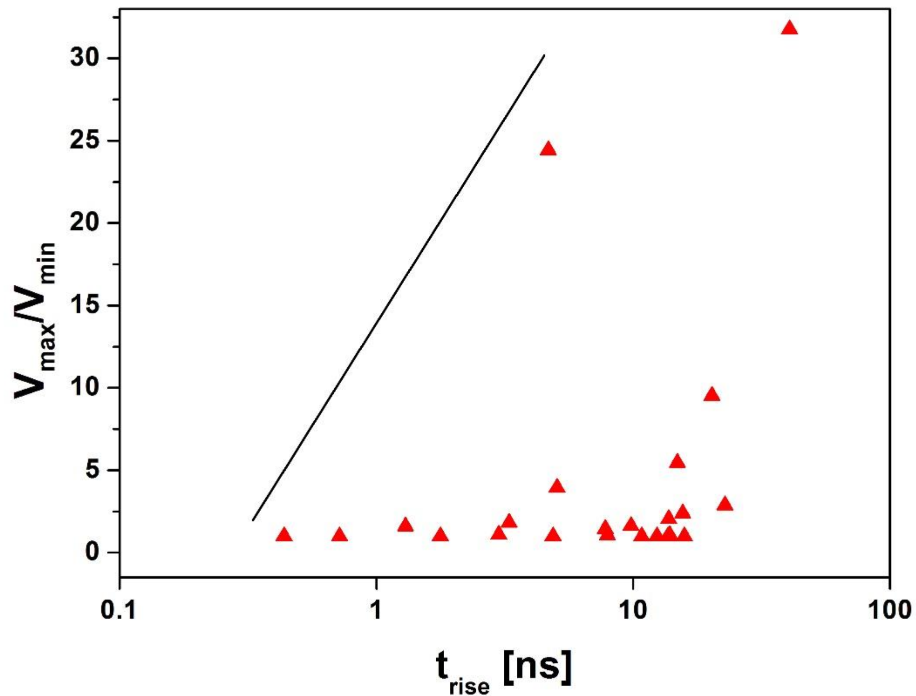


Figure 3.36 Output swing (Vmax/Vmin) vs the rise time of inverters of all configurations showing the tradeoff between speed and sensitivity of the circuits mainly due to the device limitations.

4

OCFET Proof of Concept

The operating principle of the Optically Controlled FET is similar to a traditional MOSFET, with a photo-absorbing gate. The goal was to fabricate a conventional MOSFET collaborating with an industrial lab. The MOSFET will have a source and drain with metal contacts, but without a gate contact, exposing the gate oxide. A poly-crystalline Ge absorbing layer that is used in our lab for NIR photodetectors will be deposited on the gate oxide. Due to some technical issues, at the time of this writing, the collaborators were able to provide only a "Trench MOSFET", in which the Ge layer cannot be grown directly on the gate. In order to evaluate the concept of the optically controlled FET, I resort to fabricate a separate Ge-on-Si photodiode to be connected to the trench-MOSFET's gate. The photovoltage from the photodiode is used to modulate the MOSFET channel. In this chapter I discus the fabrication and characterization of Germanium on Silicon photodiode and a metal gate MOSFET and demonstrate the OCFET proof of concept with the external photodiode connected to the MOSFET gate.

4.1. Germanium on Silicon Photodiodes

The Ge-on-Si photodiodes are fabricated on <100> n-type Silicon substrate with 1-3Ω resistivity. The Si wafer is cleaved into small samples and subsequently cleaned to remove any contamination on the surface. At first, a simple degreasing is done by cleaning the samples with Acetone and isopropanol, rinsed with deionized (DI) water and dried. A complete RCA cleaning [96] is done following the initial degreasing. In the Standard Clean [SC1], the samples are cleaned with a 5:1:1 mixture of NH_4OH : H_2O_2 : H_2O at 75°C typically for 15 minutes. The base-peroxide mixture removes organic residues by oxidative

breakdown and dissolution. The ammonium hydroxide dissolves and removes metals like, -gold, silver, copper, nickel, cadmium, zinc, cobalt, and chromium by complexing. The thin oxide layer formed by the SC1 process is removed by dipping the samples in diluted HF:H_2O solution at room temperature before subjecting them to SC2 process. In the SC2 treatment, the samples are dipped in 6:1:1 mixture of H_2O:H_2O_2:HCL at 75°C typically for 15 minutes. This step removes alkali ions, and cations such as Al^{+3}, Fe^{+3} and Mg^{+2} that form insoluble hydroxides in NH_4OH solutions. This second step also removes metallic contaminations that were not entirely removed by the SC1 treatment. It also prevents the electrochemical displacement replating of heavy metals in the solution by forming soluble complexes with the dissolved metal ions [97].

As the exposed Silicon surface easily forms native oxide film after RCA cleaning, it is important to remove the oxide layer before deposition and passivate the Silicon surface. The etching and H^+ passivation of Si surface is done by wet chemical etching of the surface by buffered oxide etchant (NH_4F and HF mixture). This hydrogen-passivated surface is chemically stable and resists oxidation allowing the specimen handling before deposition [98].

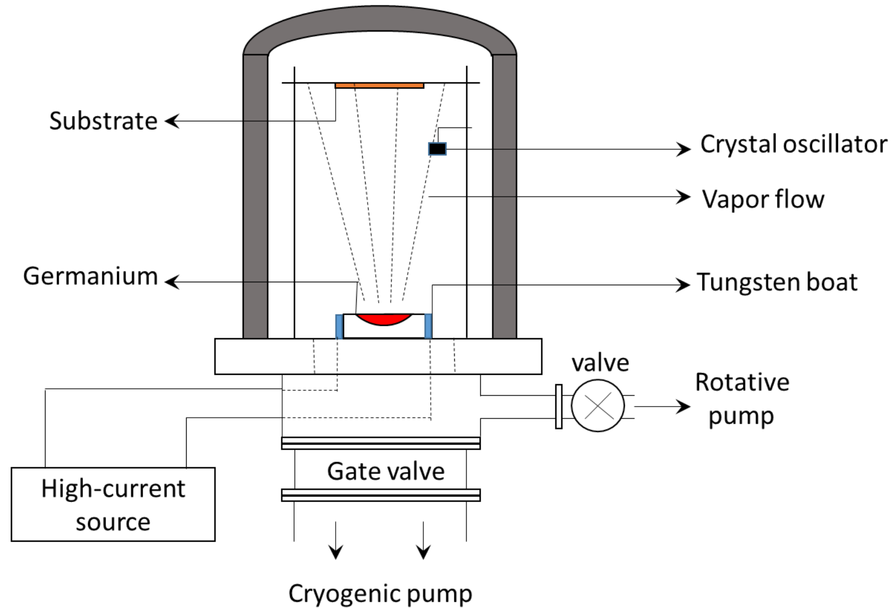


Figure 4.1 Schematic of a thermal evaporation system

The deposition of Germanium film is carried out by thermal evaporation following the method proposed by Colace et.al [99-104] in a vacuum chamber with a background pressure

of 10^{-8} Torr and about 10^{-7} Torr during deposition. The thermal evaporation system is shown in fig. 4.1. The material source was high purity (99.999%) Germanium grains in a tungsten boat fed by a low voltage, high current power supply controlled by a variac. The Germanium melts at 938°C and evaporates when the current reaches about 50A. During evaporation the vacuum is maintained at about 10^{-7} Torr. The film growth is controlled by a quartz crystal sensor that uses the resonance of a vibrating crystal of piezoelectric material (quartz) to create an electrical signal with a precise frequency. During evaporation the material deposits on the crystal, varying the crystal oscillation frequency thus providing information about the growth rate and film thickness.

Other important parameters affecting the deposition process are the substrate temperature T_s and the deposition rate D_r (Å/s). Both parameters strongly affect the crystal structure [97]. The Germanium films are amorphous in structure when deposited below 225°C, mono-crystalline between 225°C and 400°C and poly-crystalline structure above 450°C [105]. The Substrate temperature was monitored by a control system heating the substrate holder via the Joule effect, and a constant temperature was maintained by a temperature controller feedback with a thermocouple. The system allowed to heat the substrate up to 500 C with a ±1°C accuracy. The Germanium film of various thickness are deposited for this study (50nm, 350nm, 500nm and 600nm) at a substrate temperature of 300°C and a growth rate of 2 Å/s.

After depositing germanium film on silicon substrate, the device patterns are transferred on the samples using optical lithography. The photo masks were written on a 4-inch Iron Oxide on glass photoplates produced by Towne Technologies Inc. The Iron Oxide is semi-transparent to visible light while completely opaque to UV, facilitating the alignment operations. The device geometry consists of square mesas of six different areas, ranging from 60x60 μm^2 to 220x220 μm^2 in planar geometry. The top contacts are provided with a wide window to allow normal incidence illumination. The device geometry are schematically shown in figure 4.2.

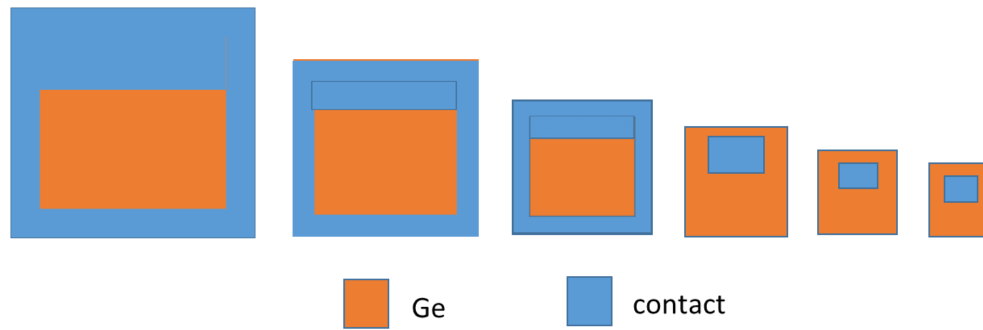


Figure 4.2. The photodiode geometry. The area of the Ge mesa varies between 60x60 μm^2 to 220x220 μm^2

The samples are coated with a positive photoresist Megaposit SPR220 at 4000 rpm for 40 seconds and then pre-baked at 120°C for 90 seconds. The pattern transfer from the mask to the sample is done by using a Karl Suss MA6 Mask aligner, a top and bottom side contact printer used for lithography down to 1μm or better. The MA6 uses a Hg-source filtered to UV-wavelength of 365 nm, with typical exposure intensity of 25 mW/cm^2. The samples are aligned and exposed for 20 seconds and developed using NaOH based developer for 40 seconds.

Then the samples are post baked for 90 seconds at 120°C. The Germanium mesas are realized by etching the samples in a solution of H_3PO_4:H_2O_2:H_2O. After etching the samples are rinsed in DI water and the photoresist are removed using Acetone. The samples are then coated with a positive photoresist AZ 5214 at 3000 rpm for 50 seconds and pre-baking is done for 210s at 90°C. This photoresist is capable of image reversal, resulting in a negative pattern of the mask for lift-off process. The image reversal capability is obtained by a special crosslinking agent in the composition; it becomes active above a threshold temperature around 110°C only in the exposed areas of the resist. The crosslinking agent together with an exposed photoactive compound lead to a nearly insoluble (in developer) and light insensitive film, while the unexposed areas behave as a normal unexposed positive photoresist. After pre-baking the samples, the mesas and the contact pattern are aligned, and exposed for only 2s. The samples are then baked at 120°C for 90 seconds for image reversal. Then the samples are exposed for 20 seconds without masks. The contact pattern is then developed with the standard positive developer AZ 400 K.

The contact metal layer consists of Cr and Au deposited by thermal evaporation at ambient temperature in a vacuum atmosphere between 10^{-6} and 10^{-7} Torr, with a growth rate of 2 Å/s for both the metals. The final contact layer thickness is 100nm with 50 nm of Cr and 50 nm of Au. The lift-off is done by using Acetone alone or with Acetone in ultra-sonic bath in some cases till the photoresist is completely removed. Figure 4.3 (a) shows the schematic of a final device and (b) the image of the fabricated photodetectors. The cathode (on Si) is common to all devices while the anode (on Ge mesa) consists of a square frame, with one side wider than the others to allow electrical probing.

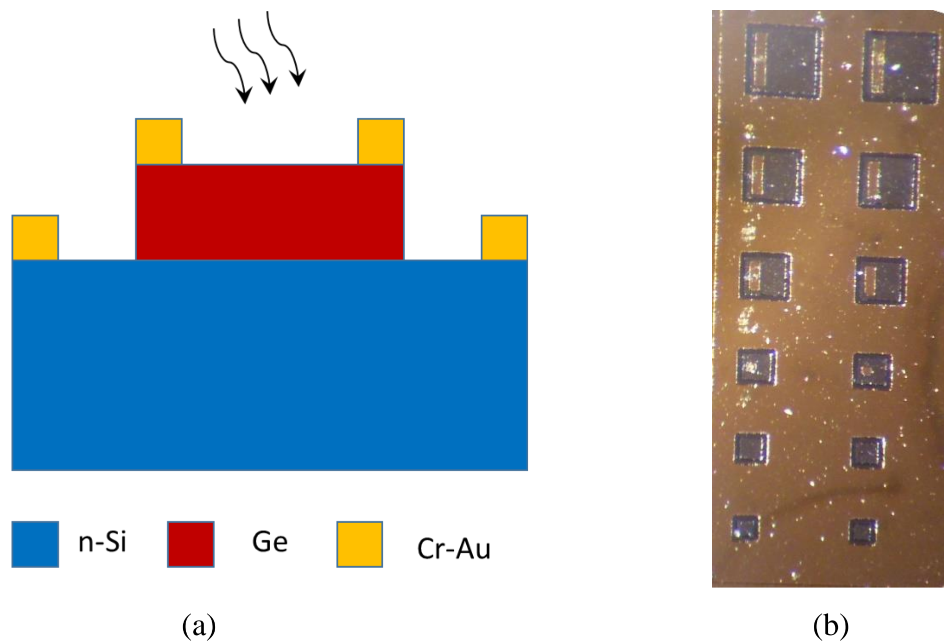


Figure 4.3 (a) Schematic representation of Ge on Si photodiode and (b) Image of fabricated photodiodes.

4.1.1 Device Characterization

The electronic and optical properties of the fabricated Ge-on-Si photodetectors were investigated. In this section, the main figures of merit for photodetectors like the dark current density, the responsivity and the dynamic properties are studied. In this device the p-Ge (Ge, although not doped intentionally, is high p doped due to defects) and n-Si forms a p-N heterojunction due to the difference in their bandgap. The band profiles depend on the electron affinities χ, the energy band gaps E_g and the work functions ϕ of the two materials

[106]. When different semiconductors are brought together to form a junction, we expect discontinuities in the energy bands as the Fermi levels line up at the interface in equilibrium. The discontinuities in the conduction band (ΔE_C) and the valence band (ΔE_V) accommodate the difference in band gap between the two semiconductors ΔE_g. In an ideal condition,

$$\Delta E_C = q(\chi_2 - \chi_1) \; and \; \Delta E_V = \Delta E_g - \Delta E_C \tag{4.1}$$

According to the above equation, most of the band offset occurs in the valence band while conduction band are almost aligned. Even if such Anderson's model fails to predict actual band offsets for semiconductor heterojunctions due to the strain and dislocation energies at the interface, it works relatively well in Ge/Si relaxed structures.

4.1.2. Current-Voltage Characteristics

The current-voltage characteristic of a photodiode with no incident light is similar to a rectifying diode. When the photodiode is forward biased, there is an exponential increase in the current. When a reverse bias is applied, a small reverse saturation current appears. It is related to the dark current as:

$$I_D = I_{SAT}\left(e^{\frac{qV_A}{K_B T}} - 1\right) \tag{4.2}$$

where I_D is the photodiode dark current, I_{SAT} is the reverse saturation current, q is the electron charge, V_A is the applied bias voltage, k_B=1.38 x 10^{-23} JK^{-1}, is the Boltzmann Constant and T is the absolute temperature (273 K). The optical radiation, shifts the I-V curve by the amount of photocurrent (I_{Ph}),

$$I_{TOTAL} = I_{SAT}\left(e^{\frac{qV_A}{K_B T}} - 1\right) - I_{ph} \tag{4.3}$$

The current-voltage measurement set-up consists of an automatic acquisition system composed by a voltage source and picoammeter (Hewlett-Packard HP4140B) controlled by a computer under LabView environment. By means of internal switches, it is possible to activate the voltage across the device and monitor the current while sweeping the bias. I used a GSG (ground-signal-ground) micro-probe to make contact with the device terminated by

an SMA connector. From the current-voltage characteristics, it is possible to extract important parameters of the photodetectors like, dark current, series and shunt resistances.

The dark current is crucial as it affects the sensitivity in terms of SNR (signal to noise ratio) and NEP (noise equivalent power). The most important noise source in photodectors is the shot-noise from currents flow. Since the photodetectors work in reverse bias, the shot noise depends on the sum of photocurrent and dark currents,

$$\langle i_s^2 \rangle = 2q\Delta\nu \left(i_d + i_{ph} \right) \tag{4.4}$$

Where $\langle i_s^2 \rangle$ is the shot-noise mean value, q is the electron charge, Δν is the bandwidth, Iph and Id are the photocurrent and dark current respectively. It is important to keep the dark current low in order to increase the sensitivity.

The dark current density of Ge-on-Si photodiodes of different Ge mesa area (60μmx60μm to 220μmx220μm) are shown in figure 4.4 (a). The Germanium layer thickness is 600nm. The devices exhibit typical dark current densities in the range 2-3.7 $mAcm^{-2}$ at 1V reverse bias which is comparable to best reported values for the similar devices [107].

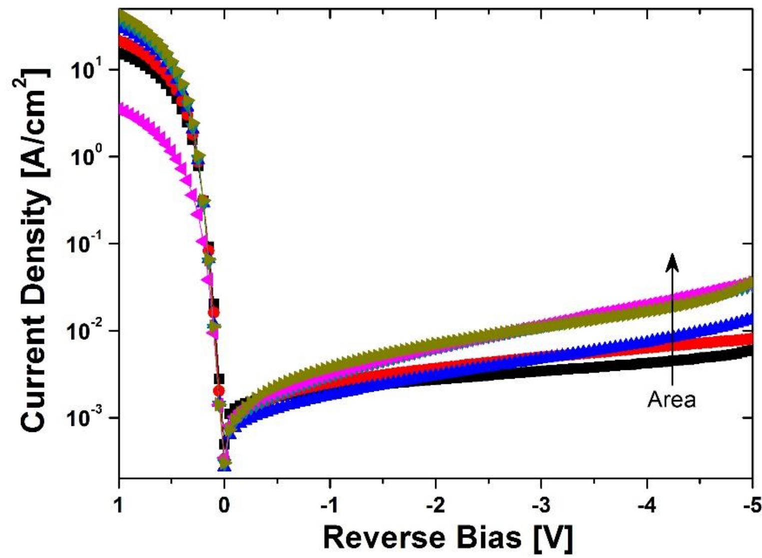


Figure 4.4 (a). Dark current density of Ge-on-Si photodiodes as a function of Germanium mesa area with a thickness of 600nm.

The dark current mainly depends on the threading dislocation density at Ge/Si interface and in Ge layer. The concentration of threading dislocations associated to the lattice mismatch depends on a number of processing conditions like Ge layer thickness and annealing conditions.

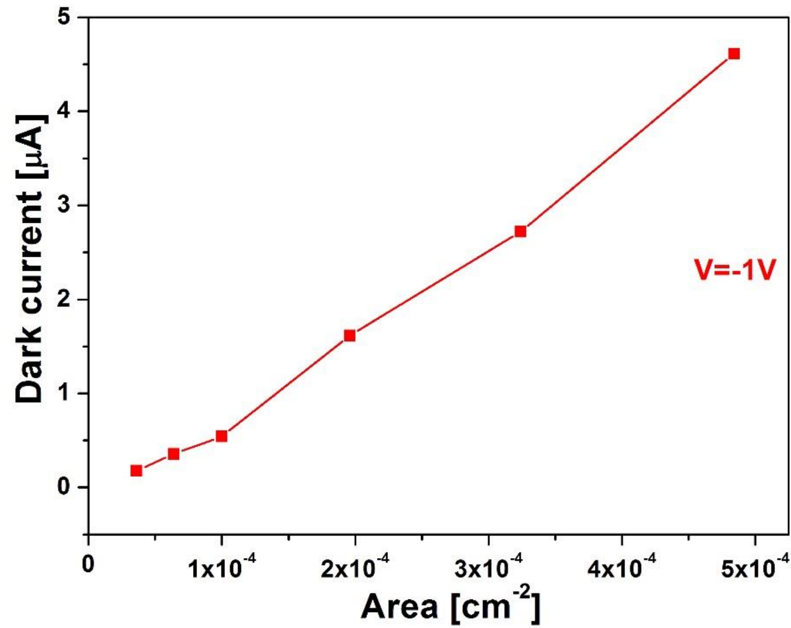


Figure 4.4 (b) Experimental values of dark current at -1V as a function of Germanium mesa area. The Ge layer thickness was 600nm.

Figure 4.4 (b) shows the linear scaling of dark current at 1 V reverse bias as a function of device area, mainly due to the generation of minority carriers in the depletion region of the device [108].

Figure 4.5 shows the dark current density of Ge-on-Si photodiodes of 220μmx220μm Germanium mesa with layer thickness of 600nm and 350nm. The dark current density of a photodiode with 350nm thick Ge layer exhibits 0.7mA/cm^2 whereas it increases to 3.7mA/cm^2 for 600nm thick Ge layer. We note that the dark current density increases as the Ge absorption layer thickness increases from 0.35μm to 0.6μm. The dark current is originated in both the depletion layer and the neutral layer of the Ge side. Due to the high unintentional Ge doping, the thickness of the depletion layer is few nanometers, however it contains most of the dislocations. The neutral region is wider but TDD progressively

reduces. Considering the generation processes assisted by deep levels related to threading dislocations, a direct a correlation between dark current densities and threading dislocations was demonstrated [109].

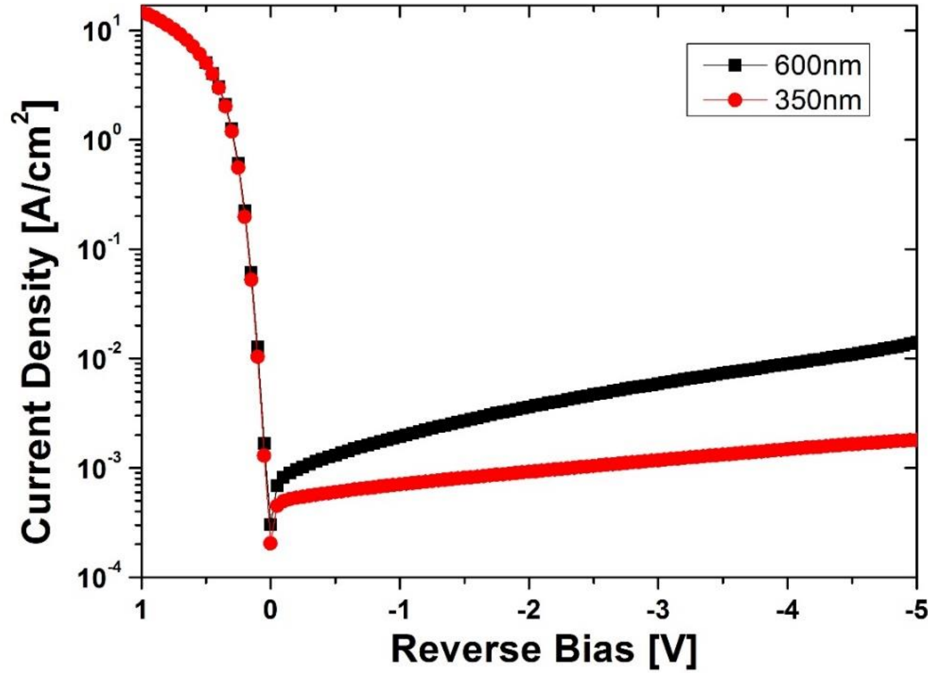


Figure 4.5. Current density versus reverse bias of a Ge-on-Si photodiode with an area 220μmx220μm as a function of Germanium layer thickness.

4.1.3. Series Resistance

The series resistance is the resistance of the semiconductor material and depends on the physical dimensions, junction area and resistivity of the material. The series resistance affects the forward biased I-V characteristics and the transient response of the p-n diodes. In this device, the resistance depends on two material regions, the Si substrate volume, the Germanium mesa and the Silicon area linking the Ge mesa with the contacts. In both cases, the series resistance is an inverse function of the Ge mesa size. The series resistance of Ge-on-Si diodes are extracted by fitting a section of the I-V characteristics of the device with the following equation:

$$V = R_s I_f + \eta V_T ln\left(\frac{I_f}{I_0}\right) \tag{4.5}$$

where R_s is the series resistance, η is the ideality factor, and V_T is the thermal voltage (25mV at room temperature). Figure 4.6 shows the inverse relation between the series resistance and the area of the Ge mesa with a thickness of 350nm. The series resistance value ranges from 90Ω of larger area device to 400Ω for smaller area devices.

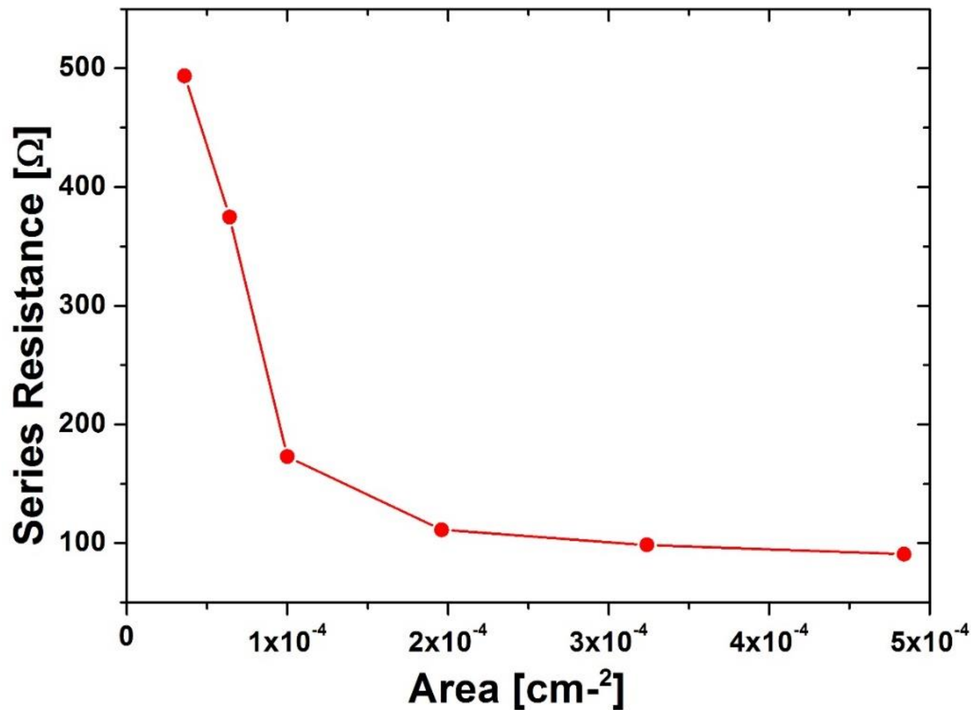


Figure 4.6. Series resistance vs the Ge mesa area of 350 nm thickness.

From the results, there is a strong relation between the size, the shape and the location of the illuminated part of a junction photodiode, and its series resistance. This relation creates an expectation for a big variation of the response time (the time for which the photo-generated charge will be removed). This is because the time constant of the photodiode, which is one of the main factors defining the response time, is a product of the series resistance and the junction capacitance. The time response of the Ge-on-Si photodiodes with respect to the area is discussed later in this chapter.

4.1.4. Responsivity

The responsivity or photoresponse is the figure of merit of the photodetector conversion efficiency. It is a measure of how the photodetector absorbs the light, converts it into electron hole pairs and extracts the photogenerated carriers from the device by generating a current. The photocurrent depends on the collected carriers generated in the space charge region and within one diffusion length. The photocurrent of Ge-on-Si photodiode is measured with a current to voltage converter and a lock-in amplifier to cancel the dark current and get rid of the noise. A laser source at 1550nm wavelength is focused by lenses on the top of the Ge mesa and measured with a power meter.

The device responsivity is obtained by dividing the photocurrent by the incident optical power. The light beam is modulated by a chopper and the modulated photocurrent is collected by the GSG probe and converted into a photovoltage by an adjustable transimpedance amplier (TIA), which is capable of biasing the device with an external voltage source. There is a slight increase in responsivity with applied reverse bias due to an improved charge collection efficiency in the photodiode and the increase of the depletion layer. The TIA output is demodulated by the lock-in amplifier and acquired in LabView environment.

Fig. 4.7 shows the measured responsivities versus the reverse voltage for two Germanium layer thickness. The responsivity values ranges from 1.2mA/W to 1.4 mA/W at 1V reverse bias and 1550nm wavelength. It is evident from the figure that a thicker Ge film will increases the responsivity [110], by increasing the probability of photon absorption. However, the response time will be increased due to the longer transit time for the photocarriers to reach the electrodes.

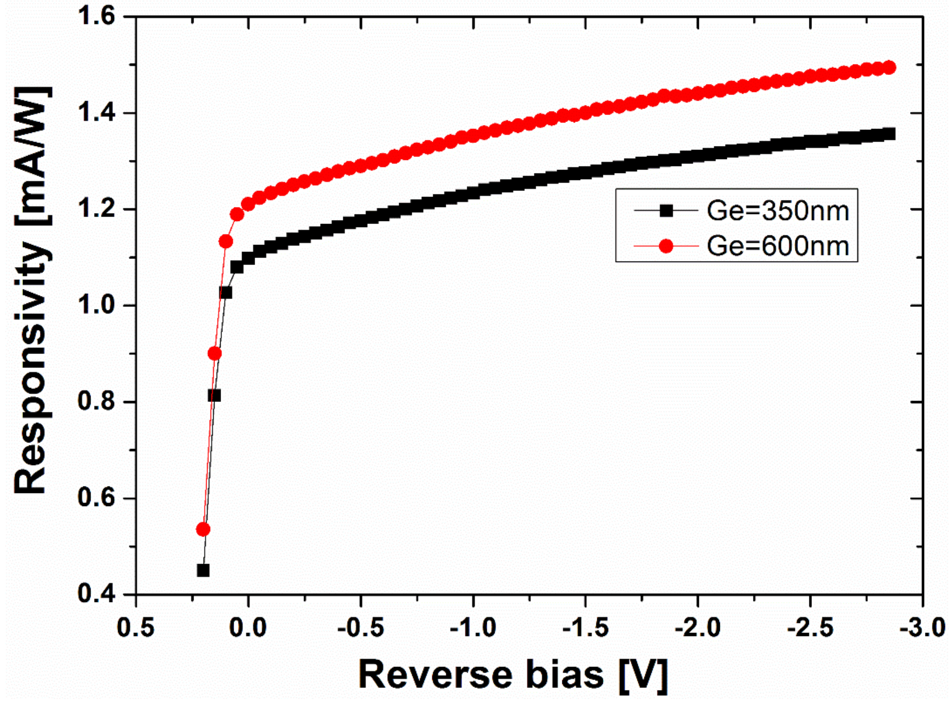


Figure 4.7. Responsivity of Ge-on-Si photodiode as a function of reverse bias for different Germanium layer thickness.

The obtained responsivities are rather low because of the highly defected Ge layer. The active absorption layer can be estimated from,

$$R = \eta_c \frac{\lambda}{1.24}(1-\Theta)\left(1-e^{-\alpha(\lambda)d}\right) \qquad (4.6)$$

where the (1-Θ) term accounts for the reflection at Ge/air interface. The active absorption layer is:

$$d = -\frac{1}{\alpha} ln\left(1-\frac{1.24R}{\eta_c \lambda(1-\Theta)}\right) \qquad (4.7)$$

Assuming a typical absorption coefficient of Ge thin films [82], the active layer is estimated in the range 10-100 nm depending on the collection efficiency λ_c. The devices exhibit large short-circuit currents with a maximum responsivity at zero bias. This is commonly associated to efficient collection properties. It is possible to conclude that evaporated Ge-on-Si detectors exhibit good detection properties but with short minority carrier diffusion length. By adopting waveguide configuration however, it would be possible to obtain improved collection efficiency and avoid the limitations due to the short active

layer. Therefore, the reverse currents flowing across the junction are limited by transport mechanisms; probably the trap-assisted tunneling due to interface states rather than associated to standard generation/recombination models. These effects are related to the Si/Ge interface quality and are important when the defect-density increases.

4.1.5. Time Resolved Photoresponse

The time resolved photoresponse of the Ge-on-Si photodiode was investigated by illuminating the devices with picosecond light pulses and data acquisition is performed with a high-bandwidth sampling oscilloscope (Tektronik CSA 803C). The setup involves a picosecond fiber-laser (Pritel) at 1550nm wavelength, amplifed by an optical fiber amplifer to provide a larger signal. The photocurrent is converted into voltage by the low input resistance (50Ω) of the digital oscilloscope. A bias-tee is inserted between the instrument and the photodetector to filter out the lowest frequencies, like the dark current, and to provide an external reverse bias to investigate the temporal response versus bias. Turn-on and turn-off response times (τ_{on} and τ_{off}) depend on series resistance, bias, optical power, area and thickness of the Ge layer.

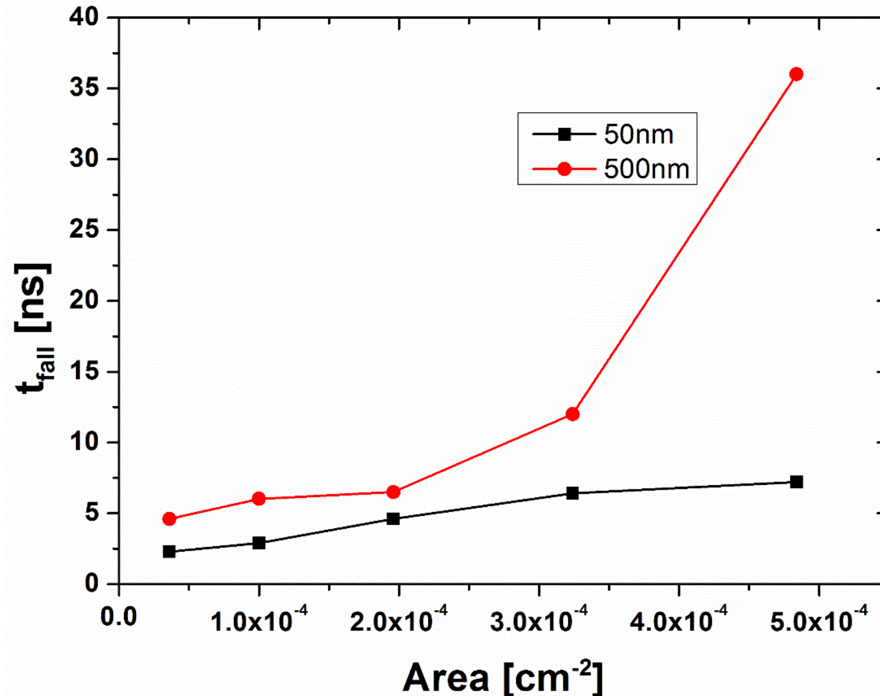


Figure 4.8. Fall time vs Ge mesa area of the photodetector as a function of Germanium layer thickness.

Fig. 4.8 shows the fall time extracted from the measured pulse response of Ge-on-Si photodiodes with 50nm and 500nm Germanium films. The turn-on time is very short compared to turn-off time. The detector with 50nm Ge layer exhibits fall time from 2ns for smaller device to 7ns for larger area devices. Meanwhile the detector with 500nm Ge layer exhibits fall time in the range of 4ns to 36ns. The longer tail in turn-off time is due to the diffusion of the photogenerated carriers and the faster response can be related to extrinsic RC time constant of the pn junction as discussed in section 4.1.3.

4.2. Ge-on-Si Photodiode Connected to MOSFET Gate

The concept of controlling the drain to source current of a MOSFET by an optical input was successfully demonstrated by many researchers by connecting a photodiode to the MOSFET gate either by bonding [111-113] or by direct connection. In addition, photodiode connected to the body of a SOI-MOSFET, where, Carriers photo generated in the photodiode flow to the body and induce the bipolar action of the SOI MOSFET and the SOI MOSFET amplifies the diode photocurrent [114].

In order to test the operating principle of the simulated optically controlled FET, I have used a photodiode connected to a MOSFET gate. The Ge-on-Si photodiode discussed in the previous section is used as a photosensitive gate connected directly to a MOSFET fabricated in a foundry pilot line. The fabricated device is a trench gate, p-channel MOSFET operating in enhancement mode. Some of the physical parameters of the trench MOSFET are shown in table 4.1.

Parameters	Values
Pitch [μm]	2.2
W_{trench} [μm]	0.6
A_{gate} [mm^2]	9.5

Table 4.1. Device physical parameters of the trench gate MOSFET.

The schematic cross section and optical microscope picture of the fabricated trench MOSFET is shown in figure 4.9. The source and body of the MOSFET are interconnected and the drain is at the bottom.

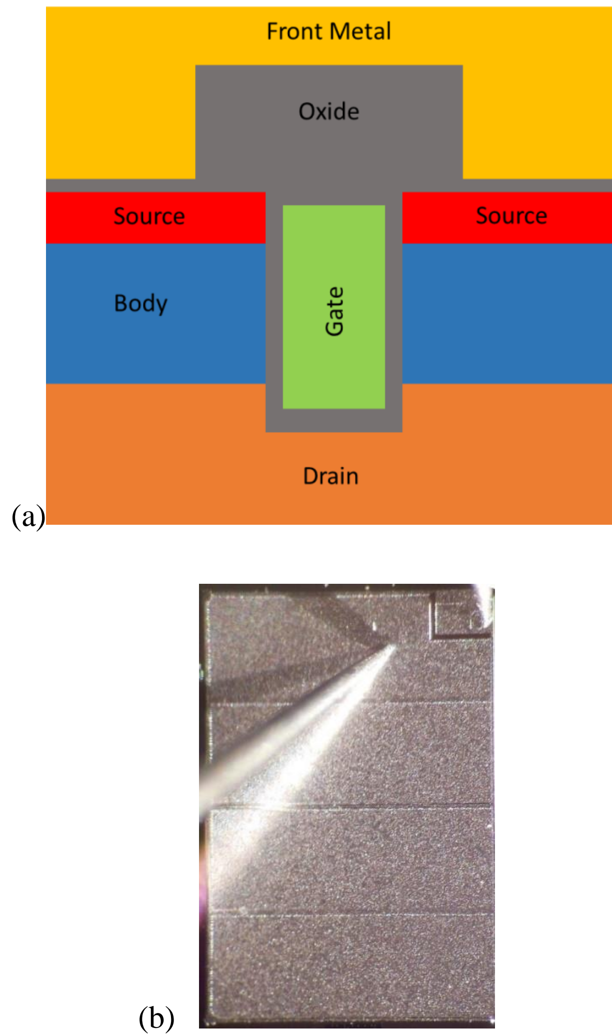


Figure 4.9. Schematic representation (a) of the Trench MOSFET and (b) its optical microscope image.

The current-voltage characteristics of the trench gate MOSFET are studied and its threshold voltage is evaluated as -2.5V. Figure 4.10 (a) and (b) shows the I_{Drain}-V_{Gate} and I_{Drain}-V_{Drain} characteristic plots of a typical device, respectively. I choose to rotate the curves to the first quadrant for better readability. At a drain voltage V_{DS}=-2V, under dark condition, the trench MOSFET exhibit a threshold voltage of -2.5V. Therefore, the offset gate bias will

be kept below this threshold voltage under illumination on the photodiode connected to the gate.

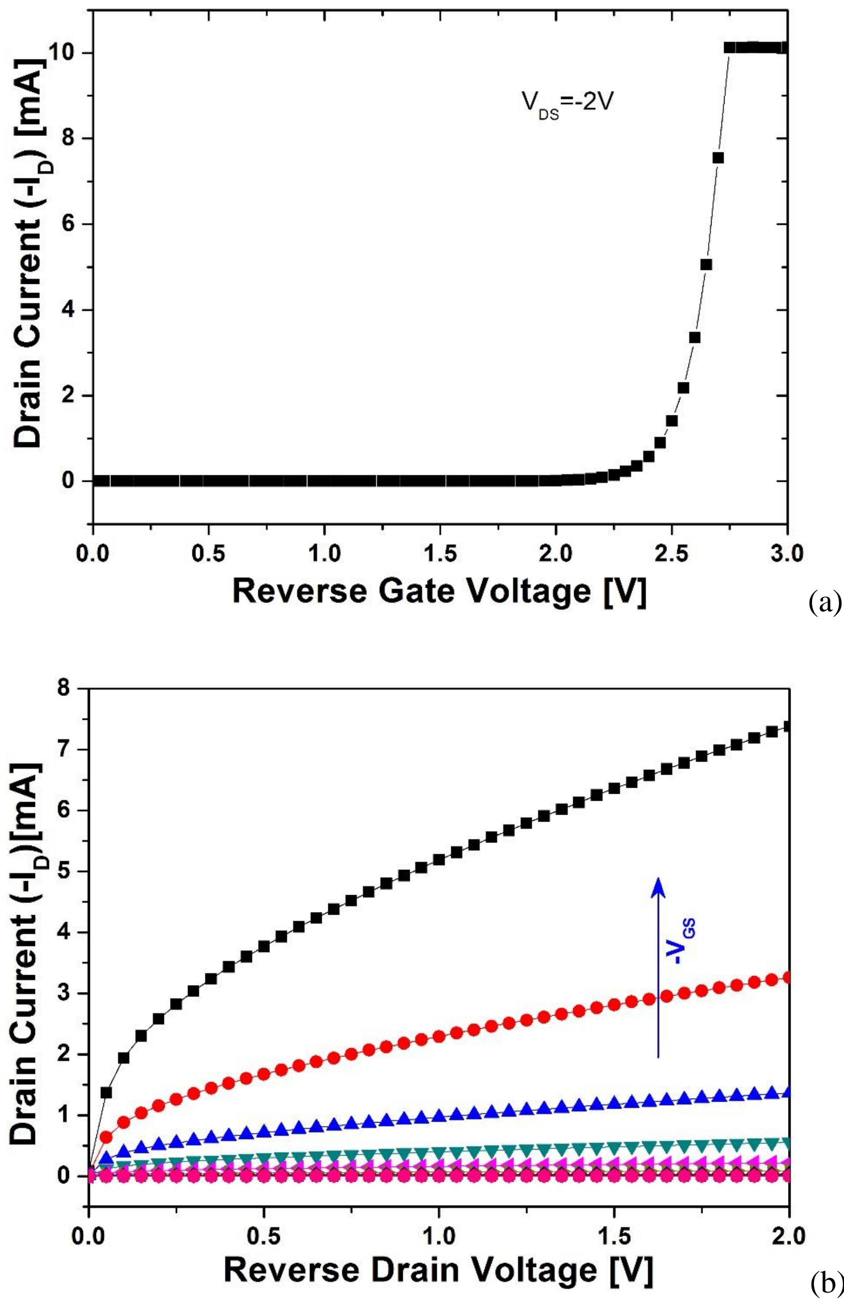


Figure 4.10. (a) I_{Drain}-V_{GS} characteristics of the trench MOSFET with V_{DS}=-2V and (b) I_{Drain}-V_{DS} characteristics of the trench MOSFET with increasing V_{GS} from -2V to -2.8V.

The Ge-on-Si photodiode is connected to the gate terminal of the trench MOSFET as shown in the fig. 4.11. The photodiode connection can be modified according to the type of the MOSFET (p- or n-channel).

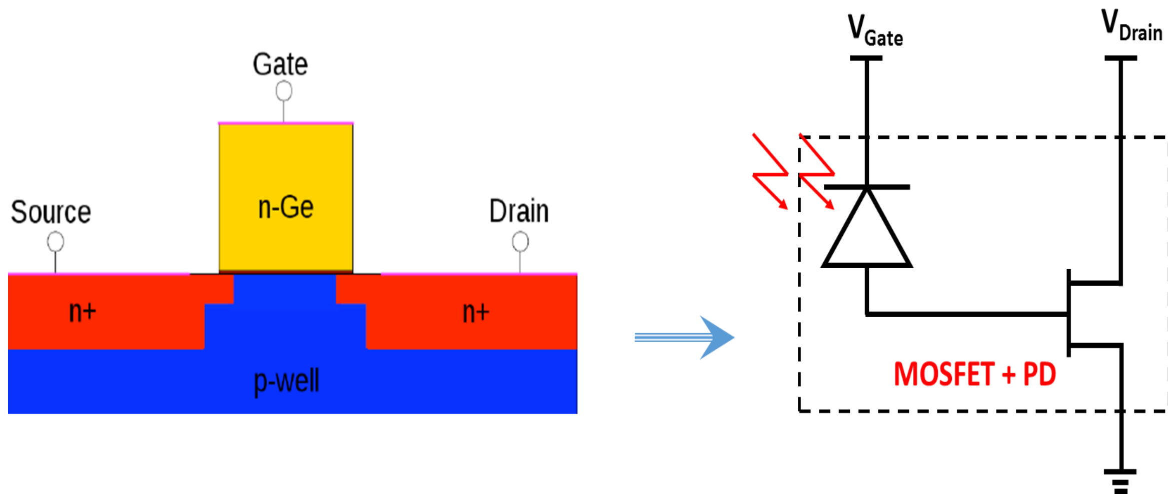


Figure 4.11. The basic configuration of connecting a photodiode to the MOSFET gate terminal to modify its channel modulation. The simulated monolithic optically controlled field effect transistor is shown on the left.

The Ge-on-Si photodiode is connected to the gate terminal of the trench MOSFET. The current-voltage (I-V) measurement set-up is an automatic acquisition system composed by a LabView environment GPIB interfaced with a voltage source (Hewlett-Packard HP4140B) as gate supply and Keithley SMU236 for drain supply and ammeter. The drain current to gate voltage characteristics of the circuit is shown in figure 4.12. The drain current was measured for V_{GS}=0V to 3V in dark condition and when the photodiode is illuminated with 10mW optical power at 1550nm. Due to the thin Ge layer, taking into account the optical absorption coefficient at 1550nm, the absorbed optical power is about 6% only. Therefore, 10mW correspond to 0.6mW.

I observed a shift in the curve similar to the characteristic curve of the simulated OCFET discussed in chapter 3 proving the additional gate voltage due to the optical input. The drain current saturates at 10mA due to the maximum measuring range of the ammeter.

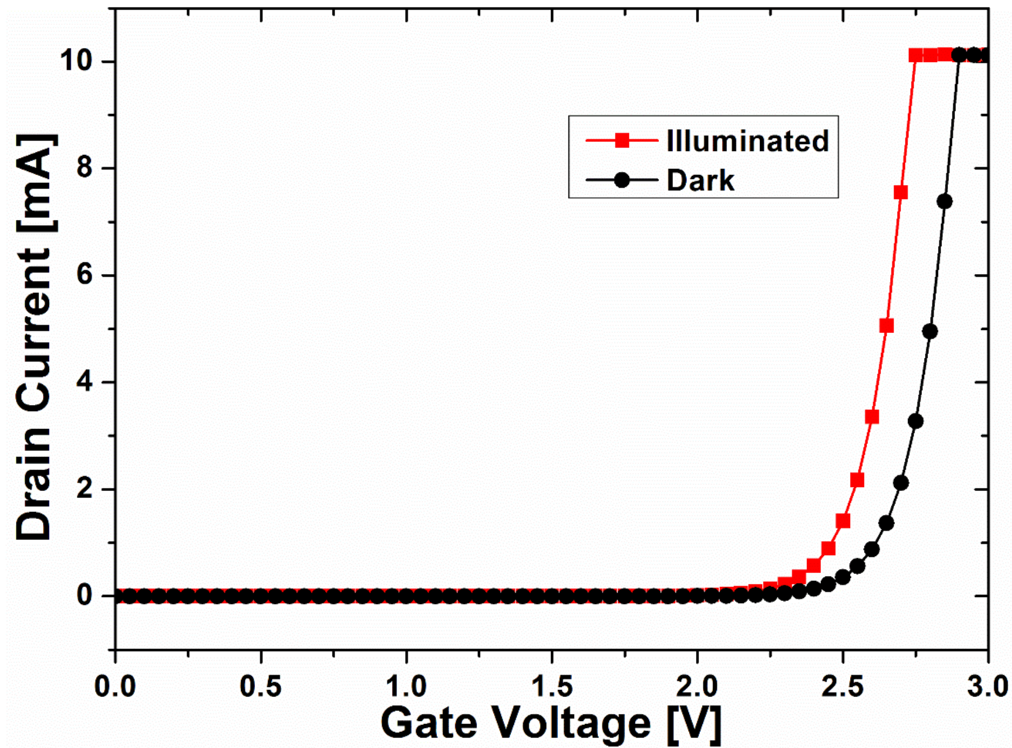


Figure 4.12. I_{Drain} vs V_{Gate} characteristics as a function of optical input power (dark condition and 10mW, 1550nm).

Figure 4.13 shows the I_{Drain}-V_{Drain} characteristic curve of the circuit as a function of optical input power at V_G=2.2V. The gate voltage was fixed at 2.2V, to maintain the input just below the threshold voltage (2.5V) of the trench MOSFET, a similar condition with the simulated OCFET. The optical input power is varied from dark condition to 10mW. The drain current increases from 60μA at V_{DS}=1V for dark condition to 100 μA at V_{DS}=1V for 10mW optical input. This corresponds to an Ion/Ioff ratio of 1.67 and a responsivity of 4mA/W. This characteristics is similar to the simulated drain current of the OCFET as a function of input optical power proving the working principle of the OCFET. The higher dark current is due to the applied gate voltage.

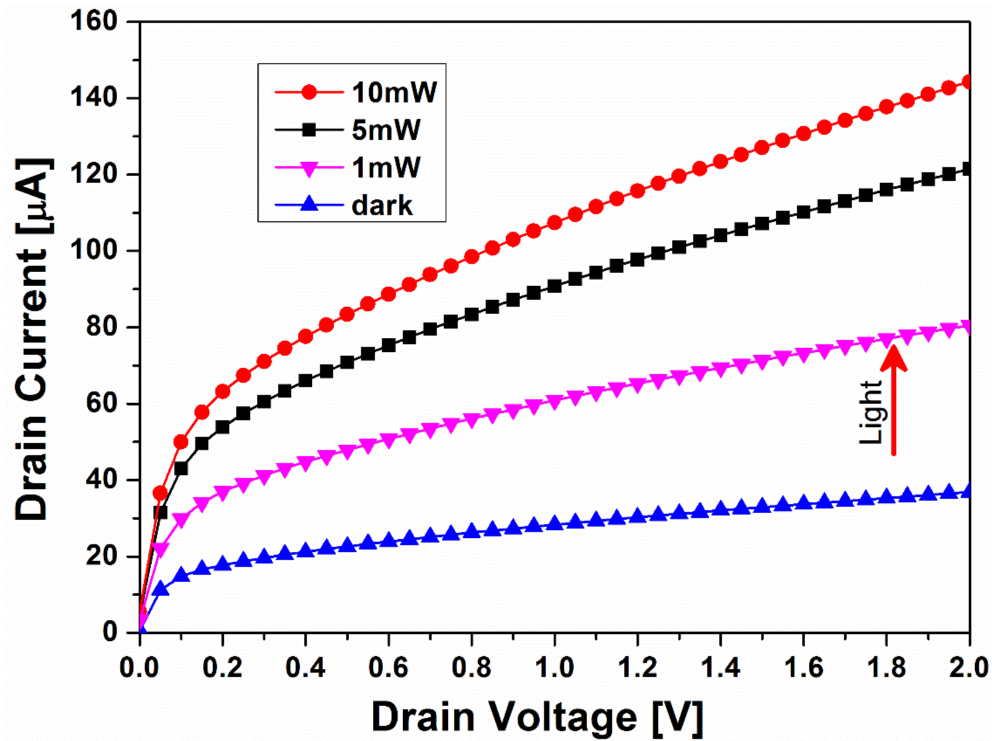


Figure 4.13. Measured drain current vs drain voltage of the circuit as a function of optical input power (1550nm) at V_G=2.2V and V_D=2V.

In this chapter, the working concept of the simulated Ge gate OCFET is studied by a Ge-on-Si photodiode connected to the gate of a MOSFET and similar results are obtained compared to the OCFET operation.

5

Optical JFET

5.1 Introduction

In recent years, a great deal of interest is shown in the field of optical interconnects due to the increasing speed degradation and many other issues of conventional metal interconnects. Integration of photonics with existing electronics technology as data and clock delivery systems is needed to resolve these issues. Excellent optoelectronic integrated circuits (OEICs) that employ p-i-n photodiodes and APDs are being studied and used for optical interconnections. Besides these photodiodes, novel structures (FET based detection) with optical gain to maintain detection efficiency even with small detector sizes, have attracted increasing research interest based on both group IV [115-117] and III-V materials [118-121]. A brief introduction of phototransistors was given in chapter 1. With the main focus of this thesis being Ge based detection, we emphasize Ge based field effect photodetectors. Germanium, being one of the critical components for low-cost Si-based optoelectronic integrated circuit, FET based detectors like, a highly scalable JFET based germanium photodetector whose dimensions are comparable with that of modern MOSFETs are reported [117]. The highest reported device responsivity was 5A/W with rise time and fall time being 40ps and 40ns respectively. Wang et al [122 and 123] demonstrated a high responsivity (642mA/W) and low standby current (0.5µA at 1V) and a scalable Ge photodetector based on a junction field-effect-transistor (JFET) structure with high sensitivity (Ion/Ioff ratio of 185) and improved rise time and fall time of 10ps and 110ps at a wavelength of 1550nm. In this chapter, I discuss the design, fabrication and characterization of an optical JFET with Ge gate operating at 1550nm wavelength.

5.2. Device Structure and Operation

In this study, I demonstrate a Ge gate p-type Optical JFET photodetector built on silicon-on-insulator (SOI) wafers with the optical input guided through a Si waveguide. I have designed two set of optical JFET, one with an intrinsic Si channel and other with a p-type Si channel, both with channel lengths of 4μm and 8 μm. The Ge gate is intrinsic in all the devices, with n-type doping for the gate contact. Such gate contact can be used to bias the device in the best operating point. The Optical-JFET device geometry is presented in figure 5.1. The devices are studied with and without applying external gate voltage.

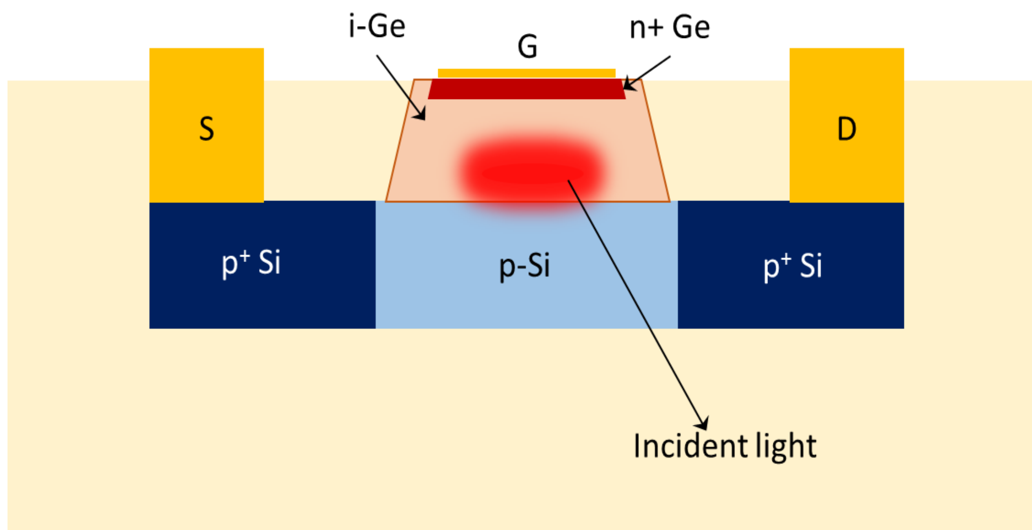


Figure 5.1. Device structure of a p-channel Ge-on-Si Optical-JFET. The light is coupled through a Silicon waveguide with grating coupling between the optical fiber and the waveguide.

The fabrication has been performed by a foundry, on a multi-project wafer run dedicated to Silicon Photonics. Since the design kit does not provide FET devices, I have adapted the design in order to obtain a JFET while satisfying the foundry design rules. In both the p-channel and the intrinsic channel Optical-JFETs, the source and drain region were formed by conventional implantation. The germanium gate is deposited by selective epitaxy at high temperature. The Optical-JFET is a conventional JFET with a Ge absorbing layer as gate. The physical parameters and dopant type of the devices are given in table 5.1.

Parameters	**Values**
Si mesa thickness (nm)	220
Ge gate thickness (nm)	500
Channel length (µm)	4 and 8
Channel doping	p-type / intrinsic

Table 5.1. Physical parameters of an Optical JFET.

The input light is coupled into the device through a waveguide scheme. The optical input coupling between a single mode optical fiber and the waveguide is performed with a planar grating coupler. Near infrared light is absorbed in the Ge gate only, and the channel conductance is expected to be changed. The direct deposition of Ge on Si, is quite defective at the interface and it introduce deep electronic states in the bandgap, pinning Fermi level close to valence band edge. Due to the fact that most of the depletion region is in the Silicon, the collection of any photogenerated carriers within the Ge film is dominated by diffusion. Due to the large valence band offset (~0.46 eV) between Ge and Si, the photogenerated holes are confined in the Germanium at the Ge-Si interface. The accumulated holes attract electrons in the Si channel, thus changing the width of the depletion region, which leads to enhanced source–drain conductance.

5.3. Characterization

In an optical JFET, the heterojunction between Ge and Si, is an important section for the optical detection. Therefore, we analyze the Ge-Si heterojunction photodiode in both dark and illuminated conditions.

5.3.1. Ge-Si Heterojunction Photodiode

The current-voltage characteristics of the Ge/Si photodiode are measured between the gate and the source (or drain) contact. A Continuous-wave near infrared light at 1550nm is coupled to the germanium mesa through a silicon waveguide by grating coupling from a single mode optical fiber. Figure 5.2 shows the I-V curves of in dark and illuminated conditions. The optical power is increased from 0 (dark) to 1mW (0dBm).

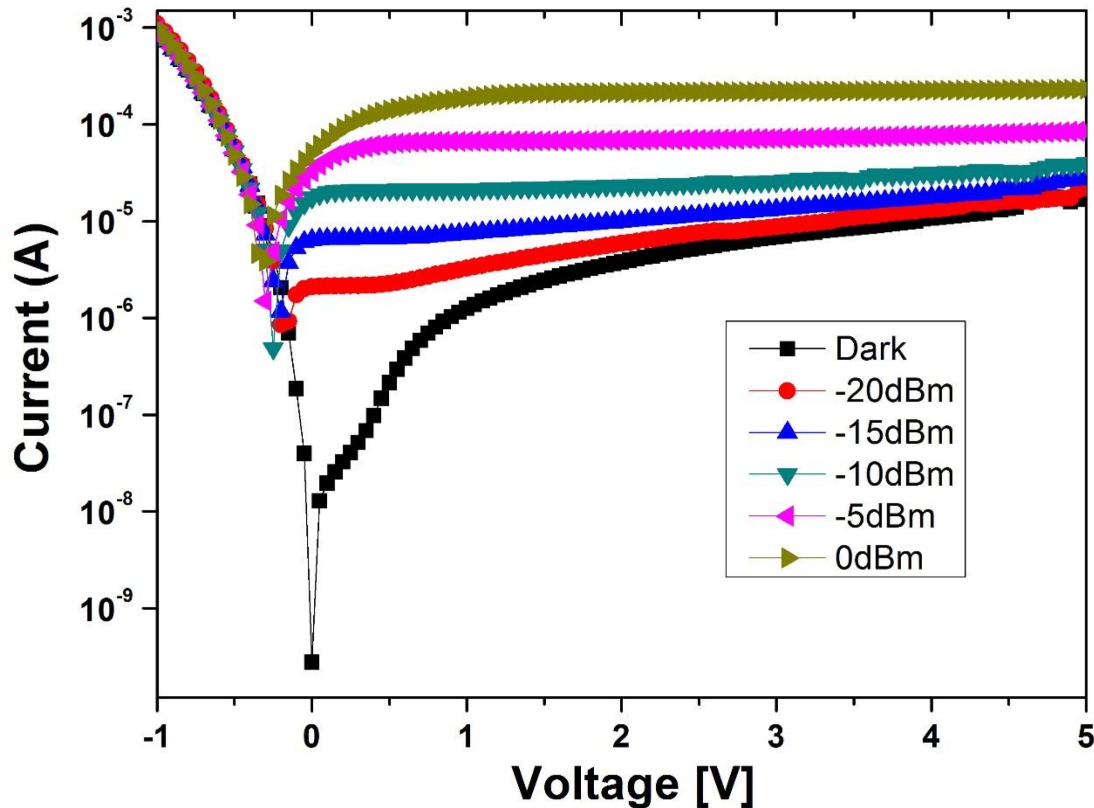


Figure 5.2. Current-Voltage characteristics of the Ge-Si heterojunction as a function of the optical power.

From figure 5.2, the dark current at the heterojunction photodiode region at 1V was around 1.2μA. For an incident power of 10μW (-20dBm) at 1.55μm, the photocurrent is 2 μA at 1V and it increases to 180 μA at 1mW (0dBm). So the responsivity of the heterojunction photodiode region is 200mA/W and 180mA/W at input optical powers of 10μW and 1mW respectively.

In the following sections, I discuss the characterization of the Optical JFET in a biased gate and floating gate configurations.

5.3.2. I-V Characteristics (Floating Gate)

At first, the current–voltage (I–V) measurements were carried out on the Optical JFET with open gate configuration. The optical input power was increased from dark condition to 0dBm (1mW) with V_{DS} swept in the -5V to +5V range. Figure 5.3 shows the I_{drain}-V_{drain} characteristics of the Optical JFET at V_{DS}=-5V with dark to 0dBm input optical power of wavelength 1550nm.

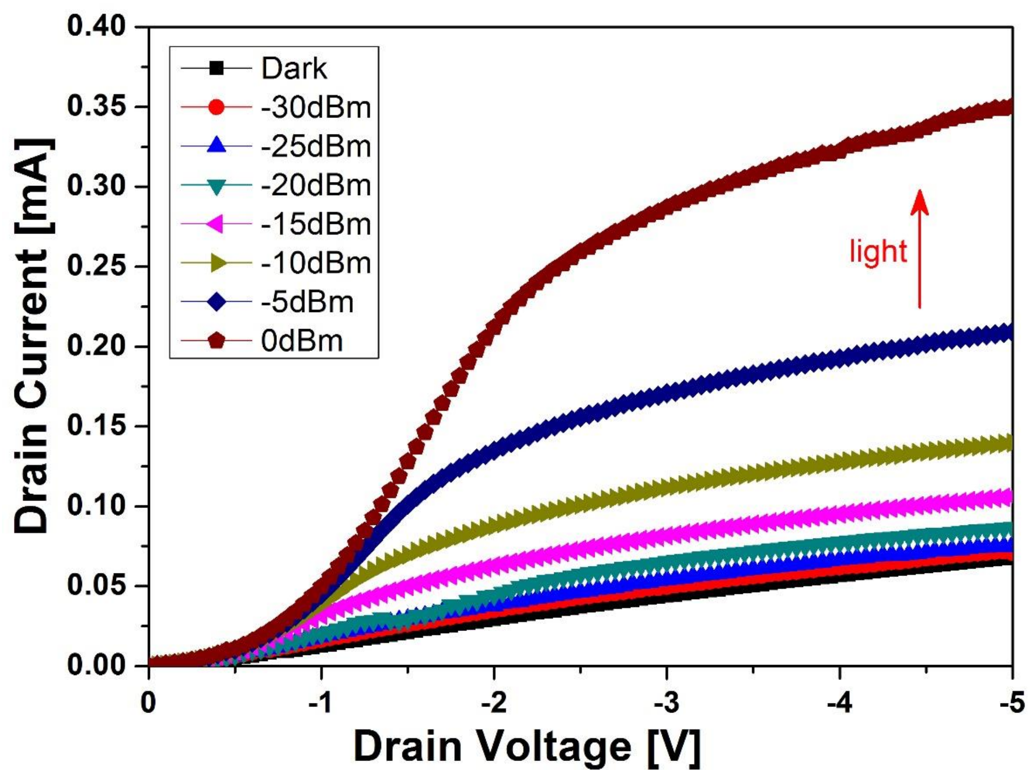


Figure 5.3. Current-Voltage characteristics of the Optical JFET as a function of optical power at floating gate configuration. The optical power was varied from 1μW to 1mW coupled through silicon waveguide via grating coupling to a single mode optical fiber.

The optical power in dBm indicates the optical input power from the fiber. Taking both grating and waveguide losses, a factor of about 4 should be evaluated (therefore 1dBm means that 0.25mW illuminates the JFET). From figure 5.3, without optical input (dark), the device exhibits a leakage current of 44μA at -3V bias, which corresponds to the channel

"off" state because of the depletion formed in the junction region between the Si channel and the Ge gate. For optical characterization, light was coupled onto the device through grating coupler from a single-mode fiber (with a core diameter of ~8.2 µm).

For our device with a 1550-nm laser of 1mW power, at a bias of V_{DS} = -3V, drain current is increased from dark current by 6.5 times to 280 µA. The responsivity is of ~5.3 A/W at -30dBm optical power and decreases to 0.2A/W at 0dBm optical input. The Ion/Ioff ratio of the device increases from 1dB at an optical power of -30dBm to 16dB at 0dBm optical power at a drain voltage of -3V. The figure 5.4 shows the Ion/Ioff ratio and the responsivity of the optical JFET as a function of optical power varied from -30dBm to 0dBm.

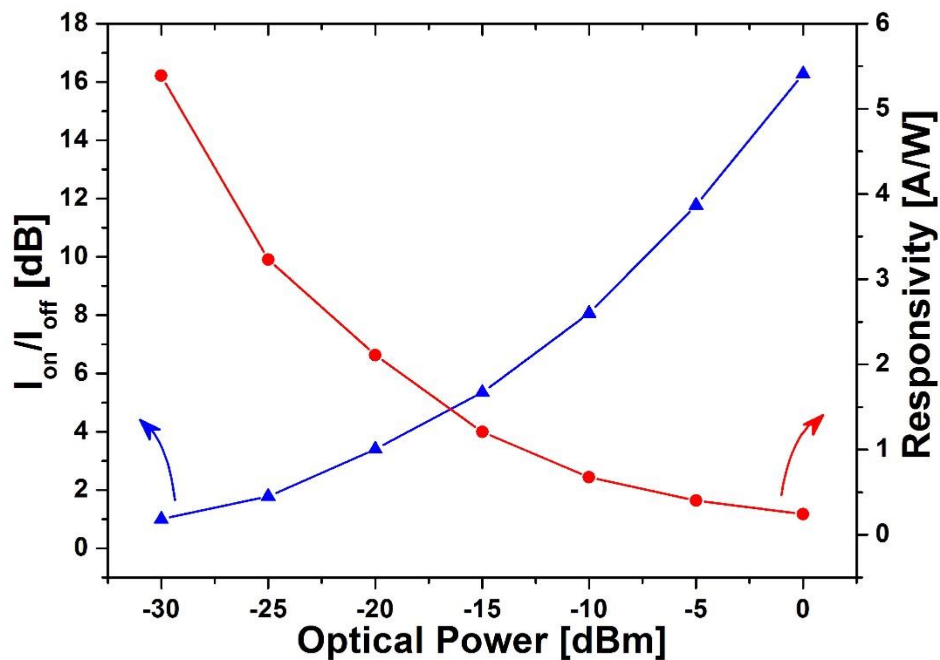


Figure 5.4. Ion/Ioff ratio and responsivity extracted from fig. 5.3, as a function of input optical power at V_{DS}=-3V.

The achieved responsivity is greater than the maximum theoretically achievable from a junction photodiode (R=1.2A/W at 1.55µm), which is a clear demonstration of the transistor effect (gain).

The decrease in responsivity with increasing optical power may be attributed to the intrinsic transistor operation similar to optically controlled MOSFET. Even though the

responsivity is high at lower power (-30dBm), in terms of ratio between the photocurrent and dark current (signal to noise ratio), the device performs better in higher optical power. The device exhibits a signal to noise ratio of 14dB at 0dBm (1mW) optical power compared to 3.7dB at -10dBm (100μW) optical power. This issue can be solved by increasing the optical power, which in turn reduces the responsivity of the device.

5.3.3. Dynamic Characteristics

The dynamic characteristics of the optical JFET is studied by simulation using ISE-TCAD. The simulated device is similar to the fabricated optical JFET with 4μm channel length and 1μm channel width. The source and drain doping concentrations are at $10^{20}cm^{-3}$ and $10^{16}cm^{-3}$ p-type channel doping. Figure 5.5 shows the transfer characteristics of optical JFET, by applying an optical pulse of 1.55μm wavelength for 10ns with floating gate and V_{DS}=-1V. The optical input was varied from 1μW to 100μW. The drain current is normalized to show the change in rise time and fall time of the optical JFET (inset).

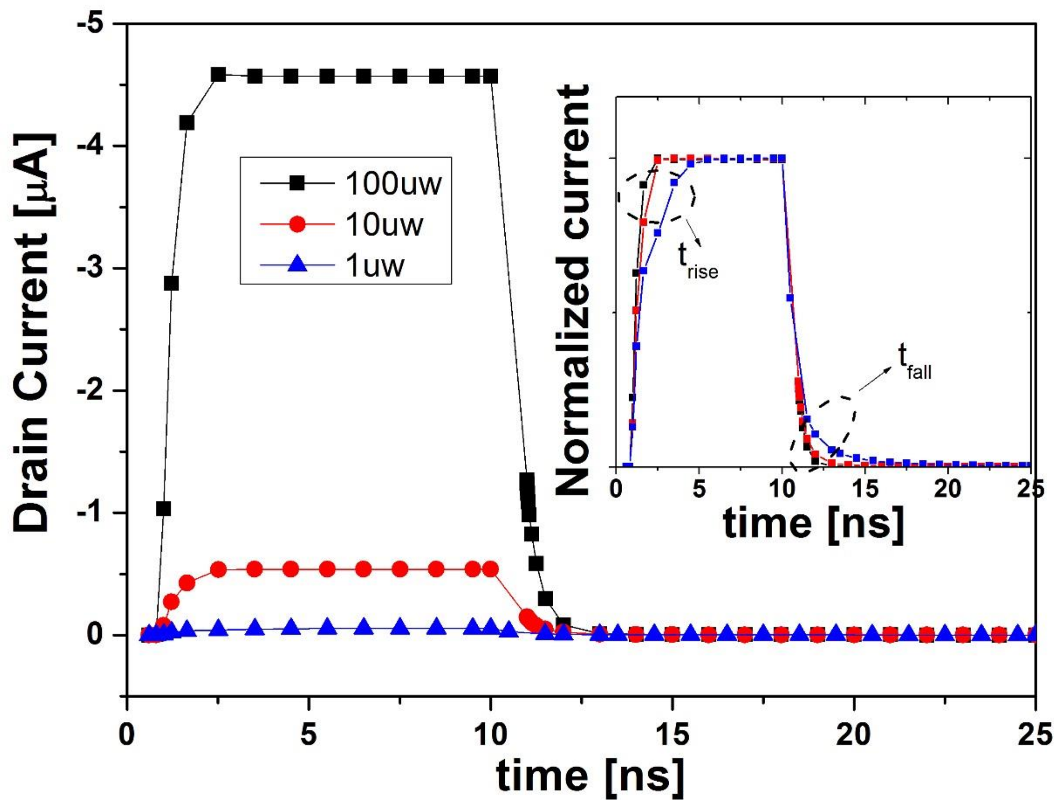


Figure 5.5. Simulated drain current vs time as a function of optical power from 1μW to 100μW. The normalized drain current versus time is shown in the inset.

From figure 5.5, the drain current for 1µW optical power was 53nA, and increases to 4.5µA for 100µW optical power. This corresponds to an increase in I_{on}/I_{off} ratio from 34dB to 72dB for 1µW and 100µW optical power respectively. The increased optical power reduces both rise time (t_{rise}) and fall time (t_{fall}) of the device. The rise time decreases from 5ns for 1µW optical power to 2ns for 100µW optical input. Similarly, the fall time is reduced from 4.5ns for 1µW optical power to 2ns for 100µW optical input. This effect of optical power is consistent with the simulated transfer characteristics of the OCFET.

Concerning the DC characteristics, applying a gate bias could exert a strong electric field, which would enhance photodetection in Ge layer. Therefore, we decided to apply an additional gate bias along with the input optical power. In the next section, I discuss the current-voltage characteristics of the Optical JFET with applied gate voltage.

5.3.4. I-V Characteristics (With Gate Bias)

In this section, the I-V characteristics of the Optical JFET is studied with added gate bias. Figure 5.6 shows the drain current vs the gate voltage with increasing optical power at a drain voltage V_{DS}=-2V. The drain current values are shifted to 1st quadrant. The drain current increases with optical power as well as with the gate voltage, showing the typical JFET characteristics.

At V_{GS}=0V, we observe the increase in drain current from 19µA at dark condition to 200µA at 1mW (0dBm) optical power. Whereas, the drain current is increased to 420µA at 1mW (0dBm) optical power with V_{GS}=-1V. Unfortunately, there is an increase in dark current as well (300µA) at V_{GS}=-1V, deteriorating the sensitivity of the device. The photocurrent I_{ph} at zero gate bias with -10dBm optical power (18µA) increases by one order of magnitude (180µA) for 0dBm optical power. At the same time, the photocurrent decreases to 12µA for -1V gate bias at -10dbm optical power. This can be attributed to the increase in carrier recombination before being reaching the Ge-Si interface. When the gate bias is large, the gate-to-source junction resistance (even the gate-to-drain junction resistance) becomes very small and thus the channel resistance is shorted.

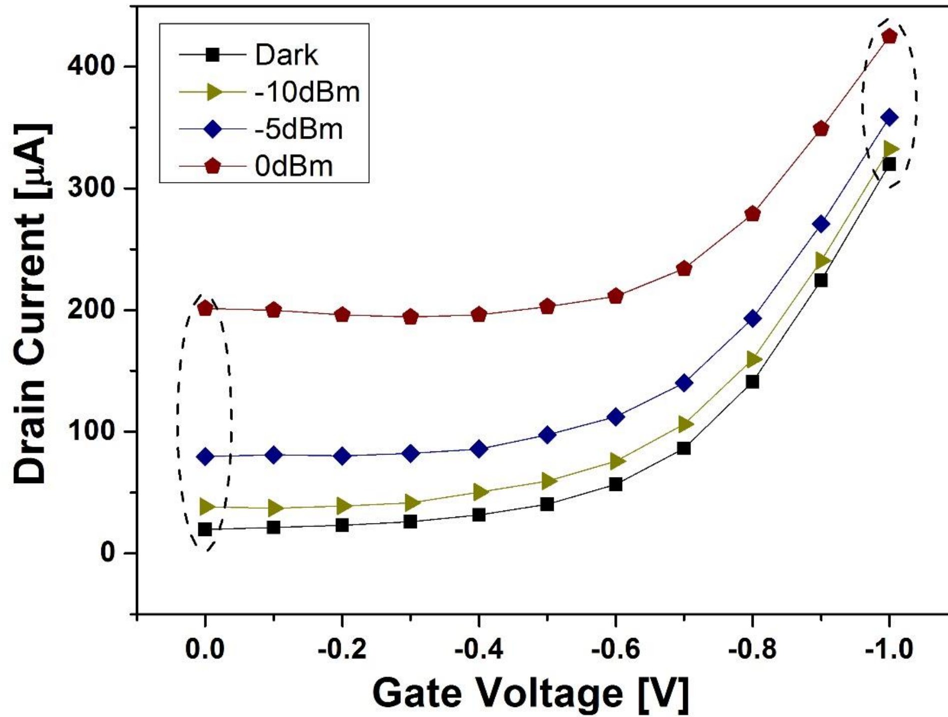
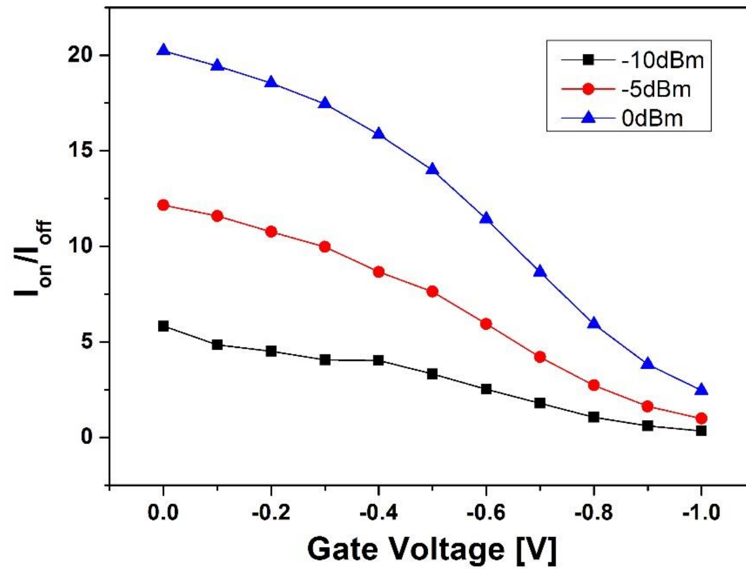
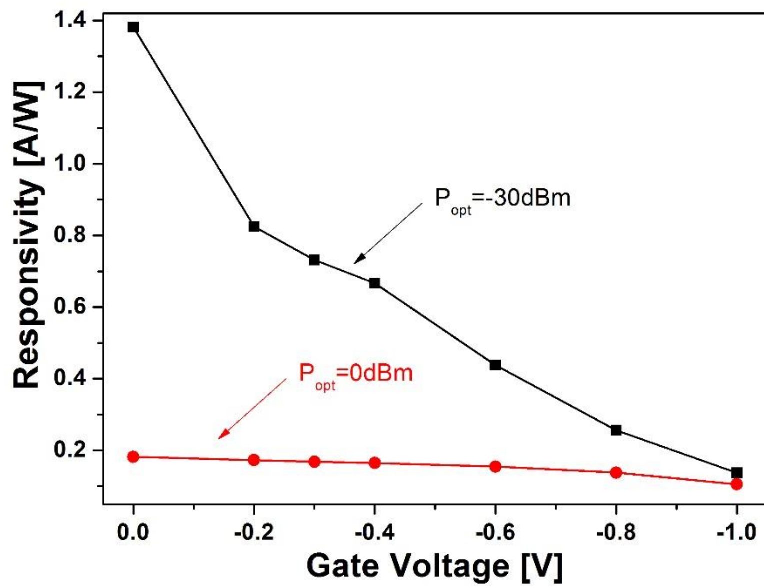


Figure 5.6. Drain current vs the gate voltage (V_{GS}) as a function of optical power at a drain voltage of -2V.

Figure 5.7 shows (a) the Ion/Ioff ratio and (b) the responsivity of the device as a function of optical power, with increasing gate bias (V_{GS}). It is evident that the Ion/Ioff ratio increases with input optical power (from 5.8dB for -10dBm optical power to 20dB for 0dBm optical power). In contrast, the Ion/Ioff ratio decreases with gate bias (from 20dB for zero bias to 2.4dB for -1V at 0dBm optical power). The increase of the gate bias increases the dark current as well, decreasing the dark-light current ratio. In fig. 5.7 (b) the responsivity shows similar trend like the floating gate configuration, where the responsivity decreases with increasing optical power. The responsivity at zero gate bias with -30dBm optical power was 1.38 A/W and it decreases to 0.18 A/W at 0dBm optical power. When we increase the gate bias from 0V to -1V, with optical powers -30dBm and 0dBm, the responsivity decreases from 1.38 A/W to 0.13 A/W at -30 dBm and from 0.18 A/W to 0.1 A/W for 0dBm optical power.



(a)



(b)

Figure 5.7. (a) The ratio between the drain current with light and dark conditions at increasing gate bias (V_{GS}=0V to -1V) as a function of optical power (from -30dBm to 0dBm). (b) The responsivity of the optical JFET at increasing gate bias (from 0V to -1V) at two optical powers (-30dBm and 0dBm). The drain voltage was -2V for both plots.

With the combination of optical input and gate bias, the drain current increases (420μA at -1V gate bias) as expected compared to floating gate configuration (212μA at floating gate) both at V_{DS}= -2V. However, the responsivity decreases from 5.3A/W in floating gate to 0.13A/W at V_{GS}=-1V and V_{DS}=-2V. With the larger gate voltage, the resistance across the channel decreases exponentially with the voltage, clearly indicating that the transistor is operated as two diodes and the channel depletion modulation is too small. Hence, the floating gate configuration performs much better than the device with additional gate voltage in terms of responsivity, even though the drain current increases with applied gate bias. Therefore, in order to improve the device sensitivity, the dark current must be improved by design (for example changing the channel doping type and concentration).

Conclusions

In this dissertation, a Ge gate, optically controlled field effect transistor (OCFET) was designed and simulated using ISE-TCAD. The DC and transient characteristics of the device in terms of Ion/Ioff ratio, responsivity and fall time were studied. Optimum doping concentrations for higher Ion/Ioff ratio (~50dB) was evaluated as ~$10^{17}cm^{-3}$ for both Ge gate and Si body. Even though the drain current decreases with reduced gate voltage, the Ion/Ioff ratio was enhanced (~70dB) due to the reduction in dark current. At V_G=0.5V the Ion/Ioff ratio increase from 3dB to 40dB when the optical power is varied from 1nW to 10μW. However, at higher gate voltage (V_G=0.8V) the increase in Ion/Ioff ratio is minimum (between 6dB to 21dB) for the same range of optical power, even when the absolute Ion increases consistently. With reduced doping, and gate bias the device exhibits faster pulse response, with reduced drain current. In terms of responsivity (drain current over input optical power), a maximum responsivity of 100A/W, corresponding 1nW optical input light and 4A/W for 1μW and 0.9A/W for 10μW optical power were obtained. When the device is scaled for channel length, the modulation current (I_{on}-I_{off}) increases by shortening the gate length, thus increasing the responsivity of the devices. With a scaling factor of 3.8, a 100x increase in modulation current was observed from 0.35μm to 0.09μm channel length.

The Ge gate thickness affects the responsivity and the fall time of the device. The responsivity of OCFET with 50nm Ge layer was 1.1 A/W at 1nW optical power, which increases to 8.3 A/W for 400nm thick Ge layer at same optical power. Both rise time (t_{rise}) and fall time (t_{fall}) decreases with increase in optical power. The Ge carrier lifetime was modified in the Scarfetter relation to modify the film property. The devices exhibit very fast rise time and much slower fall time for increasing Germanium carrier lifetime. With the help of the simulated results, possible parameters for faster and high responsivity device are evaluated.

The inverter characteristics are studied while varying the parameters of the loads (load resistor values, W/L ratio of the load transistor in saturated load inverter and W/L ratio of p-

channel OCFET in CMOS configuration) along with the device parameters studied in static characteristics. Transfer characteristics and transient response (fall time, rise time) are analyzed with various combinations of these parameters. In summary of all the inverter configurations, the lowest rise time achieved was around 400ps but with very low output swing of 0.02dB. With the highest output swing of 30dB, the rise time was around 40ns.

In order to evaluate the proof of concept of the OCFET, I had to rely on connecting a Ge-on-Si photodiode at the MOSFET gate terminal. The Ge-on-Si photodiode and trench MOSFET were designed and fabricated and the OCFET concept was investigated under dark and illuminated conditions. These experiments are quite similar in the operating principle to the simulated monolithic OCFET.

At the end of this work, we had the opportunity to resort to a foundry, which allowed enough flexibility to get a JFET fabricated. Optical JFETs with 4µm and 8µm channel length and Ge thin film of 500nm as the gate were designed and fabricated. The current-voltage characteristics of the Optical JFET were investigated with open gate and applied gate bias. The results clearly demonstrate a transistor effect with a photocurrent gain. In the open gate configuration, the device exhibits a signal to noise ratio of 14dB at 0dBm (1mW) optical power compared to 3.7dB at -10dBm (100µW) optical power. The responsivity with floating gate was 5.3A/W, which decreases to 0.13A/W with applied gate bias of -1V.

The results obtained in the simulations of OCFETs, are encouraging. This technology can be further exploited in conjunction with a waveguide scheme to realize a guided wave OCFET integrated on a Si chip. Further investigations and realization of complementary pair can be a framework to assess the impact of integration with Si photonics.

Integrating the OCFET to the on-chip optical interconnect system could be useful in surpassing the performance with traditional metal interconnects. Also in improving receiverless detection by comparing the speed and energy per bit to that of a conventional receiver circuits.

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List of Publications

1. V. Sorianello, L. Colace, S. Rajamani, and G. Assanto, Design and Simulation of Ge Based Optically Controlled Field Effect Transistor - Phys. Status Solidi C 11, No. 1, 81, (2014)
2. L. Colace, V. Sorianello, and S. Ramajani, Investigation of static and dynamic characteristics of optically controlled field effect transistor- Journal of Lightwave Technology, Vol.32, Issue 12, 2233, (2014)
3. Rajamani. S, Sorianello. V, De Iacovo. A, Colace. L, Simulations of Ge based optically controlled field effect transistors, IEEE 11th International Conference on Group IV photonics, Paris- 27-29, (Aug. 2014).
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