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Diamond lumped elements and multi-finger MESFETs

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To my parents,
my brothers
and Flavia

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Chapter 1

Introduction

During the last years, S2DEL lab of Roma Tre University has obtained remarkable results about a new technology development based on diamond substrate: this material is now used to manufacture electronic devices either for signal detector or amplification.

Just in this last area of interest we've manufactured an RF MESFET transistor with two fingers gate on polycrystalline diamond (See Figure 1.1), with DC and RF performances that have opened new possibilities. In fact we've fabricated devices with gate lengths L of 0.2 μm and f_T = 10.5 GHz f_{max} = 35 GHz.

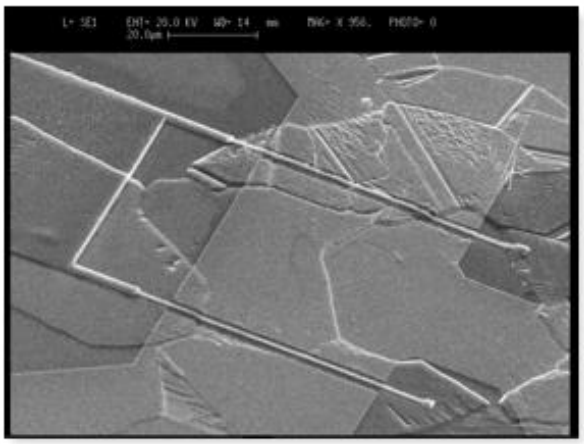
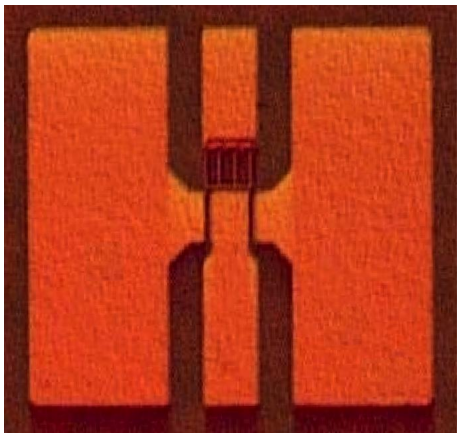
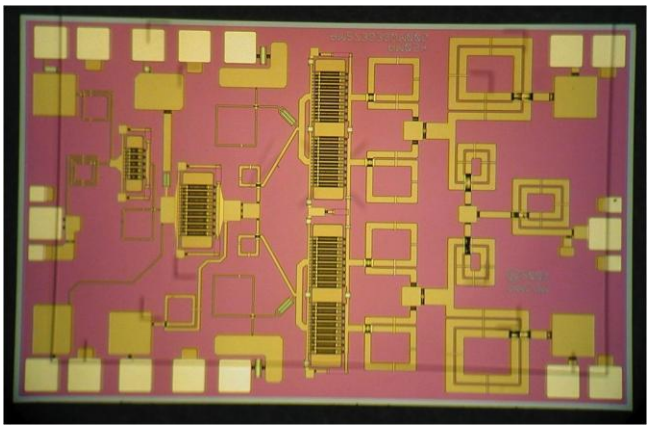


Figure 1.1 – Example of bi-finger RF MESFET transistor fabricated at S2DEL lab.

The doctorate research activity starting point is this bi-finger MESFET (see Figure 1.2a). With this work, parallel to the studying and development of this basic device, we've decided to move beyond this single active device and lay the technological foundations for a microwave monolithic integrated circuit (MMIC) (see Figure 1.2b).



(a)



(b)

Figure 1.2 – (a) Starting point: diamond bi-finger MESFET (b) Goal: diamond microwave monolithic integrated circuit MMIC.

In order to reach this important and challenging goal, we've focused our attention to the whole problem and then we've separated it in several macro-blocks, decomposable in basic elements, as shown in Figure 1.3. After that we've identified fundamental elements that compose single stages of an integrated circuit, which are inductors, capacitors, resistors and multi-finger transistors. Only after we learn manufacturing technology of these basic elements we could design and fabricate an MMIC. So the PhD work has been the study and processing of all the steps needed to manufacture passive elements and multi-fingers MESFETs on polycrystalline diamond substrate.

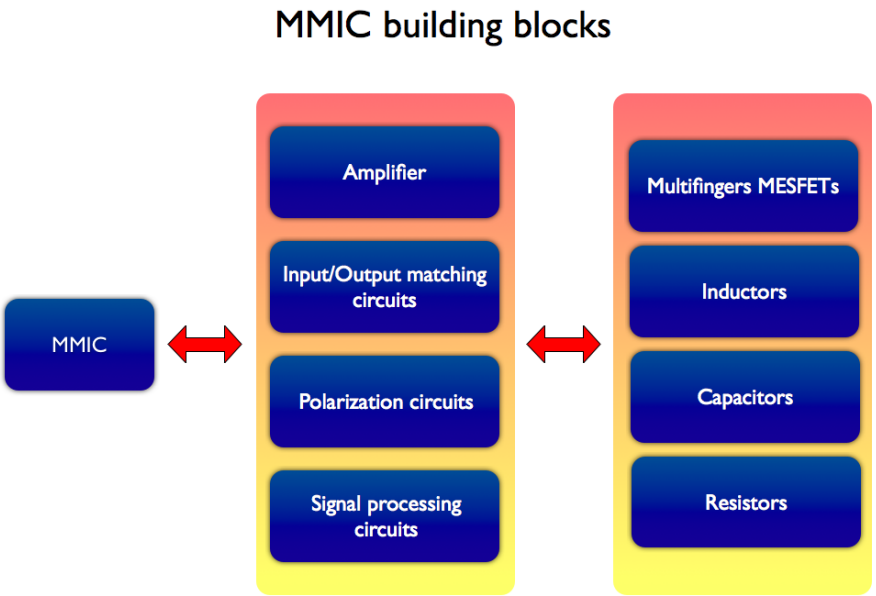


Figure 1.3 – MMIC basic building blocks and elements.

But what does the scientific community offer about it? A research made about these devices on a diamond substrate has product no results but we think that there is someone, in the world, that is working on these themes. For this reason the realization of this project could be bring our lab to assume a prime importance role on diamond technology and it should open new industrial horizons.

In the following, the doctorate thesis structure is shown (Figure 1.4). As far as passive elements concern, we started from a bibliographic study to understand how these devices worked and their manufacturing technique. After this we've designed devices layouts that are a trade off between manufacturing simplicity and performances. With the help of an electromagnetic simulator we've extrapolated the devices behaviour with frequency, using these designed layouts. Then we've manufactured process masks for optical lithography and applied and optimized all steps to devices building. First of all we decided to work using silicon substrates and then transfer the consequent technology on diamond ones, making appropriate modifications. The final step has been characterizing the devices with electrical measurements and compares them with simulations results.

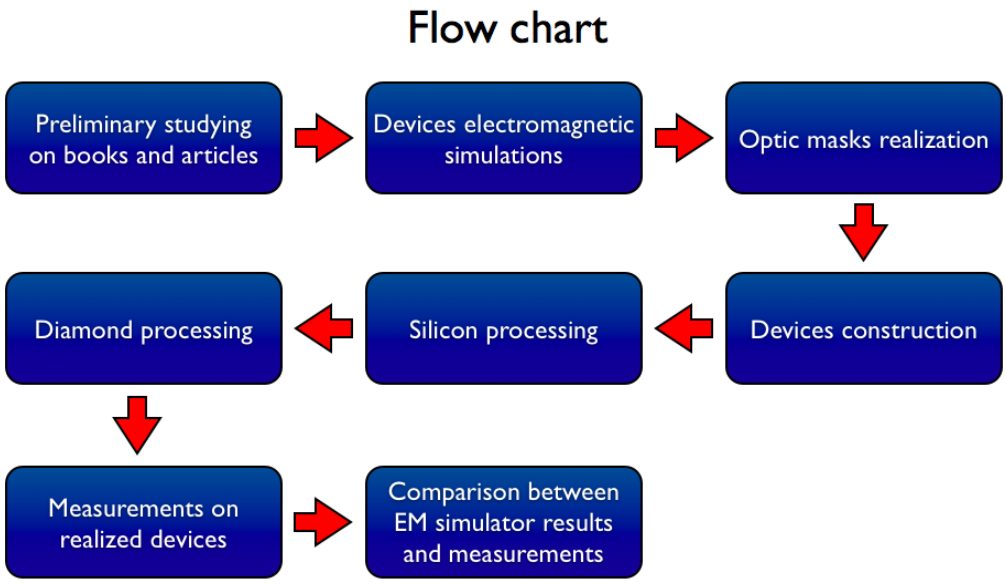


Figure 1.4 – Structure of the doctorate thesis. It's shown the flow chart followed to develop the project.

The fundamental element necessary to the development of these devices is a technological technique called "air-bridge" based on gold electroplating. So a large time has been spent to design basic steps and optimize them. As it's shown in Figure 1.5 the gold electroplating technique is used for the following reasons:

- Multi-turns inductors: the air-bridge is used to pass over the basic conductor and link the outer pad with the inner turn. In this way there isn't the cross between turns.
- Monolithic capacitors: the air-bridge is used to link the capacitor upper plate with the external circuitry or pad. In this way we avoid the short between plates.
- Multi-fingers MESFETs: in this case the air-bridge is used to link together all sources pad in order to permit the right parallel device working. In this case the bridge passes over two gate fingers and one drain pad.
- Contact thickening: as far as this last item concern we don't use the air bridge but only the gold electroplating (steps are the same). The increasing in thickness of contacts allows reducing sensitively the device pad resistance. For example increasing gate thickness we reduce the associated R_g that influence RF performances.

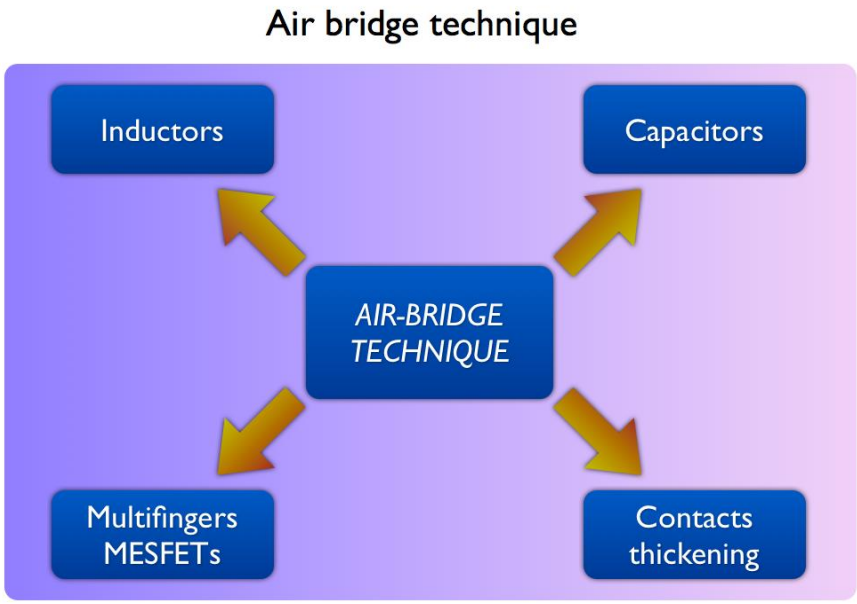


Figure 1.5 – Different use of air-bridge/gold plating technique.

Another item treated during the work has been the problem of RF measurements. In fact, at high frequencies, small parasitic elements can brought to sensitive mistakes on measurements. So we've developed an on wafer calibration kit (the technological part) to delete the parasitic effect from measurement results.

But what are lumped elements? A lumped element in microwave circuits is defined as a passive component whose size across any dimension is much smaller than the operating wavelength so that there is no appreciable phase shift between the input and output

terminals. Generally, keeping the maximum dimension less than λ/20 is a good approximation where λ is the guide wavelength. RF and microwave circuits use three basic lumped-element building blocks: capacitors, inductors and resistors.

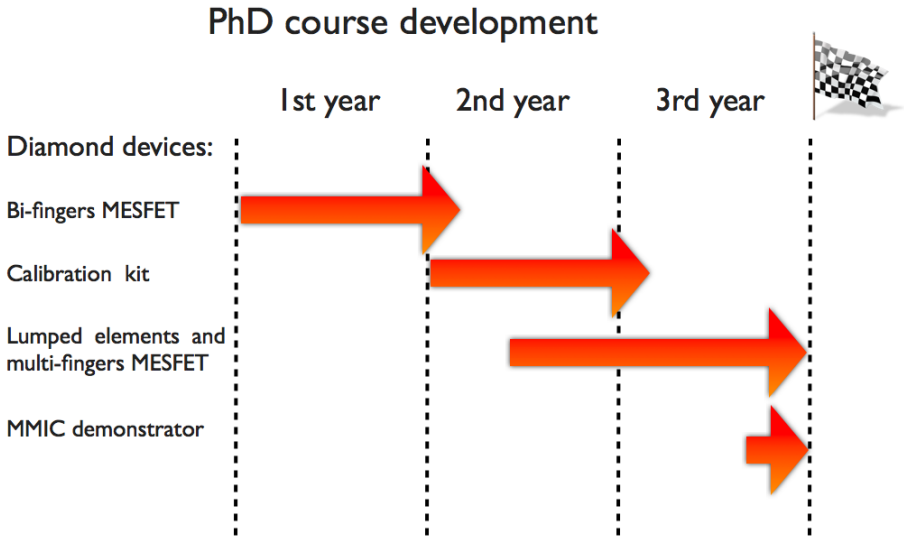


Figure 1.6 – Three years PhD course development.

Before entering into the research project details, in Figure 1.6 the three years structure of the work is shown. During the first year I've worked on two-finger gate diamond MESFETs, while during the second and third year I've focused my attention on passive elements, multi-finger MESFETs and RF calibration kit for the frequency analysis. The diamond MMIC technological demonstrator manufacturing is now in progress.

The contents of this work are divided into 9 chapters. After this introduction, in the second and third chapters a theory of printed inductors and monolithic capacitors is briefly discussed. Chapters four and five describe how we've manufactured either multi-finger MESFETs or passive elements while chapter six illustrates several technological problems we've handled. In chapter seven all experimental systems used during this thesis are shown. Chapter eight explains passive elements simulation results using SONNET electromagnetic simulator while in chapter nine we describe some results obtained for bi-fingers MESFETs and illustrate the first calibration kit constructed to allow an on-wafer calibration. At the end there are conclusions and future works.

Chapter 2

Printed inductors

Lumped-element design using inductors, capacitors and resistors is a key technique for reducing area resulting in more chips per wafer and thus lower cost. Below C-band frequencies, MMICs using lumped inductors are an order of magnitude smaller than ICs using distributed matching elements such as microstrip lines or coplanar waveguides. Inductors in MICs are fabricated using standard integrated circuit processing without any additional process steps. The innermost turn of the inductor is connected to other circuitry using a wire bond connection in conventional hybrid MICs, or through a conductor that passes under air-bridges in multilayer MIC and MMIC technologies. The width and thickness of the conductor determines the current-carrying capacity of the inductor. In MMICs the bottom conductor's thickness is typically 0.5 to 1.0 μm, and the air-bridge separates it from the upper conductors by 1.5 to 3.0 μm. Typical inductance values for MMICs working above L-band are in the range of 0.5 to 20 nH.

2.1 Inductor configurations

Inductors can be realized in one of the following three forms: a small section of a strip conductor or a wire. a single loop or a spiral (see Figures 2.1 a,b,c). The printed microstrip section inductor is used for low inductance values, typically less than 2 nH and often meandered to reduce the component's size. Printed circuit single-loop inductors are not as popular as their coil versions due to their limited inductance per unit area. The spiral/coil type are the most popular type of inductors. The coil inductors may be printed or wire wound. Both can take a rectangular or circular shape. The circular geometry is superior in electrical performance, whereas the rectangular shapes are easier to lay out.

Table 2.1 summarizes the major advantages and disadvantages of each shape. The circular geometry has the best electrical performance, whereas meander line inductors are seldom

used. It has been reported [1, 2] that the circular geometry has about 10% to 20% higher *Q*-values and f_{res} values than the square configuration.

Configuration	Advantage	Disadvantage
Meander line	**Lower eddy current resistance**	**Lowest inductance and SRF**
Rectangular	**Easy layout**	**Lower SRF**
Octagonal	**Higher SRF**	**Difficult layout**
Circular	**Highest SRF**	**Difficult layout**

Table 2.1 - Two-dimensional inductor configurations and their features

Printed inductors are fabricated by using thin- or thick-film fabrication processes or using monolithic Si and GaAs-based IC technologies. The inner connection is pulled out to connect with other circuitry through a gold wire or by using a multilevel crossover metal strip.

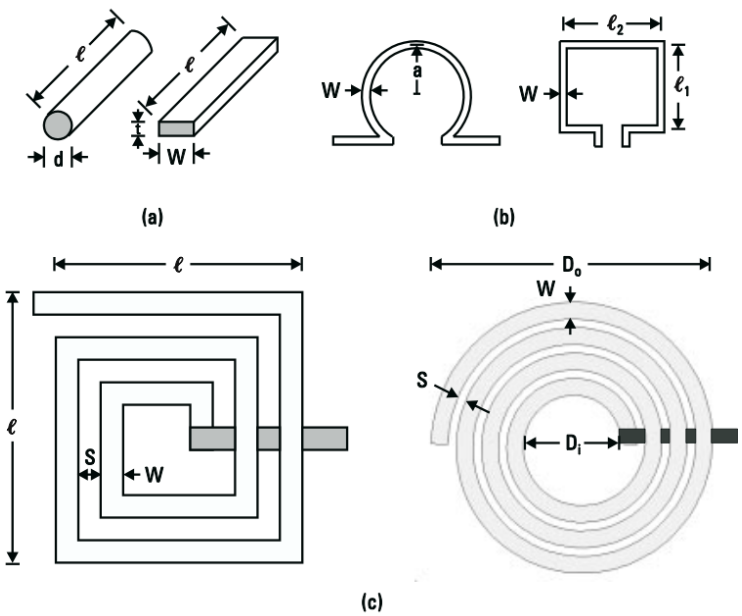


Figure 2.1 - Inductor configurations: (a) bond wire and strip sections, (b) circular and rectangular loops, and (c) rectangular and circular spirals.

The design of coil inductors it's quite complex because there are a lot of parameters that influence device behavior. The selection of physical dimensions, such as the number of turns (*n*), the trace width (*W*), the trace thickness (*t*), line spacing (*S*), and the inner diameter (D_i) as shown in Figure 2.2(a), determines the excitation of eddy currents responsible for extra loss in the conductor as well as in the substrate. The loss in an

inductor can be divided into two components; conductor loss and substrate loss. These losses are discussed next.

The design of spiral inductors can be based on analytical expressions or EM simulations or measurement-derived EC models. Usually, inductors for MMIC applications are designed either using EM simulators or measurement-based EC models.

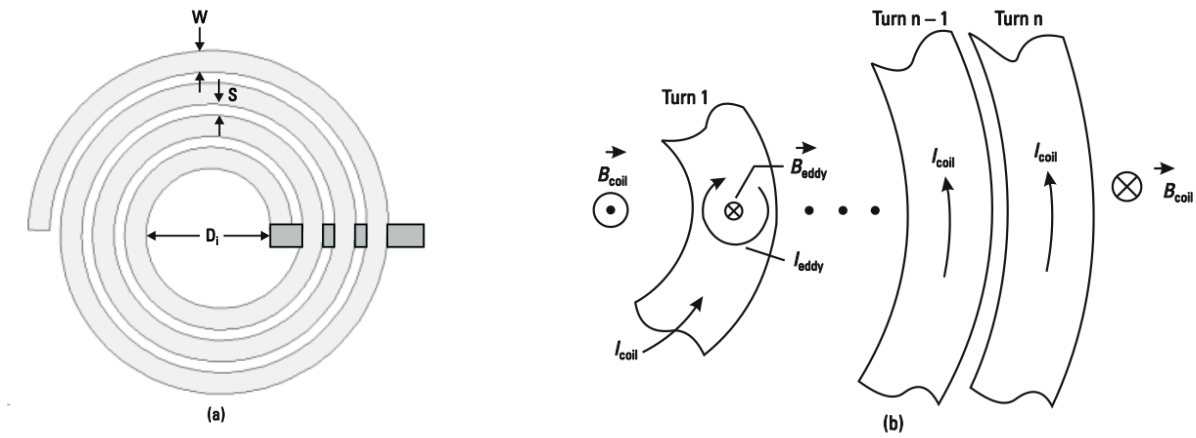


Figure 2.2 - (a) A 3.5-turn circular inductor with dimensions. (b) Excitation and eddy currents, and fields in a coil. I coil the excitation current.

2.2 Conductor Loss

The conductor loss in an inductor is proportional to its series resistance. At low frequencies, the series resistance can be calculated from the conductor sheet resistance multiplied by the number of squares of the conductor. However, at microwave frequencies, the series resistance becomes a complex function due to the skin effect and magnetically induced currents (eddy currents). The series resistance increases significantly at higher frequencies due to eddy currents. Eddy currents produce non-uniform current flow in the inner portion of spiral inductors, with much higher current density on the inner side of the conductor than on the outer side. These two components of conductor loss are briefly discussed in the following sections.

2.2.1 Sheet Resistance

The dc sheet resistance of a spiral coil can be reduced by using a thicker metallization. Several available thin metal layers can be connected or shunted together through via holes

to realize a thick metal layer or a thicker plated conductor can be used. Alternatively, high-conductivity conductors such as copper or gold can be used. At low frequencies, the total dc resistance of the coil is given by

$$R_{dc} = \frac{l}{Wt\sigma} \tag{2.1}$$

where W is the width, t is the thickness, l is the total length of the conductor strip in the coil, and σ is the conductivity of the conductor material. At high frequencies, the above equation is modified and given as

$$R_{rf} = \frac{l}{W\sigma\delta(1-e^{-t/\delta})} \tag{2.2}$$

where δ is the skin depth given by

$$\delta = \sqrt{\frac{2}{\omega\mu\sigma}} \tag{2.3}$$

where μ is the magnetic permeability of the material. Because Si technologies use thin conductors $\cong$ 1 to 2 μm thick, at RF frequencies, $t/\delta < 1$, $R_{rf} \cong R_{dc}$. Table 2.2 compares conductivities and skin depth of various metals used. Silver has the maximum conductivity.

Metal	Conductivity	Resistivity	Skin Depth	
	(10^5 Ω-cm)	**(10^{-6} Ω-cm)**	**@1 GHz**	**@10 GHz**
Aluminum (Al)	3.8	2.6	2.57	0.81
Gold (Au)	4.1	2.4	2.50	0.79
Copper (Cu)	5.8	1.7	2.09	0.66
Silver (Ag)	6.2	1.6	2.02	0.64

Table 2.2 - Conductivity, Resistivity, and Skin Depth Values of Commonly Used Metals

2.2.2 Eddy Current Resistance

The eddy current resistance in the inductor trace is a result of current crowding, that is, increasing current density along a part of the trace width. Consider a sector of an n-turn circular spiral inductor as shown in Figure 2.2(b). The inductor carries a current I_{coil} and the associated magnetic flux is B_{coil}. The magnetic flux lines enter the page plane at the far end of the turn n and come out of the page plane in the center of the coil, where they have maximum intensity. When there is not enough hollow space in the center of the coil, a large part of the magnetic flux also goes through the inner turns. According to Faraday-Lenz's

law, when a conductor is moved into a magnetic field or a conductor is placed in a time-varying magnetic field, eddy currents are induced in the conductor in the direction where their self-flux is opposite to the applied magnetic field. Thus, as shown in Figure 2.2(b), circular eddy currents I_{eddy} are generated due to magnetic fields that go through the inner turns, and an opposing magnetic field B_{eddy} due to eddy currents is established.

The eddy current loops produced within the trace width cause no uniform current flow in the inner coil turns. They add to the excitation current I_{coil} on the inside edge and subtract from the excitation current I_{coil} on the outside edge. Therefore, the inside edges of the coil carry current densities much larger than the outside edges, giving rise to a larger effective resistance compared to the case of uniform current flow throughout the trace width. Because the eddy currents are induced due to time-varying magnetic fields, their values are a strong function of frequency. The critical frequency f_c at which the current crowding begins to become significant is given by [3]

$$f_c = \frac{3.1(W+S)}{2\pi\mu_0 W^2} R_{sh} \qquad (2.4)$$

where μ_0 is the free-space permeability and R_{sh} is the sheet resistance of the trace. An approximate expression for the series resistance is given by [3]

$$R_s = R_{dc}\left[1 + 0.1\left(f / f_c\right)^2\right] \qquad (2.5)$$

The excitation of eddy currents can be minimized by cutting longitudinal slits in the inner turns' conductors or making the inner turns narrower and the outer turns wider. Because the contribution of the inner turns to the inductor's inductance is low because of its small area, removing them altogether or using a ''hollow'' coil reduces the effect of eddy currents.

An inductor's loss depends on the geometry of the inductor, metal conductivity, substrate resistivity, and frequency of operation. Metal losses dominate at low frequencies, whereas substrate losses are critical at high frequencies.

2.3 Substrate Loss

A major drawback of inductors on high conductivity substrates (as intrinsic or heavily doped silicon) is the extra substrate resistive losses due to low resistivity of the substrates. The substrate loss consists of two parts: finite resistance due to electrically induced conductive and displacement currents, and magnetically induced eddy current resistance. These losses are known as capacitive and magnetic, respectively.

2.3.1 Capacitive Loss

When a coil is excited, a voltage difference occurs between the conductor and the grounded substrate that gives rise to capacitive coupling between the conductors. If the substrate is an insulator (i.e., very high resistivity – as the diamond case) with a very low loss tangent value, the ohmic loss in the dielectric is negligible. In low-resistivity substrates, the skin depth becomes on the order of the substrate thickness, giving rise to higher ohmic losses. Because this loss is coupled through the shunt capacitance, it is also commonly referred to as capacitive or electric substrate loss. Finite resistivity loss can be minimized by using very high resistivity substrates.

2.3.2 Magnetic Loss

In high conductivity substrates, currents induced by the penetration of the magnetic fields of the inductor into the substrate cause extra resistive loss. Consider Figure 2.3, which shows magnetic field flux lines associated with the coil excitation current. The flux lines uniformly surround the inductor and penetrate into the substrate. As discussed previously, due to the Faraday-Lenz law, loops of eddy currents I_{sub} flow in the low-resistivity substrate underneath the coil, with higher current density closer to the coil. The direction of I_{sub} is opposite to the direction of I_{coil}, giving rise to extra substrate loss. Because this loss is associated with magnetic fields, it is commonly referred to as magnetic or inductive substrate loss. Substrates with high resistivity have negligible magnetic loss (as the diamond case).

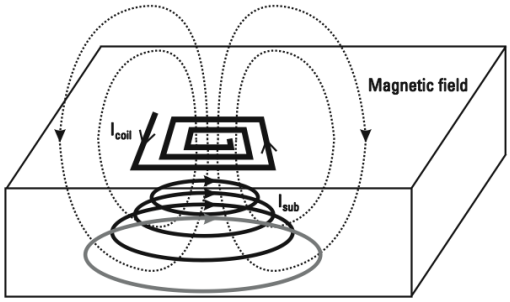


Figure 2.3 - Currents and fields in a coil printed on a lossy Si substrate.

In summary, by using narrow conductors that meet skin effect requirements ($W \cong 3\delta$) in the inner turns, using a hollow coil design, and using compact area coils, one can keep the substrate loss to a minimum. Because the magnetic field in a small coil penetrates less deeply into the substrate, eddy current loss is not severe as for large coils. Therefore, an optimum solution, in terms of inside dimensions and coil area for a given substrate, can be found.

2.4 Quality Factor

Several different definitions of Q-factors for inductors have been used in the literature [4–5]. The most general definition of Q is based on ratio of energy stored, W_S, to power dissipated, P_D, in the inductor per cycle; that is

$$Q = \frac{\omega W_S}{P_D} \tag{2.6}$$

At low frequencies an inductor's primary reactance is inductive and

$$Q = \frac{\omega \frac{1}{2} L i_0^2}{\frac{1}{2} R i_0^2} = \frac{\omega L}{R} \tag{2.7}$$

where i_0 is the rms value of the current. When the inductor is used as a resonant component close to its *self-resonance frequency* (SRF) f_{res}, a more appropriate definition of the Q-factor is in terms of its 3-dB bandwidth (BW) is given by

$$Q = \frac{f_{res}}{BW} \tag{2.8}$$

A third definition of Q-factor, which has been used for distributed resonators, is evaluated from the rate of change of input reactance with frequency [6, 7]:

$$Q = \frac{f_{res}}{2R}\left[\frac{dX_{in}}{df}\right] \tag{2.9}$$

where X_{in} is the input reactance of the inductor and dX_{in}/df is determined at f_{res}. In microwave circuits where the inductors are used far below the self-resonance frequency, the degree at which the inductor deviates from an ideal component is described by the effective quality factor Q_{eff}, expressed as [5]:

$$Q_{eff} = \frac{\mathrm{Im}[Z_{in}]}{\mathrm{Re}[Z_{in}]} = \frac{X}{R} = \frac{\omega L_e}{R} \tag{2.10}$$

where $Re[Z_{in}]$ and $Im[Z_{in}]$ are the real and imaginary parts of the input impedance of the inductor, respectively. This definition leads to the unusual condition that Q_{eff} becomes zero at resonance. Since in RF and microwave circuits, for series applications of inductors, the operating frequencies are well below the self-resonance frequency, the preceding definition is traditionally accepted.

2.5 Self-Resonant Frequency

The self-resonant frequency *(f_{res})* of an inductor is determined when $Im[Z_{in}] = 0$; that is, the inductive reactance and the parasitic capacitive reactance become equal and opposite in sign. At this point, $Re[Z_{in}]$ is maximum due to parallel resonance and the angle of Z in changes sign. The inductor's first resonant frequency is of the parallel resonance type. Beyond the resonant frequency, the inductor becomes capacitive.

2.6 Inductor Models

An inductor is characterized by its inductance value, the unloaded quality factor Q, and its resonant frequency f_{res}. Figure 2.4 shows various EC models used to describe the characteristics of GaAs inductors. Figure 2.4(a) represents the simplest model, whereas a comprehensive model for larger inductance values is shown in Figure 2.4(d). As starting point we refer to GaAs model to describe parameters because it should be quite similar to diamond: using diamond we expect negligible substrate losses thanks to its higher resistivity value.

A commonly used EC model is shown in Figure 2.4(b) and an accurate account of substrate loss is represented in a model shown in Figure 2.4(c). In all of these models, the series inductance is represented by L, R_s accounts for the total loss in the inductor, C_p is the fringing capacitance between inductor turns, and $C_{ga,b}$ represents shunt capacitances between the trace and the substrate.

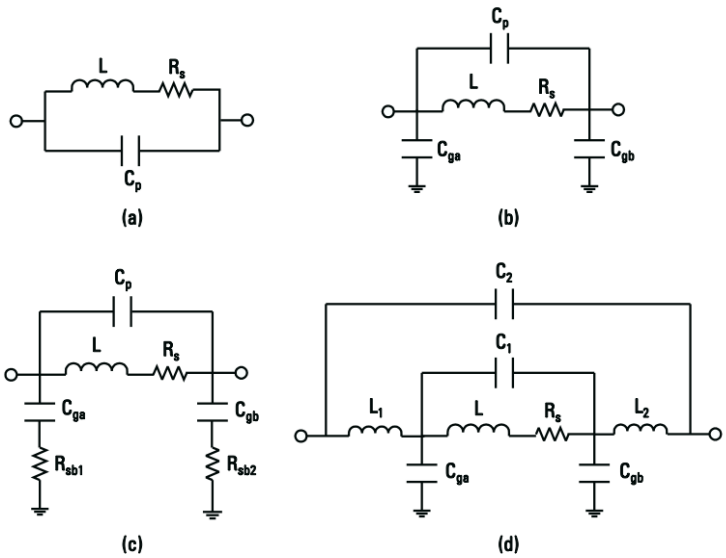


Figure 2.4 - (a–d) Lumped-element EC models of the inductor on GaAs substrate.

The two-port lumped-element EC model used to characterize inductors in this section is shown in Figure 2.4(d). The series resistance R_s used to model the dissipative loss is given by

$$R_S = R_{dc} + R_{ac}\sqrt{f} + R_d f \qquad (2.11)$$

where R_{dc} represents dc resistance of the trace, and R_{ac} and R_d model resistances due to skin effect, eddy current excitation, and dielectric loss in the substrate.

In the model L_t ($L + L_1 + L_2$), R_s and the C'_s represent the total inductance, series resistance, and parasitic capacitances of the inductor, respectively. The frequency f is expressed in gigahertz.

In microwave circuits, the quality of an inductor is represented by its effective quality factor Q_{eff} and calculated using (2.10). The Q_{eff} values were obtained by converting two-port S-parameters data into one-port S-parameters by placing a perfect short at the output port. In this case, the following relationships are used to calculate the quality factor and f_{res}:

$$\Gamma_{in} = S_{11} - \frac{S_{12}S_{21}}{1 + S_{22}} \qquad (2.12)$$

$$Z_{in} = 50\frac{1 - \Gamma_{in}}{1 + \Gamma_{in}} = R + jX(\Omega) \qquad (2.13)$$

The self-resonant frequency (f_{res}) of an inductor is calculated by setting Im [Z_{in}] = 0; that is, the inductive reactance and the parasitic capacitive reactance become equal. At this point, Re [Z_{in}] is maximum and the angle of Z_{in} changes sign. The inductor's first resonance frequency is of the parallel resonance type. Beyond the resonant frequency, the inductor becomes capacitive.

2.7 Figure of Merit

For a given inductance value, one would like to have the highest possible Q_{eff} and f_{res} in the smallest possible area. In an inductor, changing W, S, and the inner diameter affects its area and so it is difficult to make a good comparison. Here we define a unique *figure of merit of an inductor* (FMI) as follows [5]:

$$FMI = Q_{res} \cdot f_{res} / inductor - area \qquad (2.14)$$

Thus, the highest FMI value is desirable.

2.8 Basic parameters in the coils design

We've just told that the selection of physical dimensions, such as the number of turns (*n*), the trace width (*W*), the trace thickness (*t*), line spacing (*S*), and the inner diameter (D_i) and the inductor area influence in different ways the behavior of device. In the next paragraphs some GaAs examples are shown to demonstrate how these parameters are very critical. We take GaAs inductors as our reference because GaAs technologies are quite the same of diamond ones and we expect a similar beahviour between GaAs and Diamond devices.

Line Width: The line width is the most critical variable in the design of coils. In general, Qeff increases due to lower dc resistance and fres decreases due to higher parasitic capacitance with the increase in the line width. Figures 2.5 shows the variations of Qeff, fres, and inductor area for 1-nH inductance values, for W = 8, 12, 16, 20 μm, S = 8 μm, Di = 50 μm, and the number of turns is selected for the desired L value.

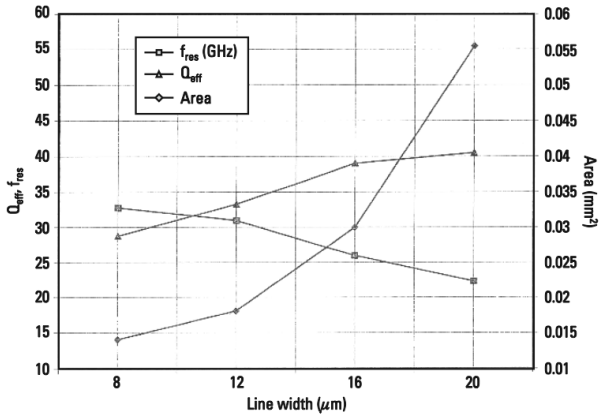


Figure 2.5 Inductor's Q_{eff}, f_{res} and area as a function of line width for a (a) 1-nH inductance value.

The effect of eddy currents can be minimized by making the line widths of the inner turns of the inductor narrower than the outer turns [8]. Narrower line widths have higher dc resistance; however, this is compensated by using wider line widths in the outer turns. This structure is shown in Figure 2.6. In this structure the improvement in Q-value is more pronounced at higher than lower frequencies, because the effect of eddy currents is more severe at high frequencies.

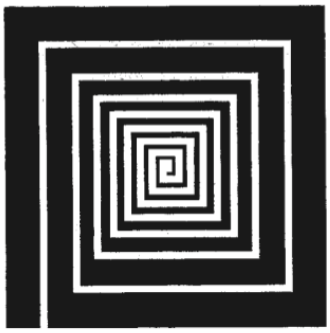


Figure 2.6 - Variable width layout of an inductor.

Spacing Between Turns: In general, Q_{eff} increases with the area of an inductor. However, small area inductors mandate small separation between the turns. Table 2.3 shows inductor parameters for 8- and 14-μm spacing. As expected a 3.5I0A inductor has a slightly higher inductance and lower f_{res} than the 3.5I4A one due to increased area. Because the 3.5I0A inductor has higher inductance and lower f_{res}, its Q_{eff} is expected to be higher than the 3.5I4A inductor's Q_{eff}. For spiral coils, $W/S > 1$ is recommended.

Inductor Parameters for Several Inductors Fabricated Using a Multilevel MMIC Process on 75-μm-Thick GaAs Substrate

Inductor Number	Width (μm)	Spacing (μm)	L_t (nH)	f_{res} (GHz)	Peak Q_{eff}
1.5I4A	12	8	0.342	>40	41.5
2.5I4A	12	8	0.808	34.2	35
3.5I4A	12	8	1.593	20.5	30
3.7I4A*	12	8	1.82	18.0	29
3.5I0A	12	14	1.82	18.7	30
3.5I1A	12	14	2.63	14.0	31.5
3.5I2A	12	14	3.63	10.6	29.5
3.5I3A	12	14	4.59	8.75	27.5

Table 2.3 - Inductor parameters for several inductors fabricated using a Multilevel MMIC Process on 75-μm-Thick GaAs substrate .

Inner diameter: Because the contribution of the innermost turn is small due to its very small inner diameter, enough empty space must be left in the center of a coil to allow the magnetic flux lines to pass through it in order to increase the stored energy per unit length. Inductors with four different inner diameters (50, 108, 158, and 210 μm) were studied. Figures 2.7 shows the variations of L_t, Q_{eff} and f_{res} as a function of inner diameter for W = 20 μm, S = 8 μm, n = 1.5, and W = 12 μm, S = 14 μm, n = 3.5, respectively. As expected, the

inductance increases and f_{res} decreases with increasing inner diameter (D_i) due to increased inductor area. As can be seen, the maximum Q_{eff} occurs around D_i = 100 μm.

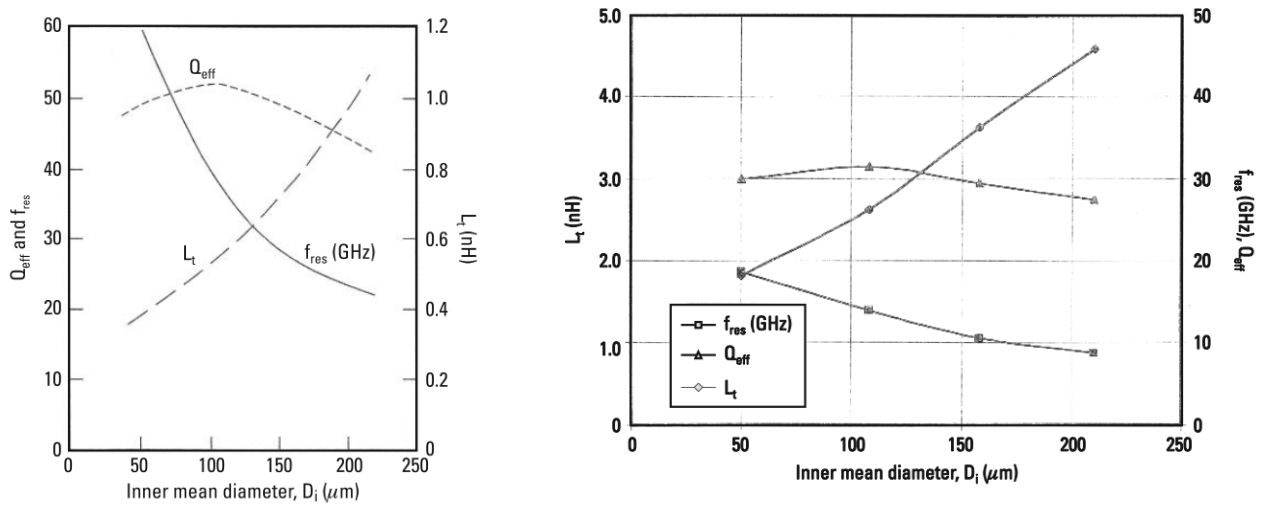


Figure 2.7 - Inductor's L_t, Q_{eff}, and f_{res} versus inner mean diameter for (a) 1.5-turn and (b) 3.5-turn inductors.

Number of turns: Multi-turn inductors have higher inductance per unit area, but due to higher parasitic capacitances, have lower-self-resonance frequencies. Figure 2.8 (a) shows the plots of L_t, Q_{eff}, and f_{res} versus number of turns for GaAs inductors (D_i=50 μm, W=S=8 μm).

The decrease of Q_{eff} with an increasing number of turns is because of increased parasitic capacitance and increased RF resistance due to eddy currents. Figures 2.8 (b) and (c) show typical variations of inductance and Q_{eff} as a function of frequency for 1.5-, 2.5-, 3.5-, 4.5-, and 5.5-turn inductors. Data are shown up to the first resonance. The maximum Q_{eff} point decreases with the increase in number of turns because of increased RF resistance due to eddy currents and the increase of parasitic capacitance. Below the maximum Q_{eff} point, the inductive reactance and Q_{eff} increase with frequency, while at frequencies above the maximum Q_{eff} point, the RF resistance increases faster than the inductive component. This results in a decrease in the Q_{eff} value with frequency, and Q_{eff} becomes zero at resonance of the inductor. As expected, the inductance increases approximately as n^2, where n is the number of turns.

Thickness effect: The Q-factor of an inductor is increased by increasing the conductor thickness because this reduces the series resistance. Moreover the metal 2 increasing thickness increases the current handling.

Inductor area: The *Q*-factor of a coil can be enhanced by increasing its area using either a larger inside diameter or wider line dimensions or by increasing the separation between the turns. In general, using a wider line dimension reduces the dc resistance of the coil. However, the parasitic capacitance of the inductor trace and the RF resistance due to eddy currents increase with the line width. This sets a maximum limit for the line width. However, for low-cost considerations one needs compact inductors.

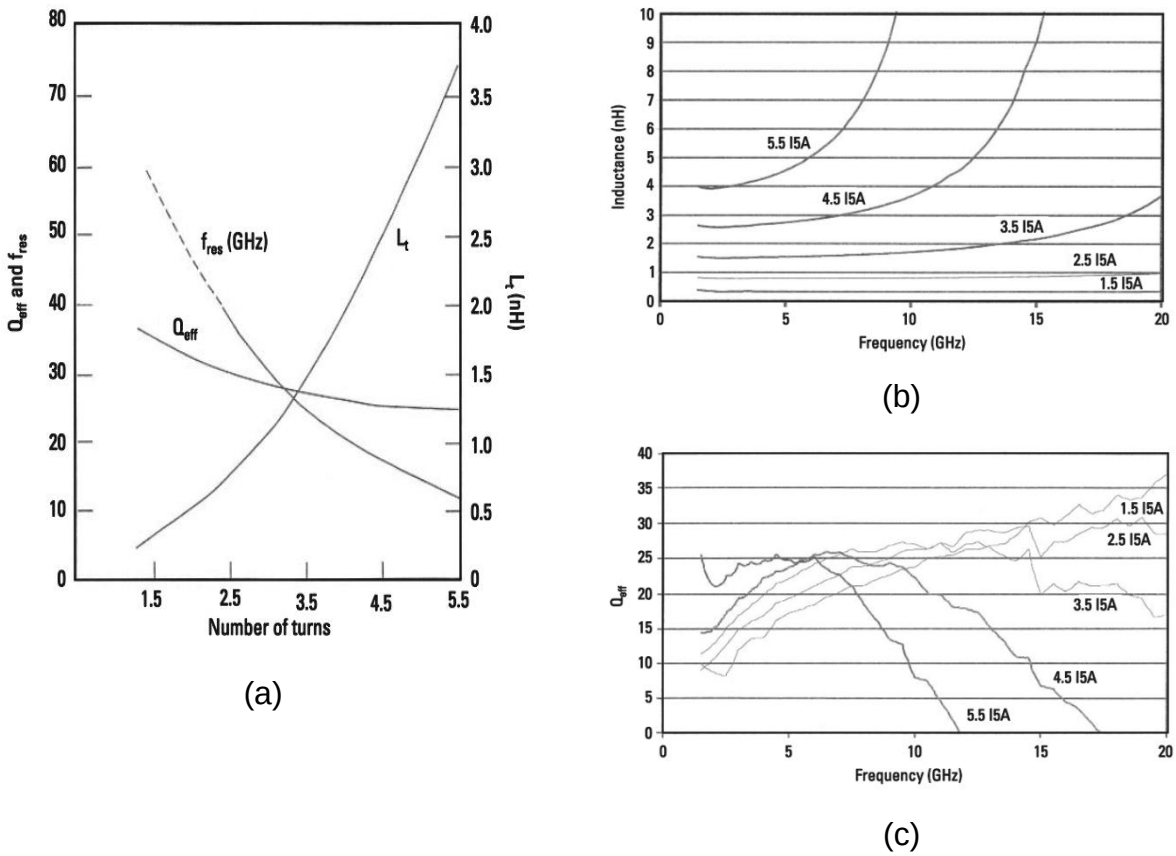


Figure 2.8 – (a) Variations of L_t,, Q_{eff}, and f_{res} area as a function of number of turns for GaAs inductors (b) Typical variations of L_t, versus frequency for different inductor turns (c)Typical variations of Q_{eff} factor versus frequency for different inductor turns.

Chapter 3

Monolithic capacitors

3.1 Introduction

Capacitance is defined as the ability to store energy in an electric field between two electrodes or efficiency of the structure in storing a charge when voltage difference exists between the plates. Its value depends on the area of electrodes, separation between them, and the dielectric material in between. Dielectrics with high values of permittivity and higher breakdown voltage are the most desirable. The capacitance C, in Farads, of a capacitor structure consisting of two conductors is expressed as:

$$C = \frac{Q}{V} \qquad (3.1)$$

where Q is the total charge in Coulombs on each electrode or conductor and V is the voltage between the two conductors in Volts. The basic structure of a capacitor as shown in Figure 3.1 consists of two parallel plates also called electrodes, each of area A and separated by an insulator or dielectric material of thickness d and permittivity $\varepsilon_0\varepsilon_{rd}$, where ε_0 and ε_{rd} are free-space permittivity and relative dielectric constant, respectively.

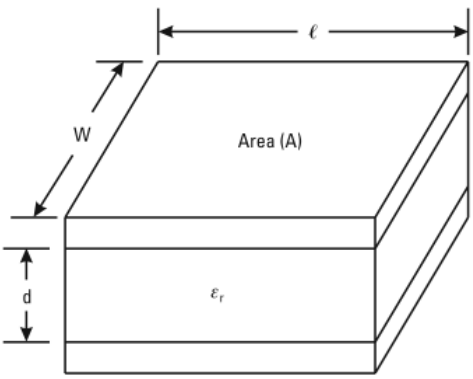


Figure 3.1 - Basic parallel plate capacitor configuration.

From 3.1 and the Gauss's law we obtain:

$$C = e_0 e_r \frac{A}{d} = e_0 e_r \frac{W \times l}{d} \qquad (3.2)$$

where W and l are the width and length of one of the plates. Equation (3.2) does not include the effect of fringing field. Equation (3.2) can be expressed in commonly used units as follows:

$$C = 8.85 \times 10^{-6} e_r \frac{W \times l}{d} \text{ (pF), } W, l, \text{ and } d \text{ in microns} \qquad (3.3)$$

Monolithic or integrated capacitors (Figure 3.1) are classified into three categories: microstrip, interdigital, and metal–insulator–metal (MIM). A small length of an open-circuited microstrip section can be used as a lumped capacitor with a low capacitance value per unit area due to thick substrates. The interdigital geometry has applications where one needs moderate capacitance values. Both microstrip and interdigital configurations are fabricated using conventional MIC techniques. MIM capacitors are fabricated using a multilevel process and provide the largest capacitance value per unit area because of a very thin dielectric layer sandwiched between two electrodes.

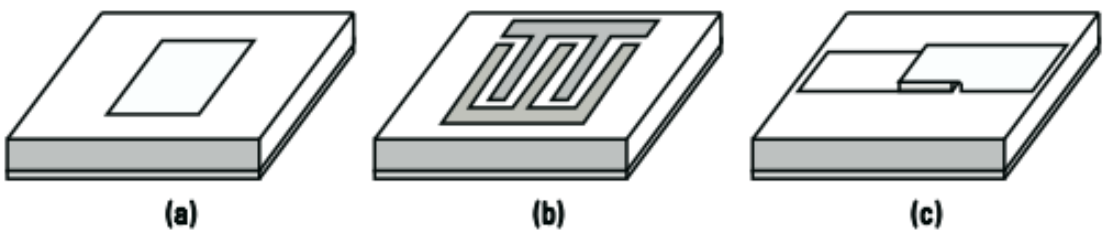


Figure 3.1 - Monolithic capacitor configurations: (a) microstrip, (b) interdigital, and (c) MIM.

Monolithic MIM capacitors are integrated components of any MMIC process and are constructed using a thin layer of a low-loss dielectric between two metals. The bottom plate of the capacitor uses first metal, a thin unplated metal, and typically the dielectric material is silicon nitride (Si_3N_4) for ICs on GaAs and SiO_2 for ICs on Si. The top plate uses a thick plated conductor to reduce the loss in the capacitor. The bottom plate and the top plate have typical sheet resistances of 0.06 and 0.007 Ω/square, respectively, and a typical dielectric thickness is 0.2 μm. The dielectric constant of silicon nitride is about 6.8, which yields a capacitance of ≅ 300 pF/mm^2. The top plate is generally connected to other circuitry by using an airbridge or dielectric crossover, which provides higher breakdown voltages.

Among various possible MIM capacitor shapes, rectangular, circular, and octagonal

geometries are used, but the rectangular geometry is the most popular. Table 3.1 lists plate areas of several possible geometries for the parallel-plate monolithic capacitors.

Dimensions					***Area***
Geometry	*Width*	*Length*	*Side*	*Radius*	*A*
Square	*W*	*W*			*WxW*
Rectangle	*W*	*l*			*Wxl*
Circle				*r*	πr^2
Regular polygon			*a*		$\frac{1}{4}na^2\cot(180°/n)$, where n is the number of sides
Parallelogram	*W*	*l*			$Wxl \sin\theta$, where θ is the angle between sides W and l
Triangle			*a,b*		$\frac{1}{2}axb\sin\theta$, where θ is the angle between sides a and b

Table 3.1 - Surface Area of Various Geometries

Rectangular Capacitors**.** The rectangular shape is the most popular because its layout is easy to draw, area calculations are simple, and connections are straightforward. One of the major problems with this geometry is the higher ESD failure due to sharp corners. Noncolinear connections have higher discontinuity reactances at higher microwave frequencies.

Circular Capacitors. Circular capacitors are seldom used due to the higher complexity of their layout and their connections to other circuitry, especially wide lines. Because such configurations do not have sharp corners, ESD failures are lower compared to other geometries.

Octagonal Capacitors**.** When MIM capacitors are used in MMICs, generally two or more connections are made between the capacitors and other circuitry. Flexibility and compactness of the circuit layout mandate these connections to be made anywhere along the periphery of the capacitors. In such situations, any connection made off the straight path (noncolinear) at defined ports or connections made at right angles add extra reactances due to discontinuities in the current path in the circuit, which in turn degrade the MMIC performance. An octagonal MIM capacitor (Figure 3.2) structure for MMIC applications has the flexibility of multiport connections with minimum added discontinuity reactances [10], and also has much lower ESD failure due to tapered corners.

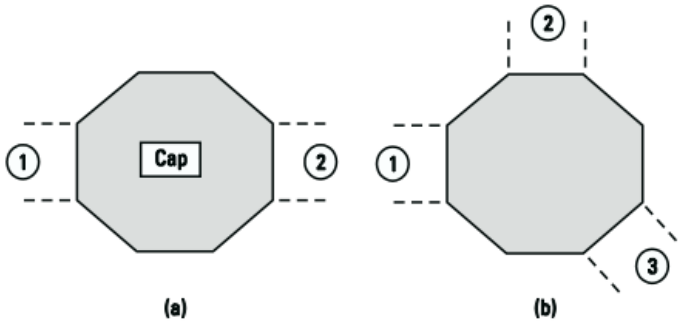


Figure 3.2 - (a, b) Octagonal MIM capacitor showing flexibility in multiport connections.

Advantages of this structure as compared to rectangular or square capacitors are as follows:

1. Chamfered corners reduce step discontinuity reactance between the feed line and the capacitor, which improves frequency performance of the MMICs.
2. Reduced bend discontinuity reactance for noncolinear feed points also improves frequency performance of the MMICs.
3. Provides more than four ports (eight total) for interconnections. When ICs require more than four ports for matching networks, it provides an ideal situation with reduced discontinuity reactances.

This structure in general has better performance at millimeter-wave frequencies compared to conventional rectangular-shaped capacitors.

3.2 Capacitor parameters

When selecting a capacitor, one should consider several of its parameters. Hereafter a lot of these parameters are described.

3.2.1 Effective Capacitance

For chip capacitors, the nominal capacitance value is measured at 1 MHz and in typical RF applications the operating frequency is much higher. Because the capacitor has an associated parasitic series inductance as shown in Figure 3.3(a), the impedance of the capacitance (neglecting series resistance) can be written

$$Z_c = j\left[\omega L_s - \frac{1}{\omega C}\right] = -\frac{j}{\omega C}\left[1 - \omega^2 L_s C\right] \qquad (3.4)$$

or

$$Z_c = -\frac{j}{\omega C_e} \qquad (3.5)$$

where

$$C_e = C\left[1-\omega^2 L_s C\right]^{-1} = C\left[1-\left(\omega/\omega_s\right)^2\right]^{-1} \qquad (3.6)$$

Here ω_S is the series resonant frequency $\left(=1/\sqrt{L_s C}\right)$. The equivalent capacitance C_e is known as the *effective capacitance* and below the resonance frequency, its value is generally greater than the nominal specified value.

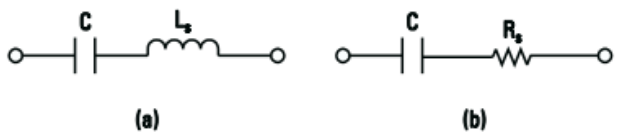


Figure 3.3 - (a, b) Series representations of a capacitor.

3.2.2 Quality Factor

Quality factor is an important FOM for capacitors and measures the capacitor's capability to store energy. When a capacitor is represented by a series combination of capacitance C and resistance R_S as shown in Figure 3.3(b), the quality factor, Q is defined by the following relation:

$$Q = \frac{1}{wCR_s} = \frac{1}{2pfCR_s} \qquad (3.7)$$

where $\omega = 2\pi f$, and f is the operating frequency. For discrete capacitors, the value of Q is typically measured at low frequencies. Figure 3.4(a) shows typical measured Q values of ATC series 180, case R chip capacitors. For a 22-pF capacitor, the Q is greater than 100 at 1 GHz [9].

3.2.3 Equivalent Series Resistance

All capacitors exhibit parasitic inductance due to their finite size and series resistance due to contact and electrode resistance. This series resistance is commonly known as ESR, and is an important parameter in circuit design using capacitors. Figure 3.4(b) shows typical measured ESR values for ATC series 180, case R chip capacitors. For a 22-pF capacitor, the ESR value is about 0.05 ohm at 1 GHz [9].

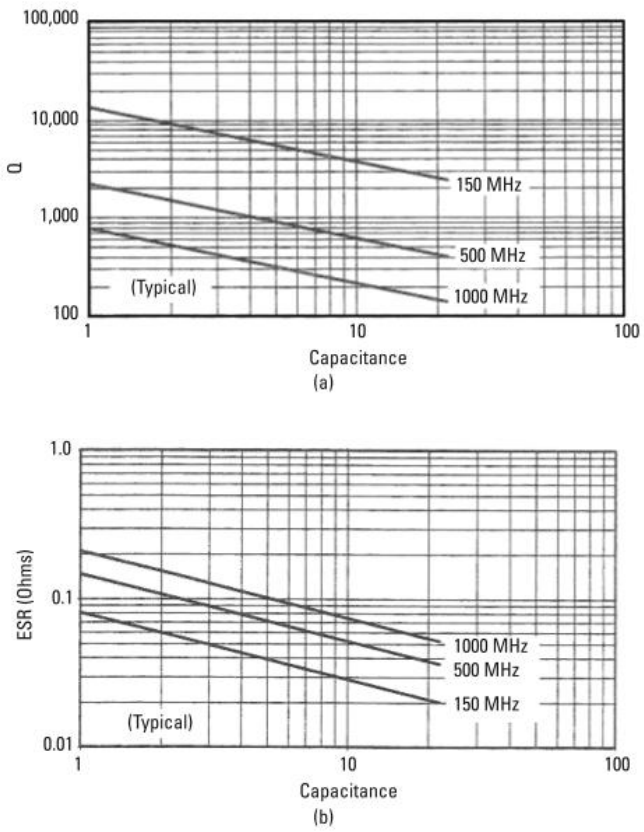


Figure 3.4 - Typical performance of ATC chip capacitors: (a) Q versus capacitance and (b) ESR versus capacitance.

3.2.4 Series and Parallel Resonances

Unlike inductors, from the equivalent circuit shown in Figure 3.5, we see that capacitors have both series and parallel resonance frequencies where the series and first parallel resonance frequencies are dominant. Below the series resonance frequency, the capacitor works as a capacitor as designed. However, above the resonance frequency, the capacitor's total reactance is inductive and it becomes again capacitive after the first parallel resonance frequency. A lumped-element equivalent circuit of a capacitor is shown in Figure 3.5, where L_s is the electrode inductance and C_p is the parasitic parallel capacitance. The impedance of the capacitance between the two electrodes can be written

$$Z_c = \frac{1}{j\omega C_p + \left(R_s + j\omega L_s + \frac{1}{j\omega C} \right)^{-1}} \qquad (3.8)$$

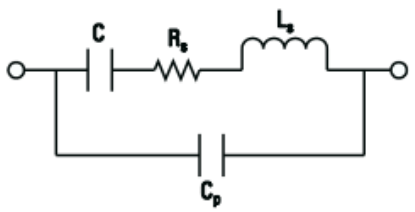


Figure 3.5 - Equivalent circuit of a parallel plate capacitor.

Thus, the value of Z_c is infinite (because of C and C_p) at dc and decreases with frequency. Finally it becomes zero at infinite frequency (because of inductance L_s). However, as shown in Figure 3.6, the behavior of Z_c is no ideal. Figure 3.6 also shows variations of an ideal inductor L, for an ideal capacitor C, and for a parasitic capacitor C_p. When $C >> C_p$, at frequency ω_s, the reactances of series elements C and L_s become equal, that is, $w_s L_s = \frac{1}{w_s C}$, resulting in total reactance equal to zero. The frequency ω_s at which this happens is called the *series resonant frequency* (SRF), and the capacitor's impedance is equal to resistor R_s. Thus, at SRF, a capacitor mounted in a series configuration is represented by a small resistor and its insertion loss is low. As the frequency increases, the reactance of the capacitance becomes very small and the reactances of the parallel elements L_s and C_p become equal, that is, $\omega_p L_s = \frac{1}{\omega_p C_p}$. The frequency ω_p at which this occurs is known as the *parallel resonant frequency* (PRF), and the capacitor becomes a very large resistor whose value is given by

$$R_p = \frac{1}{R_s\left(\omega_p C_p\right)^2} \qquad (3.9)$$

Thus, at PRF, R_p is infinite when $R_s = 0$.

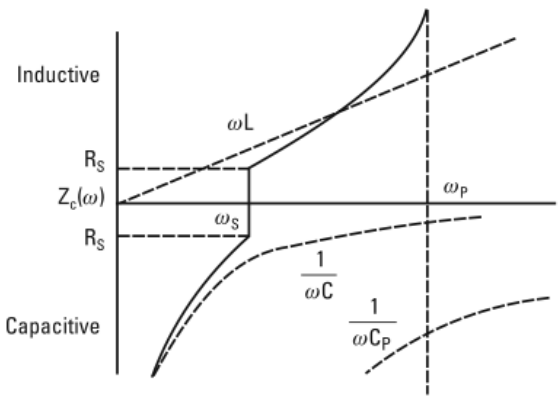


Figure 3.6 - Variation of input impedance of ideal series inductor, series capacitor and parallel capacitor, and parallel plate capacitor [9].

3.2.5 Dissipation Factor or Loss Tangent

The *dissipation factor* (DF) of a capacitor is defined as a ratio of the capacitor's series resistance to its capacitive reactance, that is,

$$DF = wCR_s = \frac{1}{Q} = \tan d \qquad (3.10)$$

where Q was defined earlier in (3.7). The dissipation factor tells us the approximate percentage of power lost in the capacitor and converted into heat. For example, DF = tanδ = 0.01 means that the capacitor will absorb 1% of total power. To dissipate negligible power, one needs a capacitor with very high Q on the order of 1,000 to 10,000.

3.2.6 Rated Voltage

The maximum voltage that can be applied between the capacitor terminals safely without affecting its reliability or destroying it, is known as the *rated voltage* or *working voltage*. The value of the rated voltage for chip capacitors is between 50 and 500V, whereas for monolithic capacitors, it is less than 100V. A typical value for Si3N4 capacitors is about 50V.

3.3 Simple MIM Capacitor Equivalent Circuit Models

Several models for MIM capacitors on GaAs substrate have been described in the literature [11] [12], that include both EC and distributed models.

When the largest dimension of the MMIC capacitor is less than $\lambda/10$, in the dielectric film at the operating frequency, the capacitor can be represented by an equivalent circuit, as shown in Figure 3.7, where B and T depict the bottom and top plate, respectively. The model parameter values can be calculated from the following relations:

$$C = \varepsilon_0 \varepsilon_{rd} \frac{Wl}{d} = \frac{\varepsilon_{rd} 10^{-15}}{36\pi} \frac{Wl}{d} \text{ (F)} \qquad (3.11)$$

$$R = \frac{2}{3} \frac{R_s}{W} l \qquad (3.12)$$

$$G = \omega C \tan\delta = \frac{1}{18} \varepsilon_{rd} f \frac{Wl}{d} \times 10^{-6} \tan\delta \quad \text{(mho)} \qquad (3.13)$$

where ε_{rd} and tanδ are the dielectric constant and loss tangent of the dielectric film, respectively; R_s is the surface resistance of the bottom plate expressed in ohms per square; and W, l, and d are in microns, and f is in gigahertz.

The conductor (Q_c) and dielectric (Q_d) quality factors can be expressed as

$$Q_c = \frac{1}{\omega RC} = \frac{3W}{2\pi f 2R_s lC} = \frac{27 \times 10^6 d}{fR_s l^2 \varepsilon_r} \quad (3.14)$$

$$Q_d = \frac{1}{\tan\delta} \quad (3.15)$$

where *f* is in gigahertz and *l* and *d* are in microns.

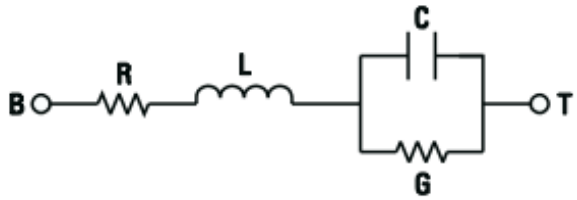


Figure 3.7 - EC model of a MIM capacitor.

The total quality factor Q_T is given by

$$Q_T = \left[\frac{1}{Q_c} + \frac{1}{Q_d}\right]^{-1} \quad (3.16)$$

Figure 3.8 shows another simple lumped EC. Empirically fit closed-form values for such capacitors were obtained as follows:

L (nH) = 0.02249 × log (10 × C) + 0.01 (3.17)

C_1 (pF) = 0.029286 × C + 0.007 (3.18)

C_2 (pF) = 0.00136 × C + 0.004 (3.19)

where C is capacitor value in picofarads, the substrate thickness is 125 μm, capacitor range is 1 to 30 pF, and the frequency range is dc to 19 GHz.

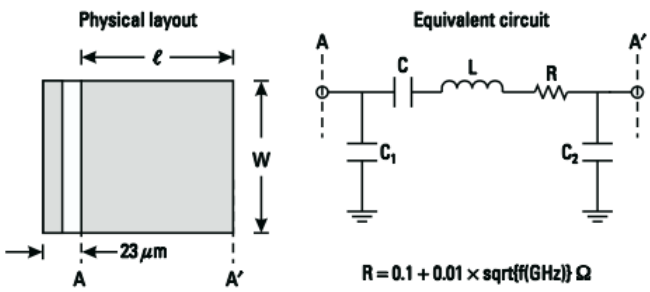


Figure 3.8 - MIM capacitor and its EC model.

Figure 3.9 illustrates the variation of Q-factor for various GaAs capacitors as a function of frequency, whereas Figure 3.10 shows the series SRF of various capacitors. As expected, higher capacitor values indicate lower Q at a given frequency.

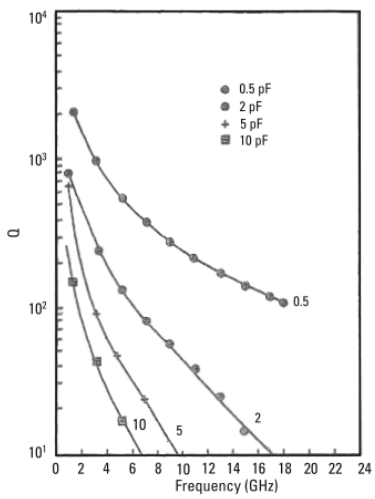


Figure 3.9 Q-factor versus frequency for various MIM capacitors on 125-μm-thick GaAs substrate.

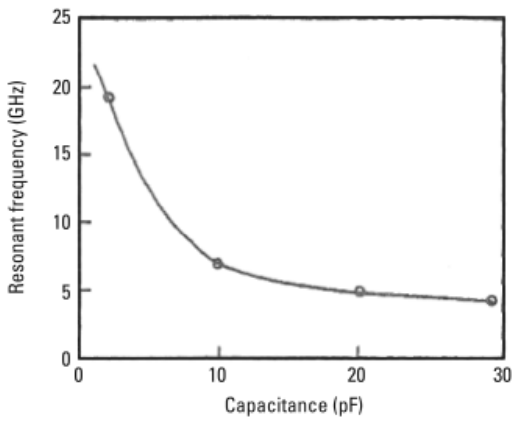


Figure 3.10 Series SRF of various MIM capacitors on 125-μm-thick GaAs substrate.

3.4 Q-Enhancement Techniques

Several techniques to improve the *Q*-factor of MIM capacitors have been used, including thicker and high conductivity metal 1, increasing the aspect ratio (width is greater than length), and micromachining.

Thicker and High Conductivity Metal 1. In MIM capacitors, the bottom metal known as metal 1 is thin. The quality factor of MIM capacitors can be enhanced by using thicker and higher conductivity metal 1.

Aspect Ratio. The resistance of the bottom plate (metal 1) can be reduced by increasing the thickness and reducing the aspect ratio of the conductor and by using a higher conductivity material. For standard fabrication processes, a conductor's thickness and conductivity cannot be changed; however, the capacitor's aspect ratio is at the designer's

disposal. For example, for a given capacitance value, $W = 2l$, Figure 6.28 lowers the dc resistance by a factor of 2, compared to the conventional square geometry, and also reduces the parasitic inductance and increases the series resonance frequency. The aspect ratio (l/W) of a capacitor can be decreased up to a point so that transverse effects (discontinuity and resonance) are negligible. Figure 3.11 shows the calculated value of Q for a 5-pF capacitor having three different aspect ratios.

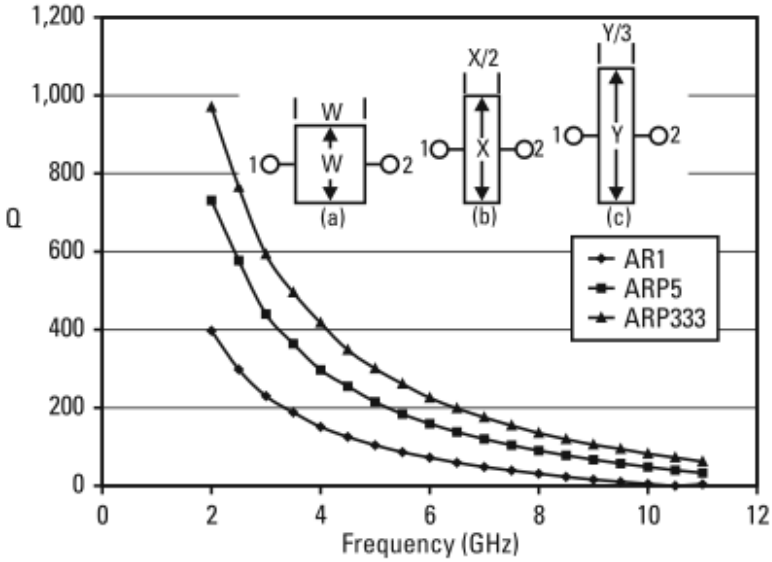


Figure 3.11 Q-factor of a MIM capacitor for three aspect ratios: 1, 0.5, and 0.333.

Chapter 4

Multi-finger MESFETs manufacturing

4.1 *Introduction*

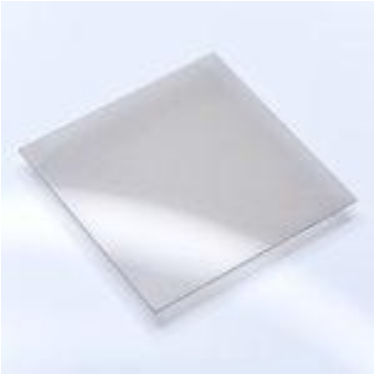
The goal of this doctorate thesis has been the construction and DC/RF characterization of polycrystalline diamond multi-finger MESFETs and passive elements like inductors and capacitors, including the optimization of technological processes. Moreover it's been manufactured a calibration kit for RF measurements and designed an MMIC technological demonstrator.

This and the two following chapters show and discuss the whole technological processes used in this thesis, the problems met during this work and their solving and experimental results compared to simulations ones.

4.2 Diamond substrates features

For diamond MESFETs and lumped elements development and construction I've used polycrystalline diamond samples bought from Element Six Company (E6).

As far as MESFETs substrates concern we have used a polycrystalline diamond sample labeled as TM180 (Figure 4.1). Its thickness is 250 μm and its dimension is 1 cm^2. Its surfaces have been submitted to mechanical polishing to reduce surface roughness in order to allow lithographic processes (see Figure 4.3). At the end of this process the roughness is less than 50 nm.



TM180 10x10 mm, 0.25 mm thick

Tolerances

+0.2 / -0.0 mm on lateral dimensions,

+/- 0.05 mm on thickness,

Surface finish: 1 side polished Ra < 50 nm,

1 side lapped Ra < 250 nm

Laser Kerf < 3°, Dimensions to smaller side

Properties

Thermal conductivity >1800 $Wm^{-1}K^{-1}$

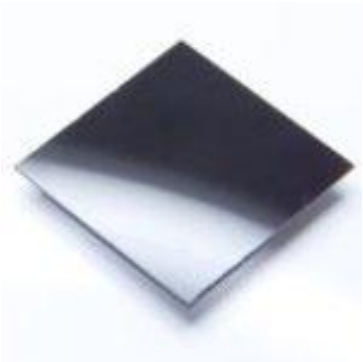
Bulk resistivity (Rv) > 10^{12} Ωcm,

Surface resistivity (Rs) > 10^{10} Ω

Laser cut edges, edge features < 200 µm

Figure 4.1 – Element Six E6 polycrystalline diamond substrate: Thermal Management Grade CVD TM 180

Writing about passive elements substrate, we have used the TM100 substrate (Figure 4.2). The main differences between this sample and the previous one are the different thickness (500 µm for TM100 vs 250 µm for TM180) and different thermal conductivity (1000$Wm^{-1}K^{-1}$ vs 1800$Wm^{-1}K^{-1}$).



TM100 10x10 mm, 0.50 mm thick

Tolerances

+0.2 / -0.0 mm on lateral dimensions,

+/- 0.05 mm on thickness,

Surface finish: 1 side polished Ra < 50 nm,

1 side lapped Ra < 250 nm

Laser Kerf < 3°, Dimensions to smaller side

Properties

Thermal conductivity >1000 $Wm^{-1}K^{-1}$

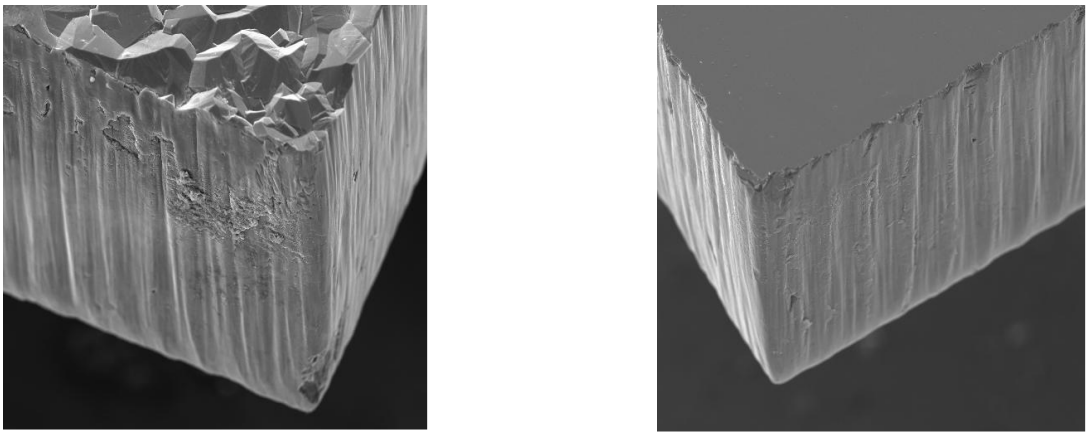
Bulk resistivity (Rv) > 10^{12} Ωcm,

Surface resistivity (Rs) > 10^{10} Ω

Laser cut edges, edge features < 200 µm

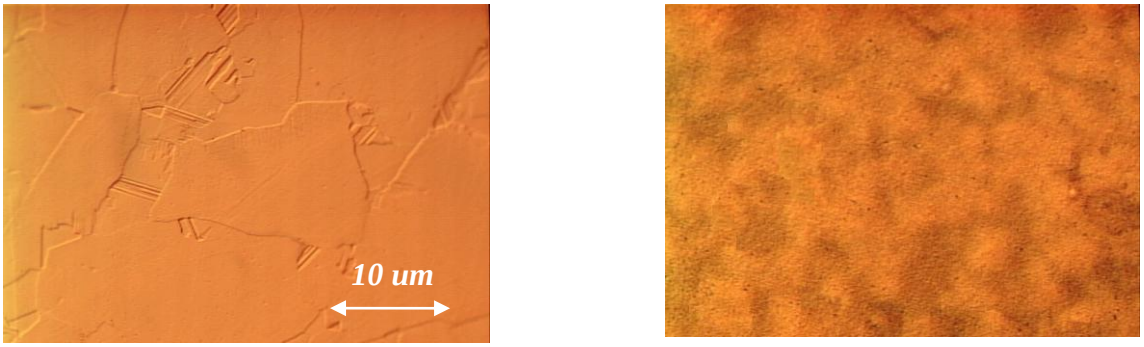
Figure 4.2 – Element Six E6 polycrystalline diamond substrate: Thermal Management Grade CVD TM 100

In Figure 4.3 (a) and (b) SEM pictures of CVD diamond film before and after mechanical polishing are shown, while in Figure 4.4 we can see optical microscope pictures of two diamond samples used in our work. The medium grain size is about 20 µm.



(a) (b)

Figure 4.3 – SEM pictures of CVD diamond film: (a) before and (b) after mechanical polishing.



(a) (b)

Figure 4.4 – Optical microscope pictures of CVD diamond film used in our work: (a) 100X zoom and (b) 5X zoom.

4.3 Air bridge technique

All the devices studied during my PhD are based on the air-bridge technique, that is a bridge construction not standing on a solid material that assures mechanical stability but suspended on air. To make this we need a defined sequence of steps based on technological processes shown next.

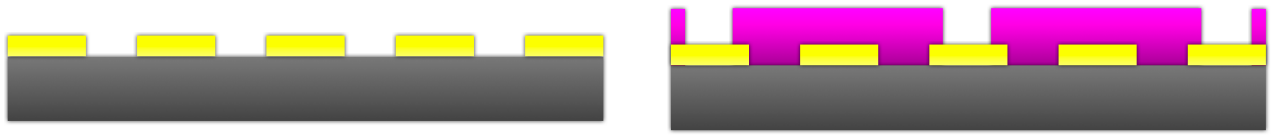
The primary purpose of air-bridges and dielectric crossovers is to provide a cross-connection for two non-connecting printed transmission-line sections. They are also commonly employed in transistor to create a non-connecting crossover between a multiple source and gate, electrodes, spiral inductors, MIM capacitors (to improve the breakdown voltage) and coplanar waveguide (CPW) based MMICs to connect both ground planes in order to suppress the propagation of the coupled slotline mode.

Air-bridges use air as the dielectric between the two conductors, whereas dielectric crossovers employ a layer of low dielectric constant material such as polymide or BCB. Air-bridges and dielectric crossovers have also been used in reducing the shunt capacitance between the conductors and the ground plane in MMIC spiral inductors and transformers. Low shunt capacitance is a desirable feature of a component to extend the maximum operating frequency.

Moreover we can use this technique (the electroplating part) to thicken our contacts and reduce their resistivity.

We start from a substrate where ohmic contacts (in case of MESFET devices, whereas first metallization level for passive elements) are realized, as shown in Figure 4.5.a.

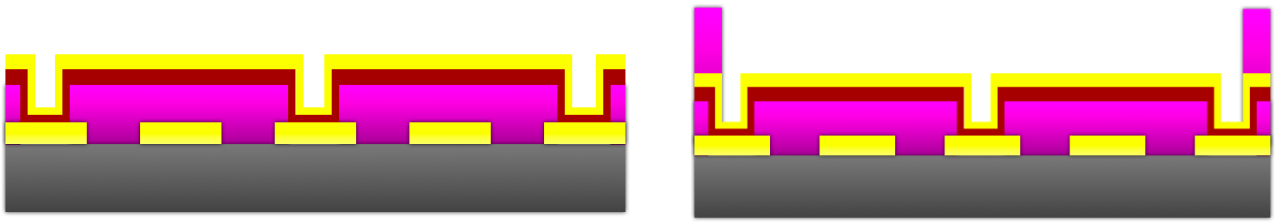
The first step is the definition, using optical lithography, of areas corresponding to the bridge piers (Figure 4.5.b).



(a) *(b)*

Figure 4.5 – (a) substrate with ohmic contacts (b) photoresist patterning to bridge piers definition.

Over this pattern a double layer of Cr and Au is deposited to generate a metallic template. The presence of this layer is fundamental for potential distribution along the sample to allow the electroplated gold growth (Figure 4.6.a).



(a) *(b)*

Figure 4.6 – (a) metallic template for potential distribution (b) bridge boundaries definition over the metallic template.

Over this template we define areas, using photoresist, where the bridge will build and then the galvanic growth of gold takes place (Figures 4.6.b – 4.7.a).

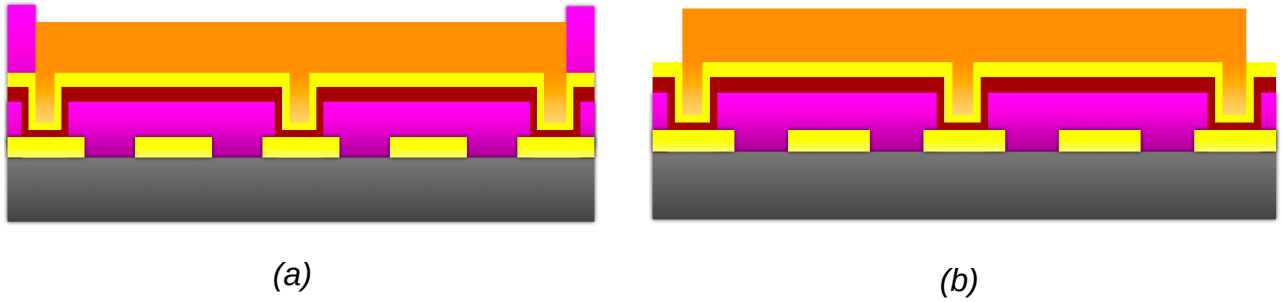


Figure 4.7 – (a) electroplating gold growth and (b) photoresist removal.

The next step is the photoresist dissolution using acetone followed by Au and Cr wet etching to remove metallic layer where it's not necessary anymore (Figures 4.7.b – 4.8.a). At the end we remove the first layer of photoresist, it means the material under the bridge, so the structure remains suspended on air (Figure 4.8.b).

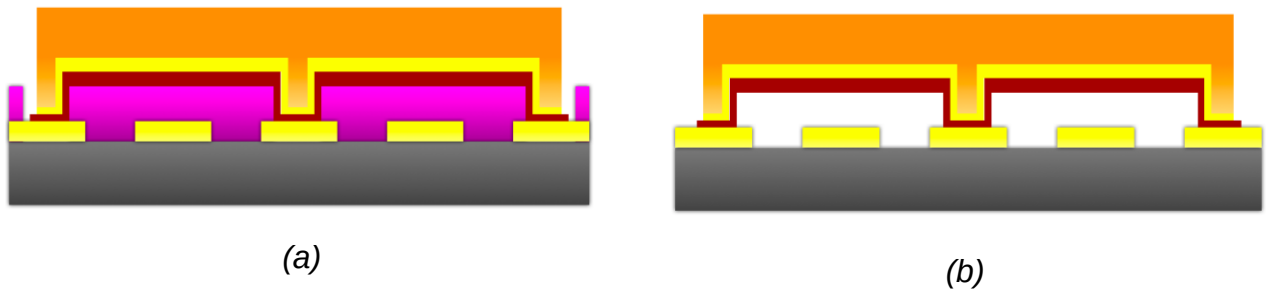


Figure 4.8 – (a) metallic template etching and (b) following photoresist removal under the brigde. At this point the device process is complete.

4.4 Multi-fingers MESFETs

Before entering into details of used technological steps, in Figure 4.9 is shown the list of the whole process to produce diamond multi-fingers MESFETs.

MULTIFINGERS MESFET PROCESS

1. SUBSTRATE CLEANING

30' at 100 °C in sulfochromic acid mixture ($K_2Cr_2O_7$ + H_2O+ H_2SO_4)

15' in aqua regia (3HCl + 1HNO_3)

15' in Kalish's mixture (1HNO_3 + 1$HClO_4$ + H_2SO_4)

20' piranha clean (5H_2SO_4 + 1H_2O_2) @120°C

15' in hot trichloroethylene

15' in hot acetone

15' in hot isopropyl alcohol

2. HYDROGEN PLASMA ON DIAMOND SURFACE

H_2 flow: 200 sccm

Substrate temperature: 770°C

Pressure: 40-60 torr

Hydrogen MW plasma power: 1,23 kW

Processing time: 30’ (at 40 torr) + 15’ (at 60 torr)

3. OHMIC CONTACTS

positive photoresist: S1818

spinning conditions: 60”@4000 rpm

bake: 2’@120°C

exposure: 25”

post exposition bake: 60”@120°C

Development: 40” with MF322 solution (1:6 - MF322:Water)

Thermal Evaporation: 50 nm Ti/Au (20/30 nm) - growth rate: Ti 0.25 nm/s, Au 0.30 nm/s

Metal lift-off with acetone

4. DEVICE ISOLATION

positive photoresist: S1818

spinning conditions: 60”@4000 rpm

bake: 2’@120°C

exposure: 25”

Development: 40” with MF322 solution (1:6 - MF322:Water)

Hard bake: 1’@120°C

RIE processing: RF 16.6%, 25% O2, Ar 20mm, P 40mT, t 60s

Photoresist removing with acetone

5. GATE CONTACTS

positive photoresist: PMMA 600K

spinning conditions: 60”@2500 rpm

bake: 5’@170°C

E.B.L. lithography: gate length 0.5, 1.0, 2.0, 4.0 μm

E-beam Evaporation: 100 nm Al growth rate 0.30 nm/s

Metal lift-off with acetone

6. BRIDGE PIERS AND SOURCES DEFINITION

positive photoresist: S1818

spinning conditions: 60”@4000 rpm

bake: 2’@120°C

exposure: 30”

Development: 40” with MF322 solution (1:6 - MF322:Water)

7. METALLIC SEED LAYER

Evaporation: 20 nm Cr

Sputtering: 200 nm Au

8. BRIDGE DEFINITION

positive photoresist: S1818

spinning conditions: 60”@4000 rpm

bake: 2’@120°C

exposure: 30”

Development: 40” with MF322 solution (1:6 - MF322:Water)

9. AU ELECTROPLATING

electroplating bathe: 15’ in Sodium dicyanoaurate $Na[Au(CN)_2]$ @ 55°C and 30 mA

Water bathe: 10’’ @ 55°C

Electroplating gold thickness: ≅ 1 μm

10. PHOTORESIST REMOVAL AND WET ETCHING

Top photoresist removal with acetone

15” metallic template Au etching (400g:100g:400ml - I_2:KI:H_2O)

5” metallic template Cr etching (2:3:12 - $KMnO_4$:NaOH:H_2O)

Bottom photoresist removal with acetone

Figure 4.9 – List of steps used to multi-finger MESFETs manufacturing.

After we have seen the process list, let’s enter into details of every single step.

4.4.1 Substrate surface cleaning

First of all we start from the cleaning of diamond substrate to remove possible impurities over the surface. We’ve executed the following steps:

30’ at 100 °C in sulfochromic acid mixture ($K_2Cr_2O_7$ + H_2O+ H_2SO_4)

15’ in aqua regia (3HCl + 1HNO_3)

15’ in Kalish’s mixture (1HNO_3 + 1$HClO_4$ + H_2SO_4)

20’ piranha clean (5H_2SO_4 + 1H_2O_2) @120°C

15’ in hot trichloroethylene

15’ in hot acetone

15’ in hot isopropyl alcohol

Excluding the first four steps that we use only at the start of the process, we can use the remaining ones after hydrogen plasma too because these cleaning are based on not oxidizing solution to guarantee diamond surface conductivity. In Figure 4.10 we can see the three different non oxidizing solutions on hot plate.

Figure 4.10 – Last three cleaning steps used for diamond substrates.

During these steps we put our attention to the process in order to sample remains always "wet" between different steps, because next solvent could dissolve impurities of previous steps.

4.4.2 Hydrogen plasma diamond surface treatment

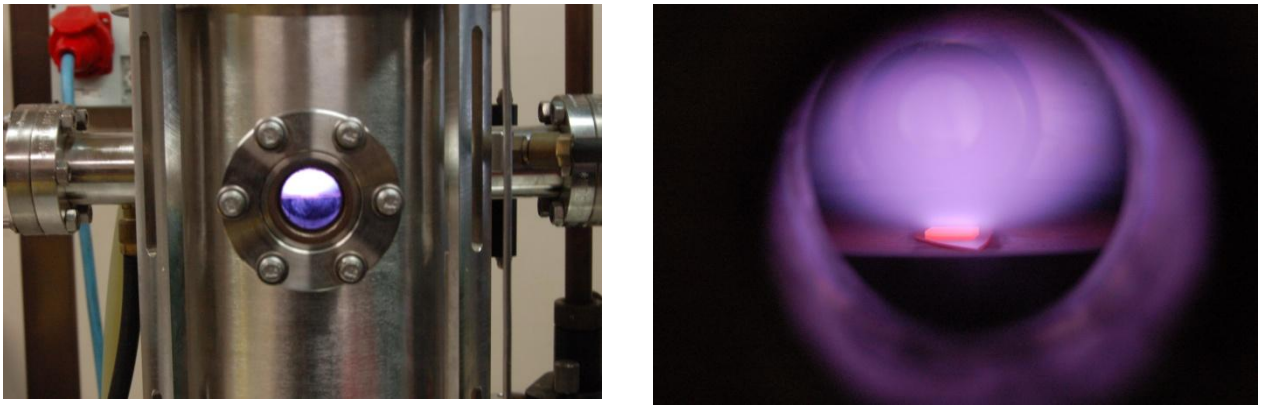
If a high resistive substrate is a necessary condition to obtain high performance passive devices (as diamond substrate), for MESFETs construction we need high conductivity areas where the transistor channel takes effect.

To make conductive the diamond surface, an hydrogen plasma is used.

This process was made at CNR – IMIP lab (Istituto di Metodologie Inorganiche e Plasmi) of Montelibretti, in collaboration with Dr. Daniele Trucchi, using these specifications:

- H_2 flow: 200 sccm
- Substrate temperature: 770°C
- Pressure: 40-60 torr
- Hydrogen MW plasma power: 1,23 kW
- Processing time: 30' (at 40 torr) + 15' (at 60 torr)

In Figure 4.11 is shown the hydrogen plasma camera and a particular hydrogen plasma step.



(a) (b)

Figure 4.11 – (a) Hydrogen plasma chamber and (b) switching on plasma process. The pink colour derives from using of hydrogen.

We can verify and estimate the surface conductivity and the quality process result making measurements using two probes directly on diamond substrate.

This first measurement is shown in Figure 4.12. It shows a resistivity of 30-40 kΩ.

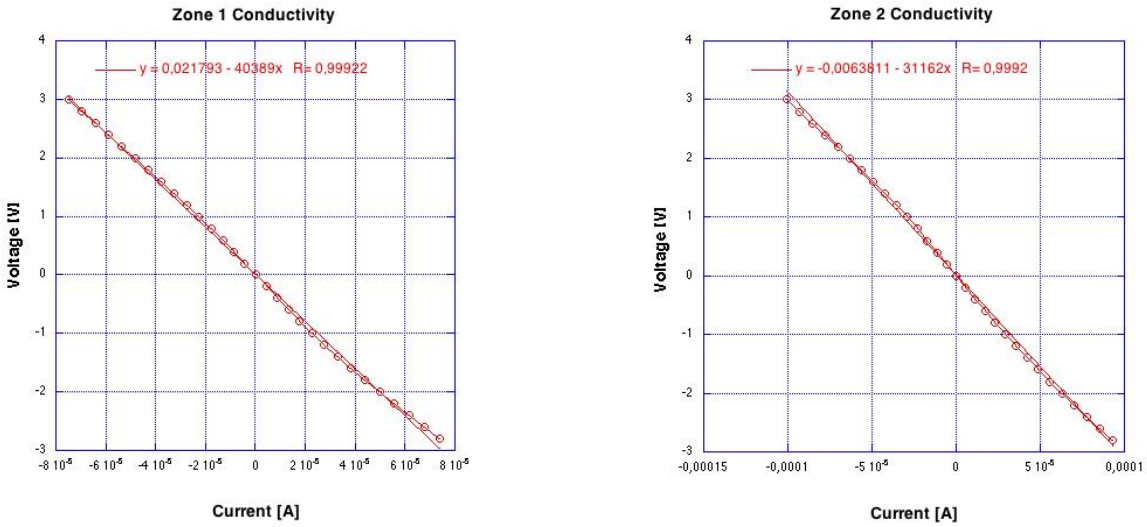


Figure 4.12 – Results of conductivity measurement on hydrogenated diamond surface. We have a resistivity of 30-40 kΩ. We use this test only to verify the hydrogenation process.

4.4.3 Ohmic contact: lithography and gold evaporation

After diamond sample pasting on a silicon substrate to increase the sample handling, we insert our substrate into the spinner. With this machine we can apply a thick layer of photoresist to permit photolithographic process. The conditions are the following:

- positive photoresist: S1818
- spinning conditions: 60”@4000 rpm
- bake: 2’@120°C

In this way we obtain a 2 μm thick photoresist layer.

The next step is the first mask layer exposure, that is where all ohmic contacts and alignment markers are designed. In Figure 4.13 this first mask layer is shown.

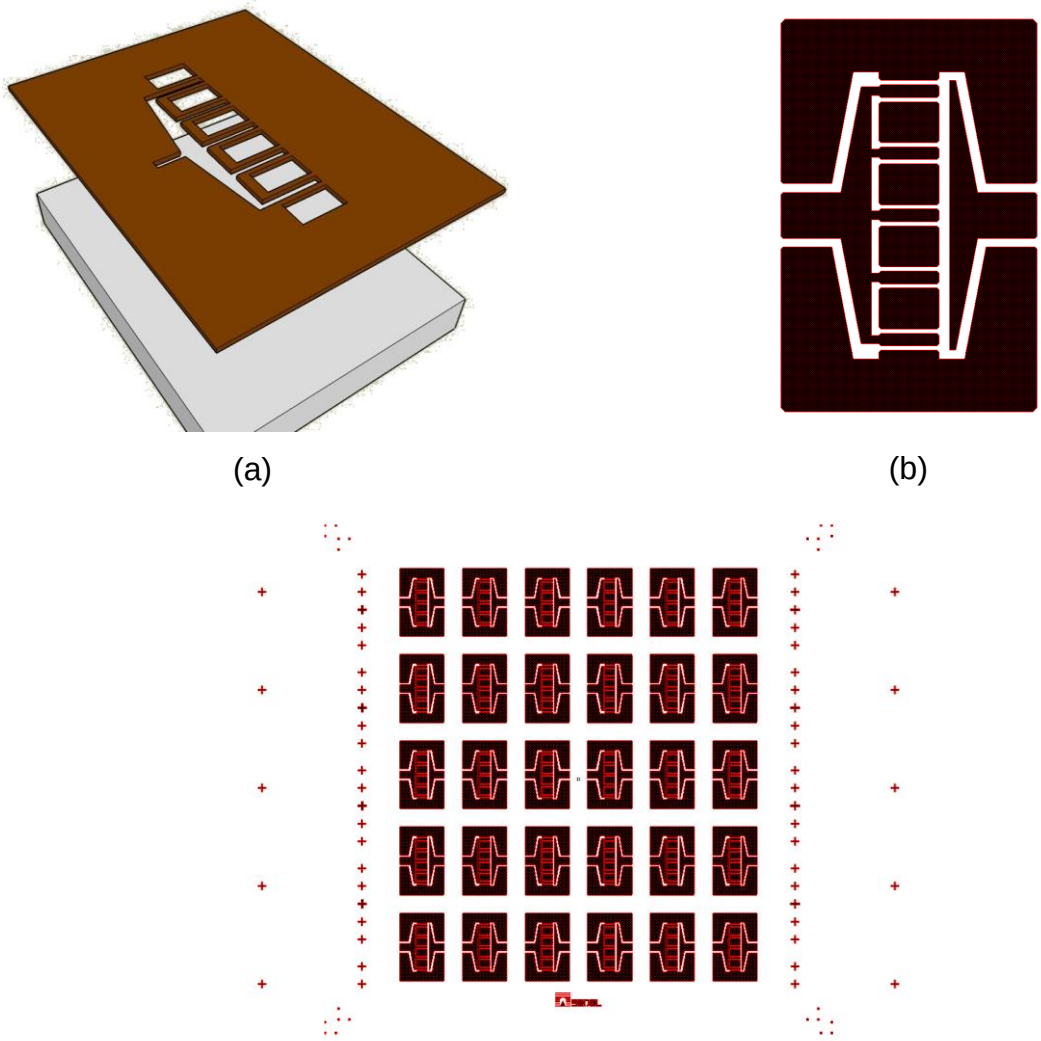


Figure 4.13 – (a) Schematic of ohmic mask applying on diamond substrate (b) device detail and (c) total ohmic contact mask designed with LASI 7 software.

The optical lithography (soft contact lithography mode) is made by Karl Suss MA6 mask-aligner with power density of 18 mW/cm^2 , using a 394 W mercury arc lamp with *i-line* emission at 365 nm.

After 25” of exposure, we make a post exposition bake (P.E.B) of 2’@120°C to improve resist adhesion and profile. Next we develop our sample and the results are shown in figure 7.14

Summarizing the lithography conditions are the following:

- exposure: 25”
- post exposition bake: 60”@120°C
- Development: 40” with MF322 solution (1:6 - MF322:Water)

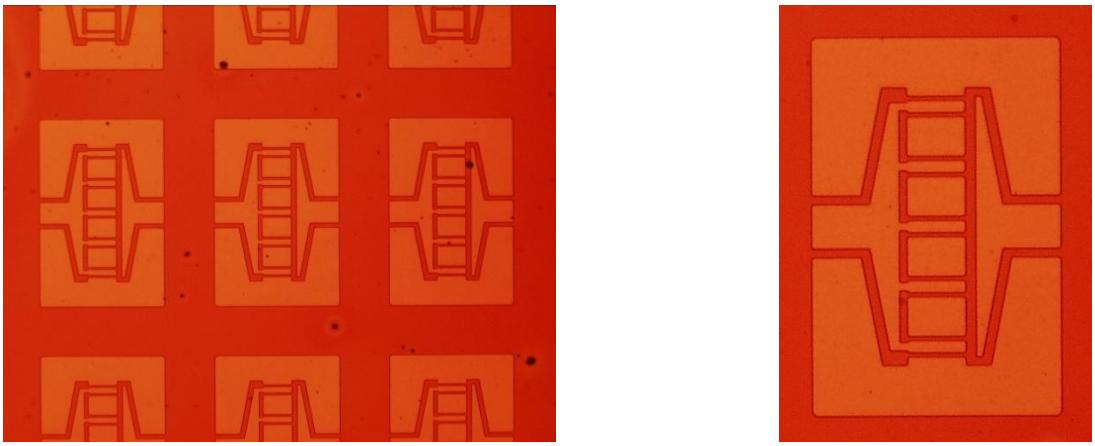


Figure 4.14 – Microscope photos of diamond sample after first step resist development. We can appreciate the butterfly shaped transistor layout for RF applications.

Then we have evaporated 20 nm of Titanium and 30 nm of Gold using a *thermal evaporator*. The growth rate is 0.25 nm/s for Ti and 0.3 nm/s for Au. Before titanium/gold deposition we need high vacuum value in the chamber, circa 8*10^{-7} mbar, thanks to cryogenic pumps. This vacuum condition is reached after 3 hours from pumps start.

Next step is the metal lift-off with acetone. In fact with this process we remove either the photoresist or the metal where we don’t need it. To dry the diamond sample we use acetone vapor to avoid halos and sediments on substrate.

After all ohmic contacts steps we have the situation shown in Figure 4.15

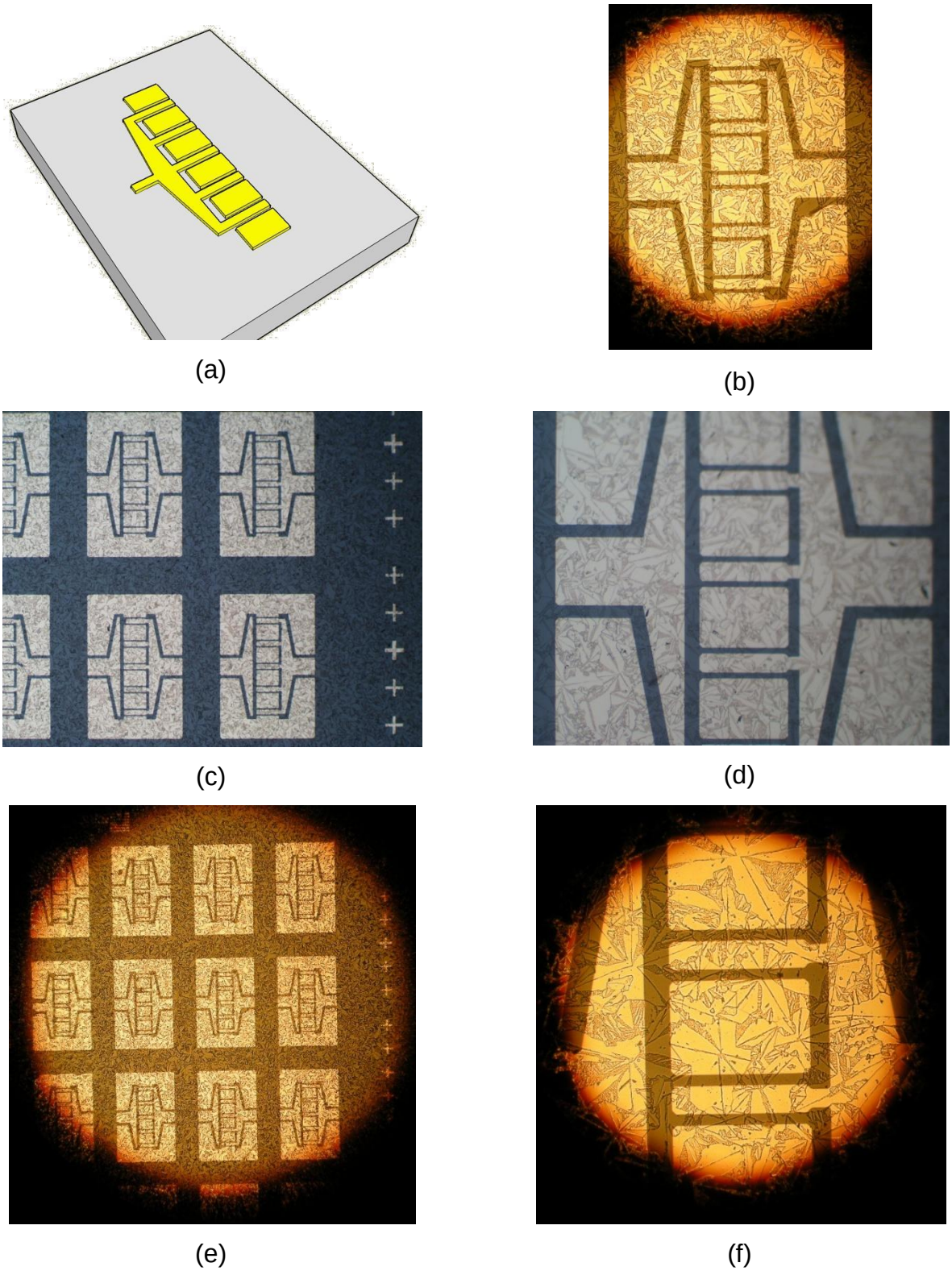


Figure 4.15 - (a) Schematic and (b)-(f) some microscope photos at different magnifications of diamond substrate after Au evaporation and lift-off. It's shown the alternation between source and drain pads.

4.4.4 Device isolation

Isolation means to narrow the wafer conductive portion to a specific areas of surface, in order to avoid to the electric current flows in different areas. Isolation is used to reach several goals:

- in active devices, it forces the current to flow in desired paths (under the gate);
- all the devices on the same wafer are electrically isolated one from each other;
- it reduces parasitic capacity and resistance;
- it creates an enough resistive surface to permit the passive elements and the transmission lines construction.

As shown in Figure 4.16, the active area is designed to link source and drain pads. The drain-source current is forced to flow under the gate contact. If a part of this current flew between source and drain without passing under the gate, this current would represent a parasitic resistance that would degrade RF performances.

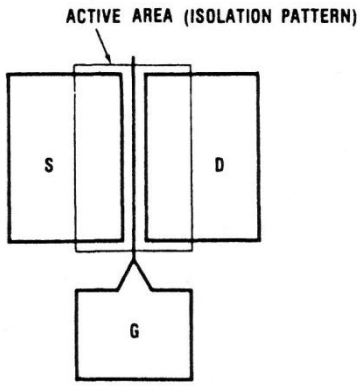


Figure 4.16 – Use of device isolation to limit the current flown under the gate area and separate electrically different devices.

The use of isolation to reduce parasitic capacitance is shown in Figure 4.17 for GaAs substrate: we can make the same observations for diamond case. The gate strip forms a Schottky barrier with a depletion area under it; a capacity is associated with this depleted area. The size of this capacitance is a function of metal area and semiconductor dopant density. If gate contact was on the conductive area, it would have an associated capacitance bigger than the gate stripe. Though an associated capacitance with the gate strip is essential to the FET operation, the pad associated capacitance is parasitic. Building

the gate pad on a insulating or semi-insulating material reduces considerably the parasitic capacitance.

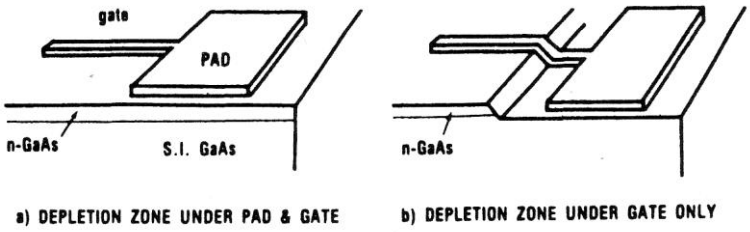


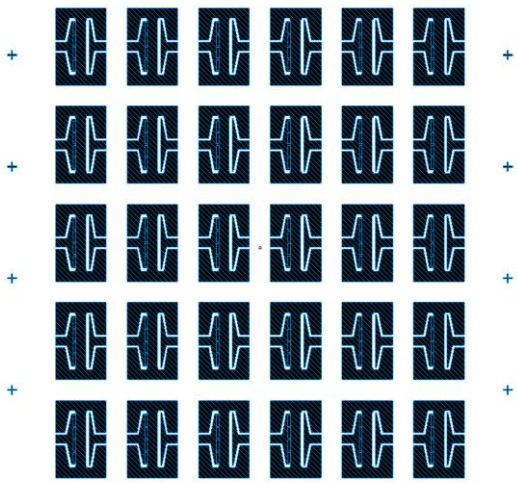
Figure 4.17 - Use of isolation to reduce parasitic capacitance: the pad over (a) active material has a big associated capacitance (b) semi-insulating material has a very small associated capacitance. Images refer to GaAs substrate but the same observations are valid for diamond too.

Returning to our process, at this point we have a series of ohmic contacts over our substrate that are still linked with the conductive hydrogen surface channel: so it's necessary remove this channel to isolate the devices one from the others.

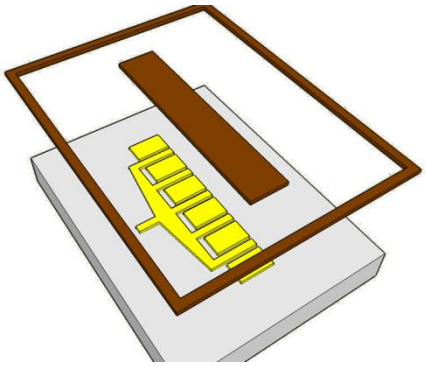
We insert our substrate into the spinner. The conditions are the same for the ohmic contact step:

- positive photoresist: S1818
- spinning conditions: 60"@4000 rpm
- bake: 2'@120°C

Than we expose the second mask, that is we cover all the areas where we want that the conductive layer remain. In Figure 4.18 this second mask layer is shown.



(a)



(b)

(c)

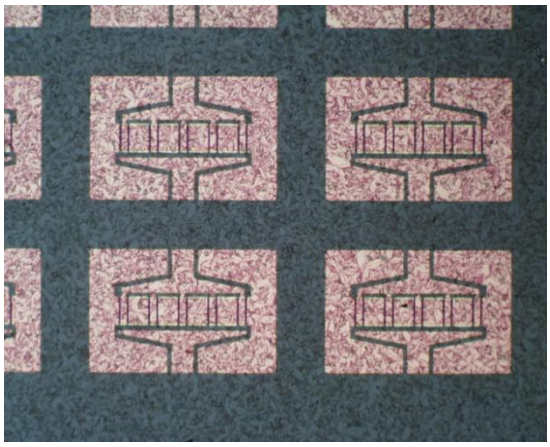
Figure 4.18 - (a) Total isolation mask exposed over ohmic contacts, (b) schematic and (c) device mask detail.

In this phase it's necessary the alignment of this mask with the ohmic contact pattern previously printed. This is obtained using alignment markers (the crosses on the both sides of samples in Figure 4.18.a).

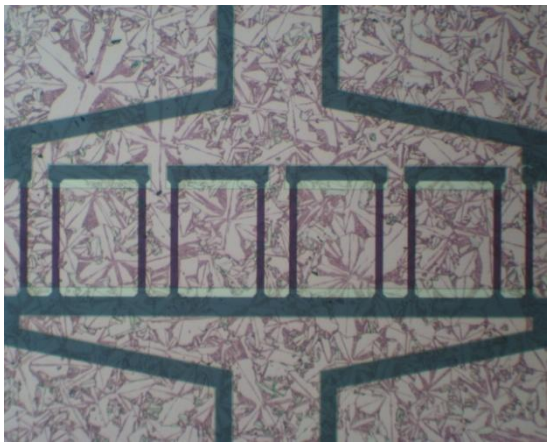
After 25" of exposure, we develop photoresist and than we make an hard bake of 1'@120°C to harden photoresist and smooth the profile. Results are shown in figure 4.19

Summarizing the lithography conditions are the following:

- exposure: 25"
- Development: 40" with MF322 solution (1:6 - MF322:Water)
- hard bake: 1'@120°C



(a)



(b)

(c)

Figure 4.19 - (a) Microscope photos before and after RIE processing. All the areas between drain and source are protected with a 2 µm *photoresist layer during Ar-O_2 plasma.*

Then we submit our sample to the *Reactive Ion Etching (R.I.E.)* process that consists in an oxygen-argon plasma with these conditions:

RIE processing:
RF 16.6%, 25% O2, Ar 20mm,
Pressure: 40mT
Time: 60s

In this way we reduce the diamond surface conductivity of many orders of magnitude.
Next step is the photoresist lift-off with acetone.

4.4.5 Gate contact: lithography and aluminum evaporation

At this point we have the sample with ohmic contacts and a conductive surface only where it's necessary. The next step is the gate construction (Figure 4.20). We have written different gate lengths (4 µm, 2 µm, 1 µm, 0.5 µm) using E.B.L. technique (Electron Beam Lithography). We made this in collaboration with CNR-IFN (Photonic and Nanotechnology Institute) of Rome – Dr. Ennio Giovine. The gate fingers position is centered between drain and source pads.

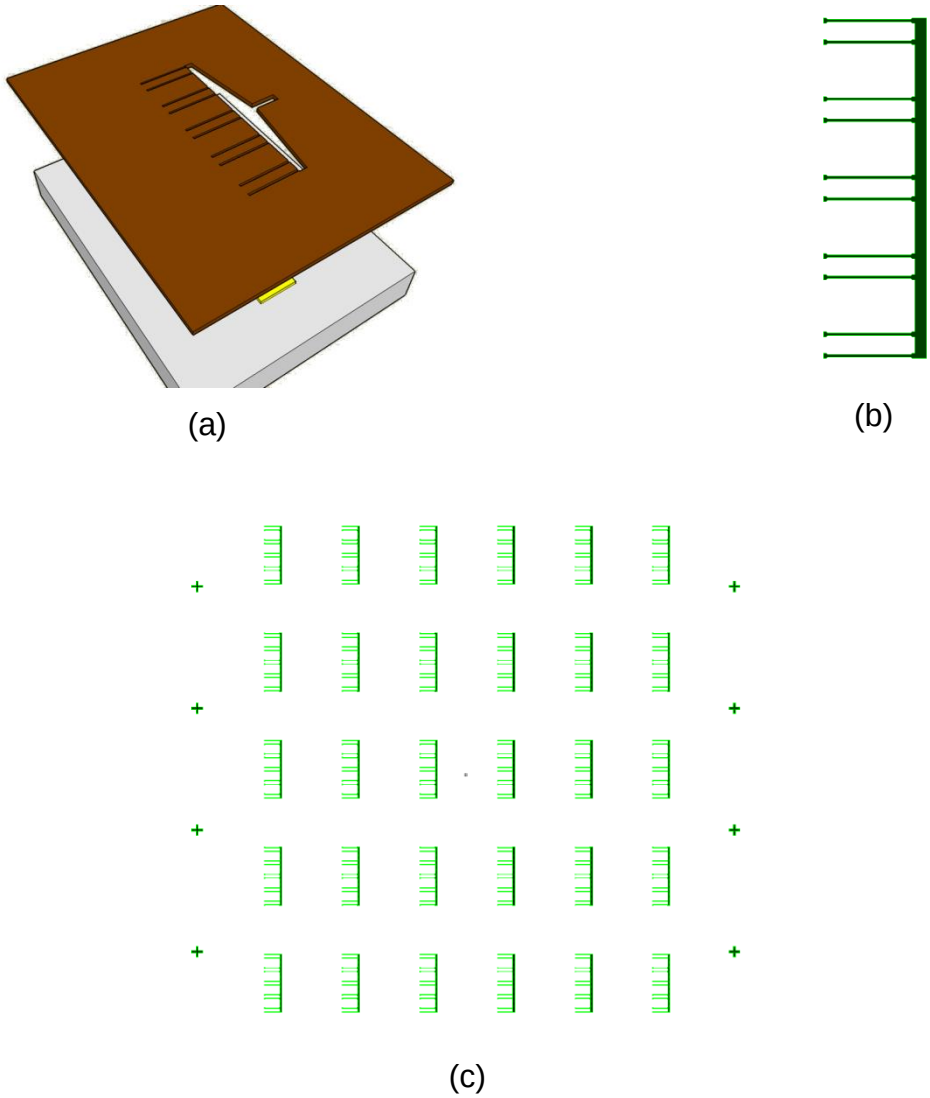


Figure 4.20 - (a) Schematic of gate mask applying on diamond substrate (b) single device detail and (c) total gate contact mask.

The use of this technique is been possible because we have design process masks with special alignment markers. These markers, as shown in Figure 4.13, are Ti-Au 20μm x 20μm squares set in the four corners of the base cell: in this way the electron beam system can align itself with other structures on the sample. Then, we have evaporated 50 nm of Aluminum using an *e-beam evaporator* with a growth rate of 0.3 nm/s. We've waited 2 hours to obtain a good vacuum condition ($1*10^{-7} \div 8*10^{-8}$ mbar).

Next step is the metal lift-off with acetone. The result is shown in Figure 4.21

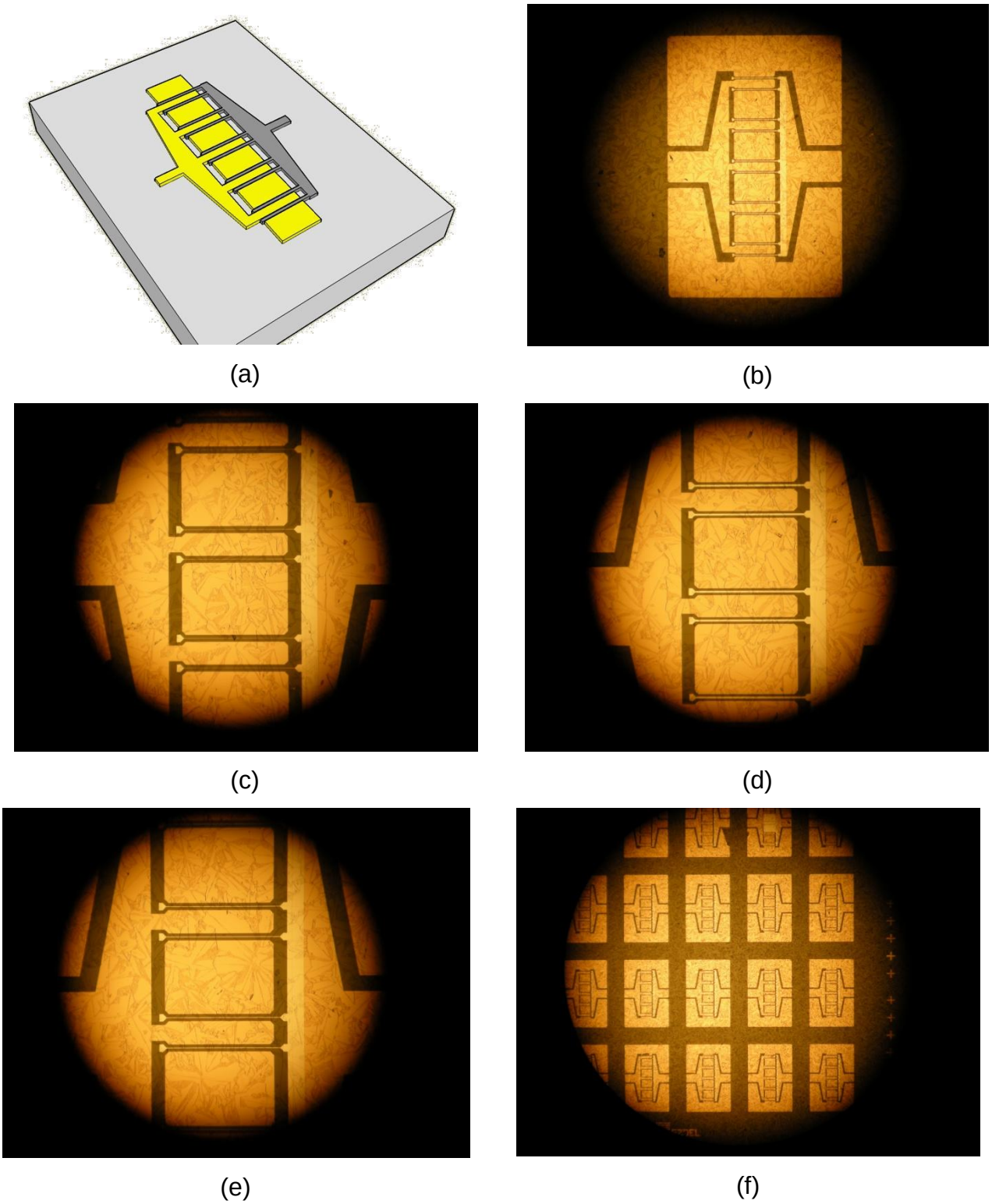


Figure 4.21 - (a) Schematic and (b)-(f) optical microscope photos at different magnifications of diamond substrate after Al evaporation and lift-off. We can see multi-fingers gate centered insertion between drain and source pads. Gate lengths L are 0.5, 1.0, 2.0 and 4.0 μm. Source pads aren't just connected each other: we need to air-bridging them to ensure device working.

4.4.6 Bridge piers and source definition

Up to now we've processed our samples as made for bi-fingers MESFETs. Now we move in a different way respect that process. In fact, after gate building, the bi-fingers MESFET is ready to work, instead multi-fingers MESFET needs to connect all the source pads each other to permit parallel working. At this point the air-bridge technique arises. In the next steps it's shown how manufacture a bridge suspended on the air. The same steps are used in parallel to thicken ohmic contacts.

First of all, starting from a substrate where we've defined all kind of contacts, we insert our substrate into the spinner and we apply a 2 μm thick photoresist layer to permit photolithographic process. The conditions are the following:

- positive photoresist: S1818
- spinning conditions: 60"@4000 rpm
- bake: 2'@120°C

The next step is the bridge piers and source definition mask layer exposure. In Figure 4.22 this mask layer is shown.

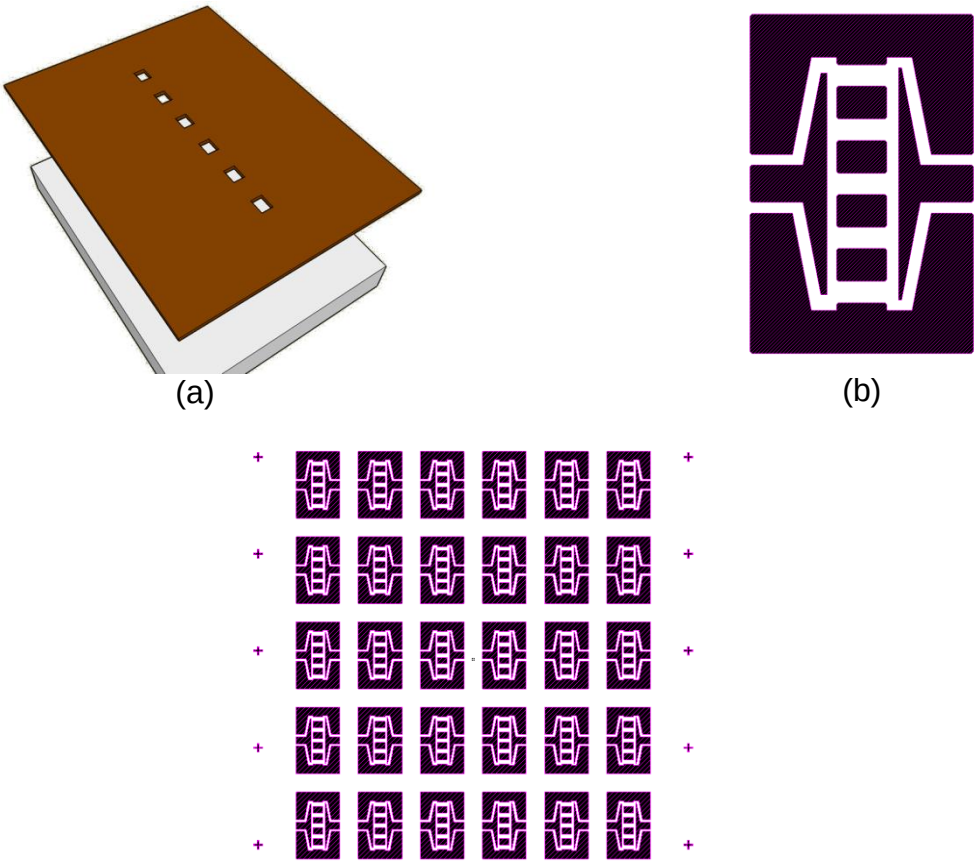


Figure 4.22 – (a) Schematic of bridge piers mask process (b) device detail and (c) total mask.

After 30” of exposure, we develop our sample for 40” with MF322 solution (1:6 - MF322:Water) and the results are shown in figure 4.23.

The 2 μm thick photoresist defines the height of the bridge too. It should be high enough to minimize parasitic capacitances.

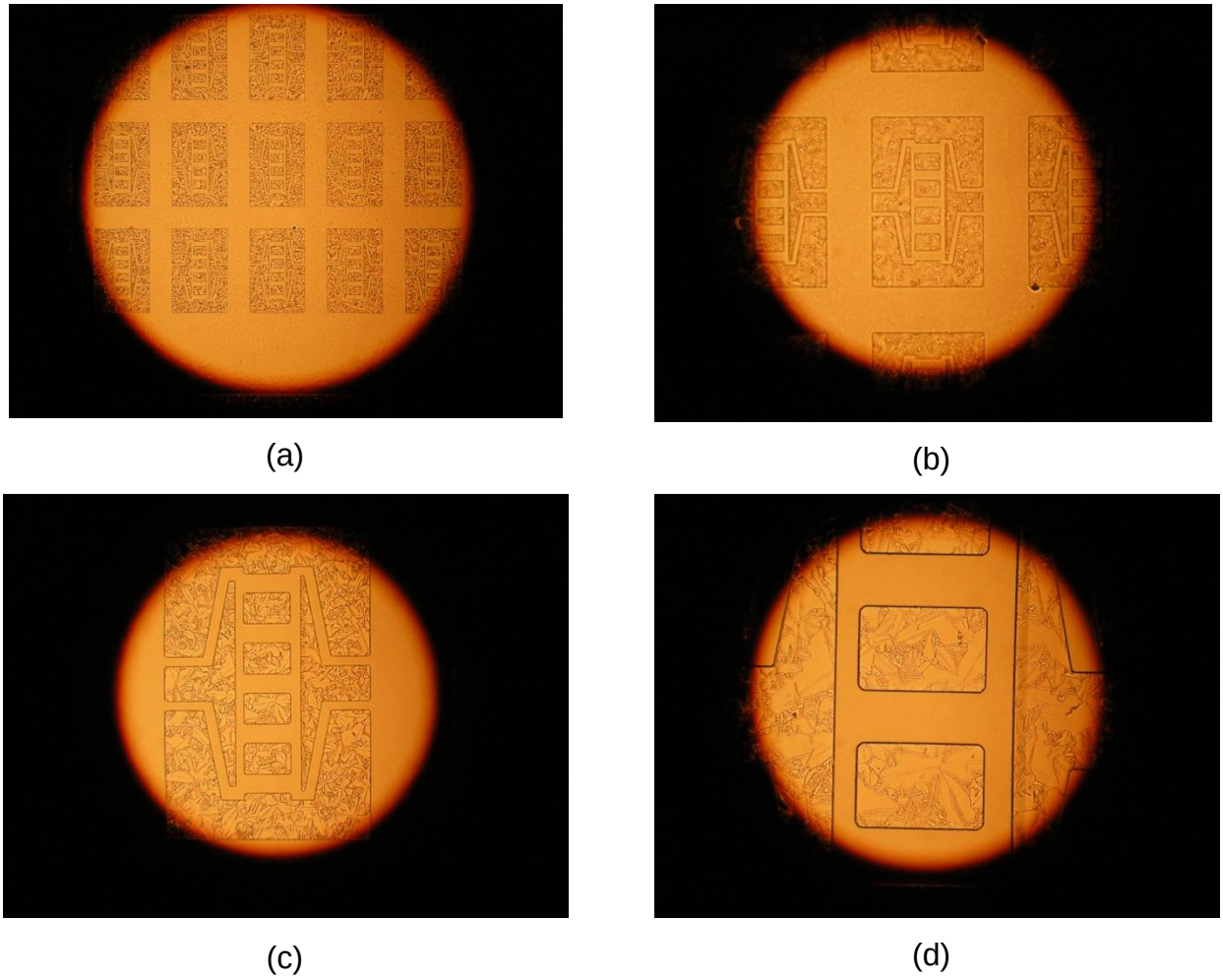


Figure 4.23 - (a) Microscope photos after bridge piers definition lithography. Over this pattern it’s applied a metallic template to permit electroplating growth.

4.4.7 Metallic seed layer

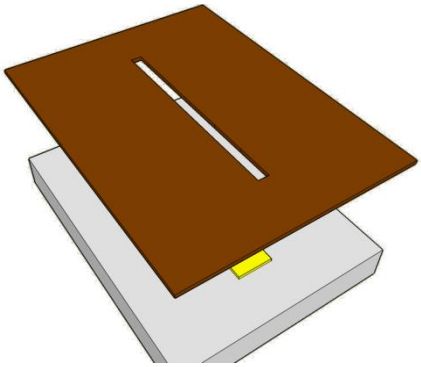
After photoresist patterning to define the bridge posts, a seed layer is deposited which serves as cathode electrode in the Au electroplating process. This seed layer should be continuous over the whole sample surface otherwise no plating will occur due to a break in the cathode electrode. Therefore, the side walls of the thick support resist should not be too steep.

We use a first 20 nm thick Chrome layer followed by 200 nm thick Au layer. The first layer is made by evaporation and the second one with sputtering process. We use a thin Chrome layer because, during the Au etching process, the etching solution could pass through underlying photoresist and attack the ohmic contact gold. On the other hand we complete this metallic layer with Au sputtering because we need a solid and conductive gold structure to grow electroplating gold.

4.4.8 Effective bridge definition

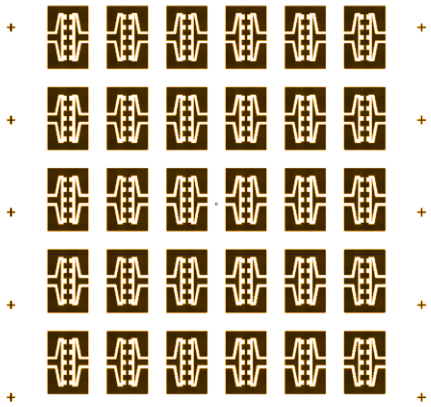
After metallic layer applying we actually define the bridges and pads boundaries. This is the last lithographic step we use. Process conditions are the same of paragraph 4.4.6 except exposure time that is 5'' less than previous one, so 25'' seconds because gold beneath resist causes back scattering during exposure process.

The definition mask layer is shown in Figure 4.24 and results are shown in Figure 4.25.



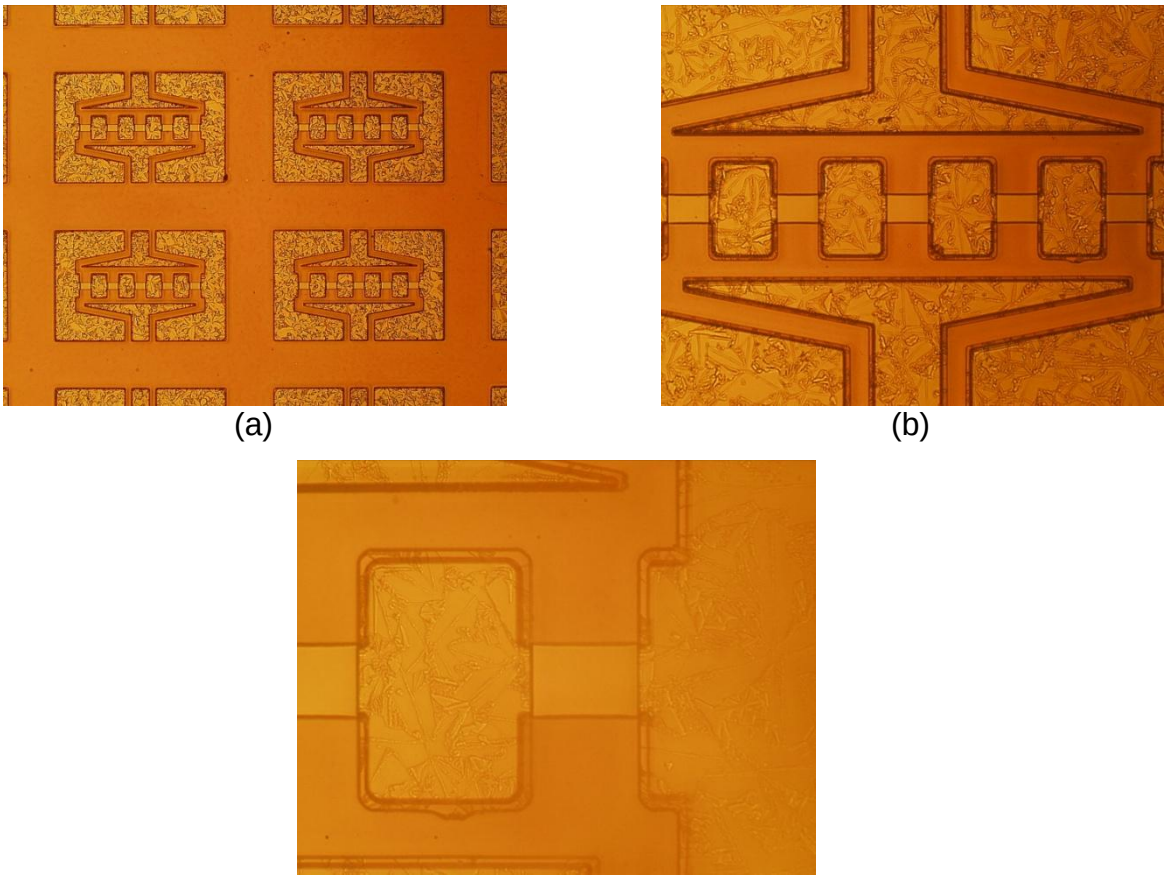
(a)

(b)



(c)

Figure 4.24 – (a) Schematic of bridge definition (b) device detail and (c) total mask.



(a) (b) (c)

Figure 4.25 - (a) (b) (c) Microscope photos after effective bridges and pads definition lithography. (c) Detail of bridge definition.

4.4.9 Electroplating gold

Next fundamental step is the Au electroplating on previously defined areas. To do this we have used an electroplating bathe at IFN-CNR of Rome – Dr.sa Annamaria Gerardino. As previously said in paragraph 4.4.7 we use two submerged electrodes and one of this (cathode) is our sample. Between these electrodes there is a current flown of 30 mA that produces an Au growth of ≅ 1 μm after 15' of process. The bathing temperature is 55°C. When we stop the current flown we take our sample out the bathe and dip it into hot water. It's necessary used hot water to avoid Au precipitation. The result of this step is shown in Figure 4.26.

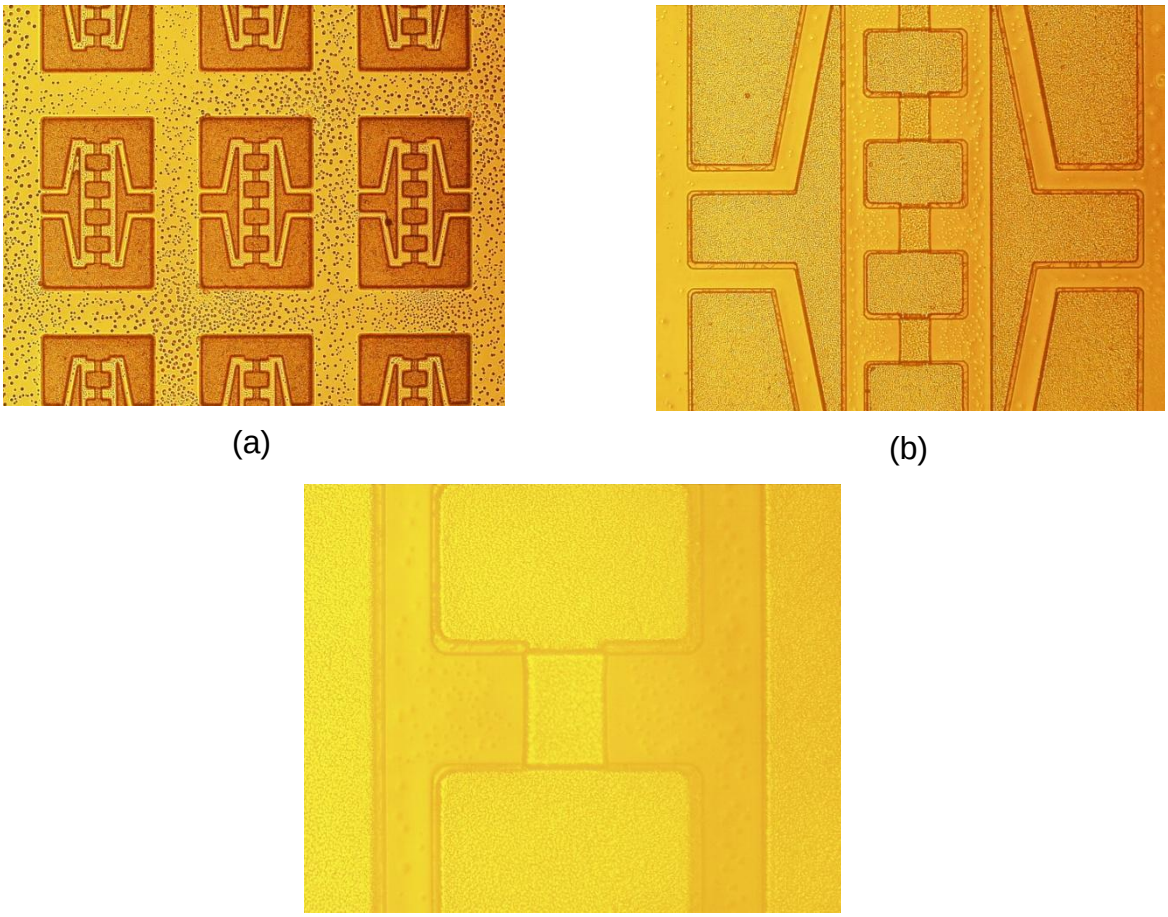
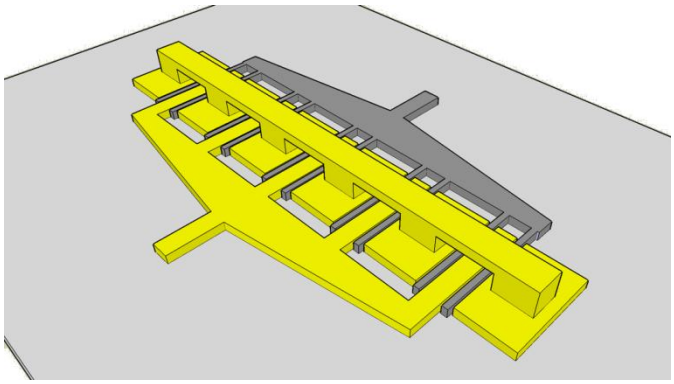


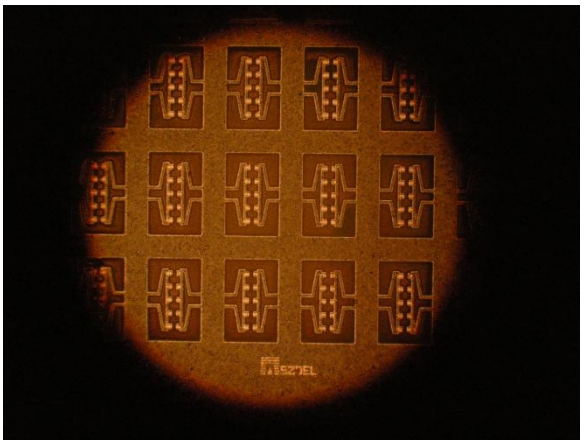
Figure 4.26 - (a) (b) (c) Microscope photos after Au electroplating. (c) Detail of bridge growth.

4.4.10 Photoresist removal and Cr-Au wet etching

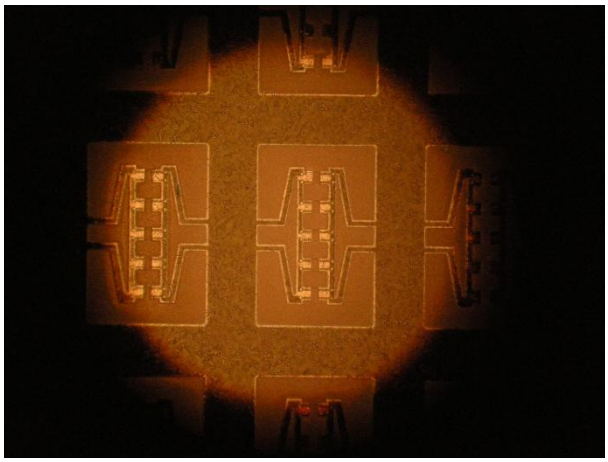
After electroplating gold growth we have to remove all linking layers between devices. In fact, at this point all devices are shorted each other thanks to Cr-Au metallic thin layer. So, first of all, we remove the upper photoresist with acetone. We dissolve only this resist layer without penetrating in the below one because it is separated from the top layer by metallic template. Second one we etch the conductive layer using 15” Au etch solution followed by 5’’ Chrome etch solution. After the elimination of conductive layer all devices are separated and we must only remove bottom photoresist with acetone. With this step we eliminate the material under the bridges, so these structures are now suspended on the air. Step processes are finished and the results are shown in Figure 4.27.



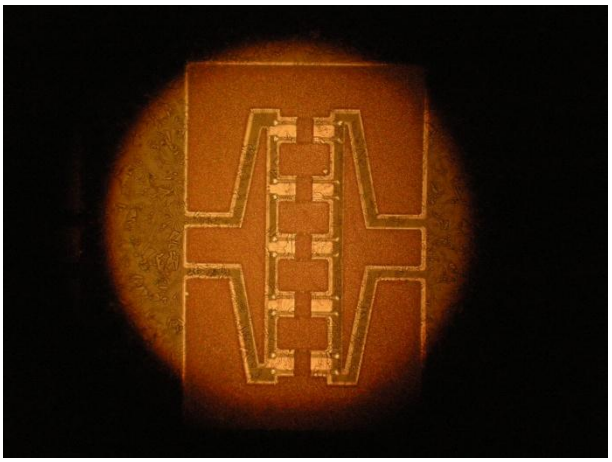
(a)



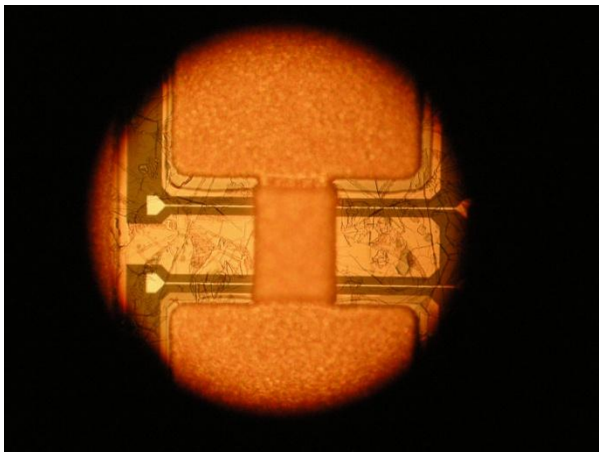
(b)



(c)



(d)

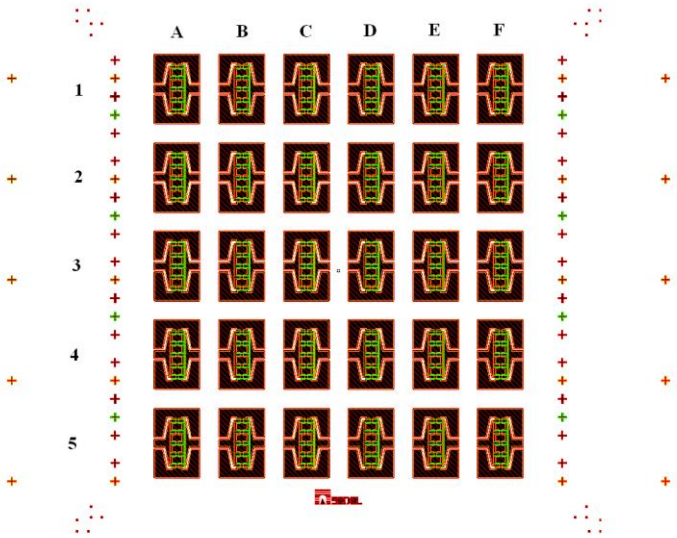


(e)

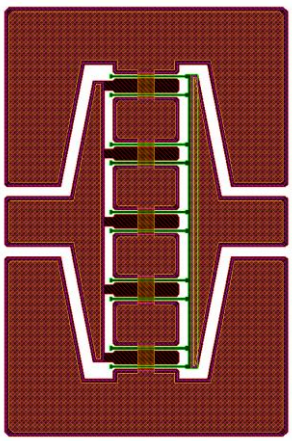
Figure 4.27 – (a) schematic and (b) - (e) results of multi-finger MESFETs process. We can see the use of air-bridge to connect source pads and to thicken contacts pads.

4.5 Process results

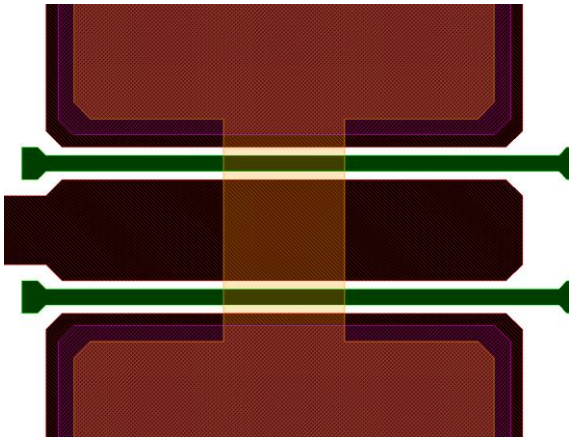
The group of steps previously listed has brought to the manufacturing of polycrystalline diamond multi-finger MESFET transistors. At the end of process we have the following situation:



(a)



(b)

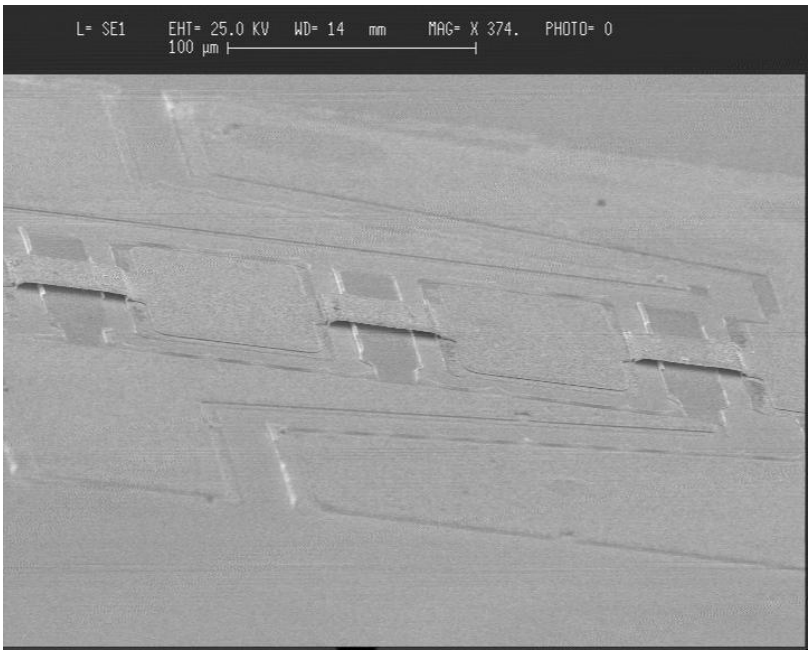


(c)

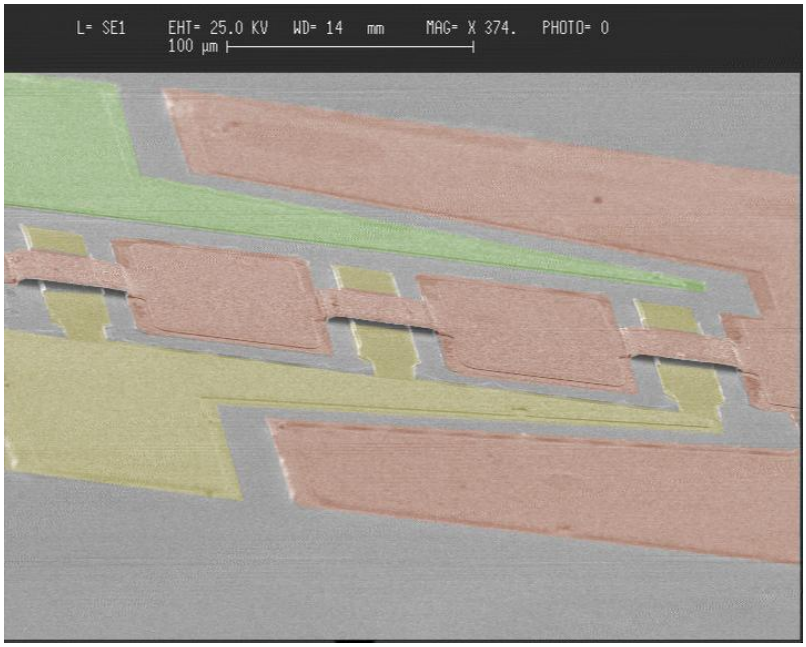
Figure 4.28 - (a) Final situation over a single diamond sample. We have 30 devices with different gate lengths but fixed width (b) single MESFET device LASI 7 picture (c)MESFET drain-source-gate detail.

As shown in figure 4.28, over each sample we have 30 transistors with a fixed gate widths and different gate lengths. The distance between Drain and Source is 8 µm for all MESFETs, width is 100 µm for all of them, while Gate length varies from 0.5 to 4.0 µm. The gate fingers are set in the middle of Source-Drain distance.

In Figure 4.29 (a) a multi-finger MESFET SEM image is shown and precisely it refers to a process without manufacturing fingers gate. In Figure 4.29 (b) we can see the same image where all different contacts are highlighted: the gate pad (without fingers) is in green, the drain pad in yellow and the source one is red. It's possible to see the air-bridges that connect all source pads passing over other contacts.



(a)



(b)

Figure 4.29 - (a) Multi-finger MESFET structure without fingers gate. (b) we can see the same image where all different contacts are highlighted: the gate pad (without fingers) is in green, the drain pad in yellow and the source one is red.

Chapter 5

Inductors and Capacitors manufacturing

5.1 Inductors and Capacitors processes

As we've previously made for multi-finger MESFETs, in Figure 5.1 is shown the list of the whole processes (in parallel) to produce diamond inductors and capacitors.

INDUCTORS PROCESS	CAPACITORS PROCESS
1. SUBSTRATE CLEANING	
30' at 100 °C in sulfochromic acid mixture ($K_2Cr_2O_7$ + H_2O+ H_2SO_4)	
15' in aqua regia (3HCl + 1HNO_3)	
15' in Kalish's mixture (1HNO_3 + 1$HClO_4$ + H_2SO_4)	
20' piranha clean (5H_2SO_4 + 1H_2O_2) @120°C	
15' in hot trichloroethylene	
15' in hot acetone	
15' in hot isopropyl alcohol	
2. FIRST METAL LAYER (TURNS AND LOWER PLATE)	
positive photoresist: S1818	
spinning conditions: 60"@4000 rpm	
bake: 2'@120°C	
exposure: 25"	
post exposition bake: 60"@120°C	
Development: 40" with MF322 solution (1:6 - MF322:Water)	
Thermal Evaporation: 50 nm Ti/Au (20/30 nm) - growth rate: Ti 0.25 nm/s, Au 0.30 nm/s	
Metal lift-off with acetone	

3. NO STEP

3. DIELECTRIC DEPOSITION

Dielectric deposition: PE-CVD Si_3N_4 - rate 250 nm/h

Si_3N_4 patterning using photoresist

Dry etching ofSi_3N_4: RIE CF_4 + 8%O_2 - rate 2 μm/h

4. PIERS/ CAP LAYER DEFINITION

positive photoresist: S1818

spinning conditions: 60”@4000 rpm

bake: 2’@120°C

exposure: 30”

Development: 40” with MF322 solution (1:6 - MF322:Water)

5. METALLIC TEMPLATE DEPOSITION

Evaporation: 20 nm Cr

Sputtering: 200 nm Au

5. BRIDGE DEFINITIONS

positive photoresist: S1818

spinning conditions: 60”@4000 rpm

bake: 2’@120°C

exposure: 30”

Development: 40” with MF322 solution (1:6 - MF322:Water)

6. AU ELECTROPLATEING

electroplating bathe: 15’ in Sodium dicyanoaurate $Na[Au(CN)_2]$ @ 55°C and 30 mA

Water bathe: 10’’ @ 55°C

Electroplating gold thickness: ≅ 1 μm

7. PHOTORESIST REMOVAL AND WET ETCHING

Top photoresist removal with acetone

15” metallic template Au etching (400g:100g:400ml - I_2:KI:H_2O)

5” metallic template Cr etching (2:3:12 - $KMnO_4$:NaOH:H_2O)

Bottom photoresist removal with acetone

Figure 5.1 – List of steps used to inductors and capacitors manufacturing.

Because we have just discussed all the steps in the previous paragraph, except for dielectric deposition, we don’t explain again all the steps but we will show what we have manufactured, always making a parallel between inductors and capacitors.

First of all we don't need a conductive surface, so it's not necessary making an hydrogen plasma process. In fact, as explained in Chapter 2, for passive elements an high resistive substrate is fundamental to reduce losses. So we can directly pass to first metal layer lithography as shown in Figure 5.2 (a) (c) (e) for inductors process and Figure 5.2 (b) (d) (f) for capacitors one. With this layer we define inductor turns, capacitor first plate and all alignment makers.

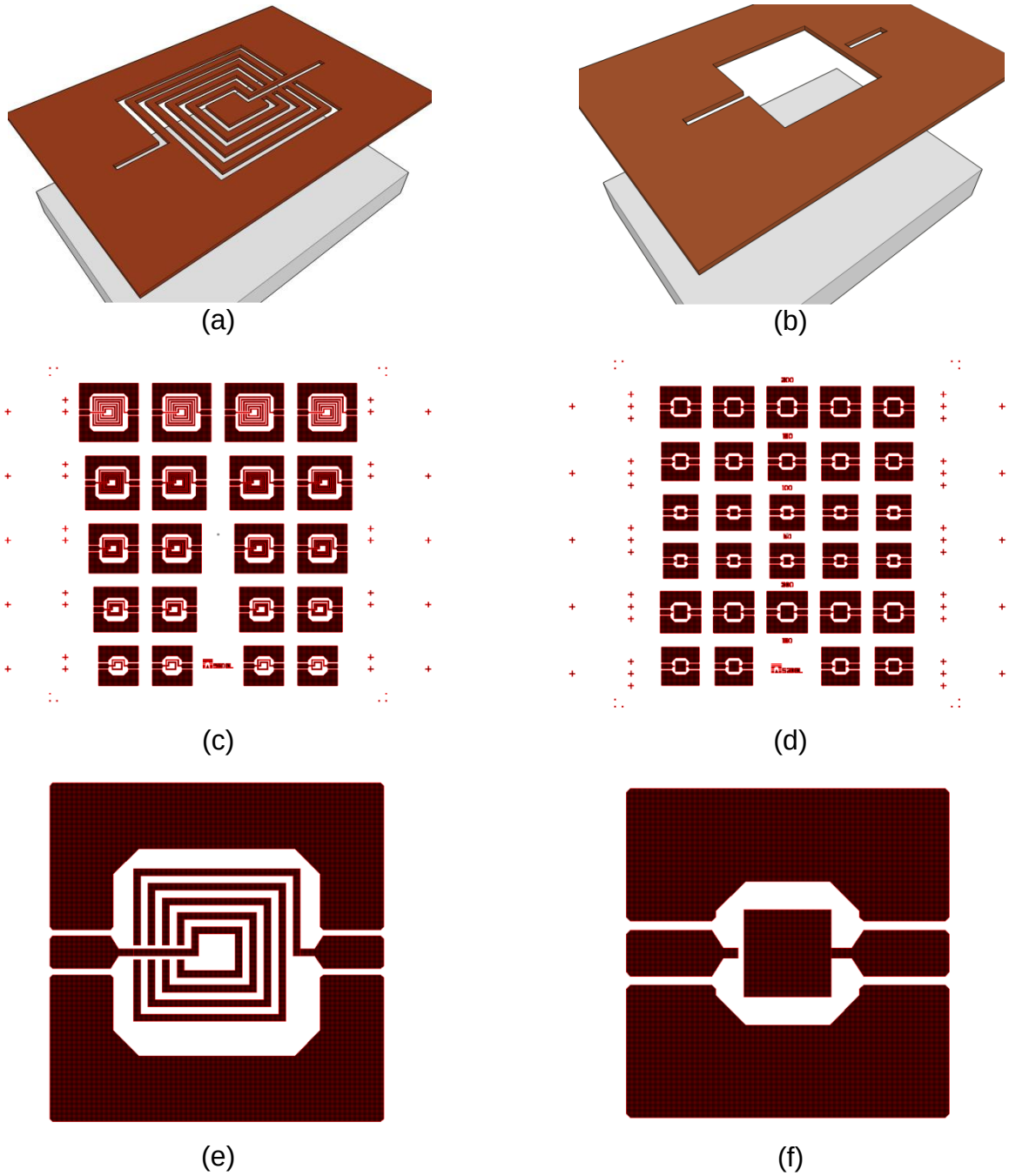
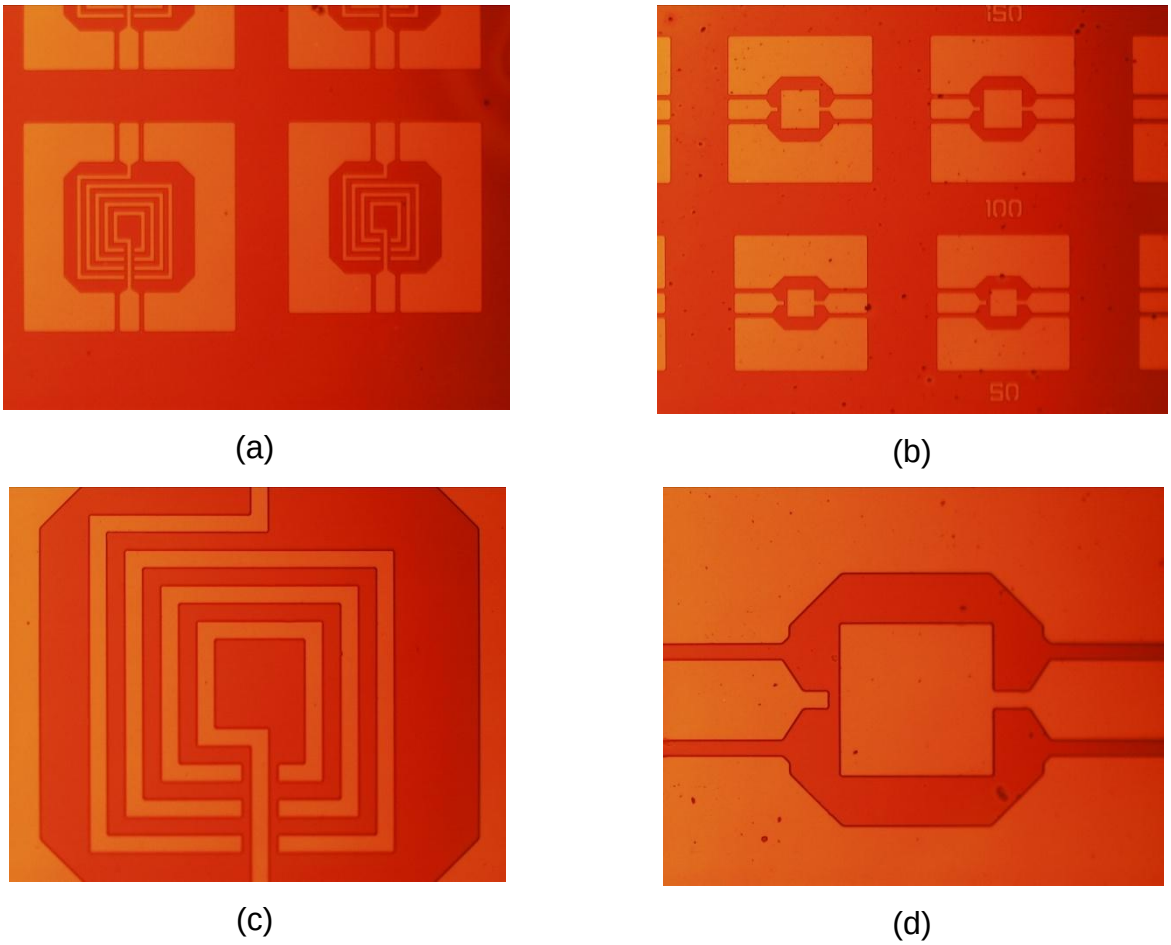


Figure 5.2 - (a) and (b) Schematic of first metal layer (b) total first metal masks designed with LASI 7 software for (c) multi-turns inductors and (d) squared capacitors. (e) (f) devices detail.

After exposuring and following photoresist development, we obtain the results as shown in figure 5.3.



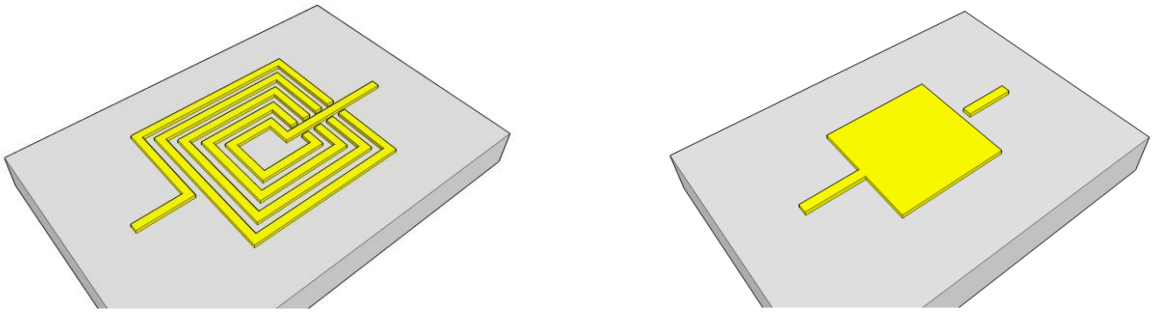
(a) (b)

(c) (d)

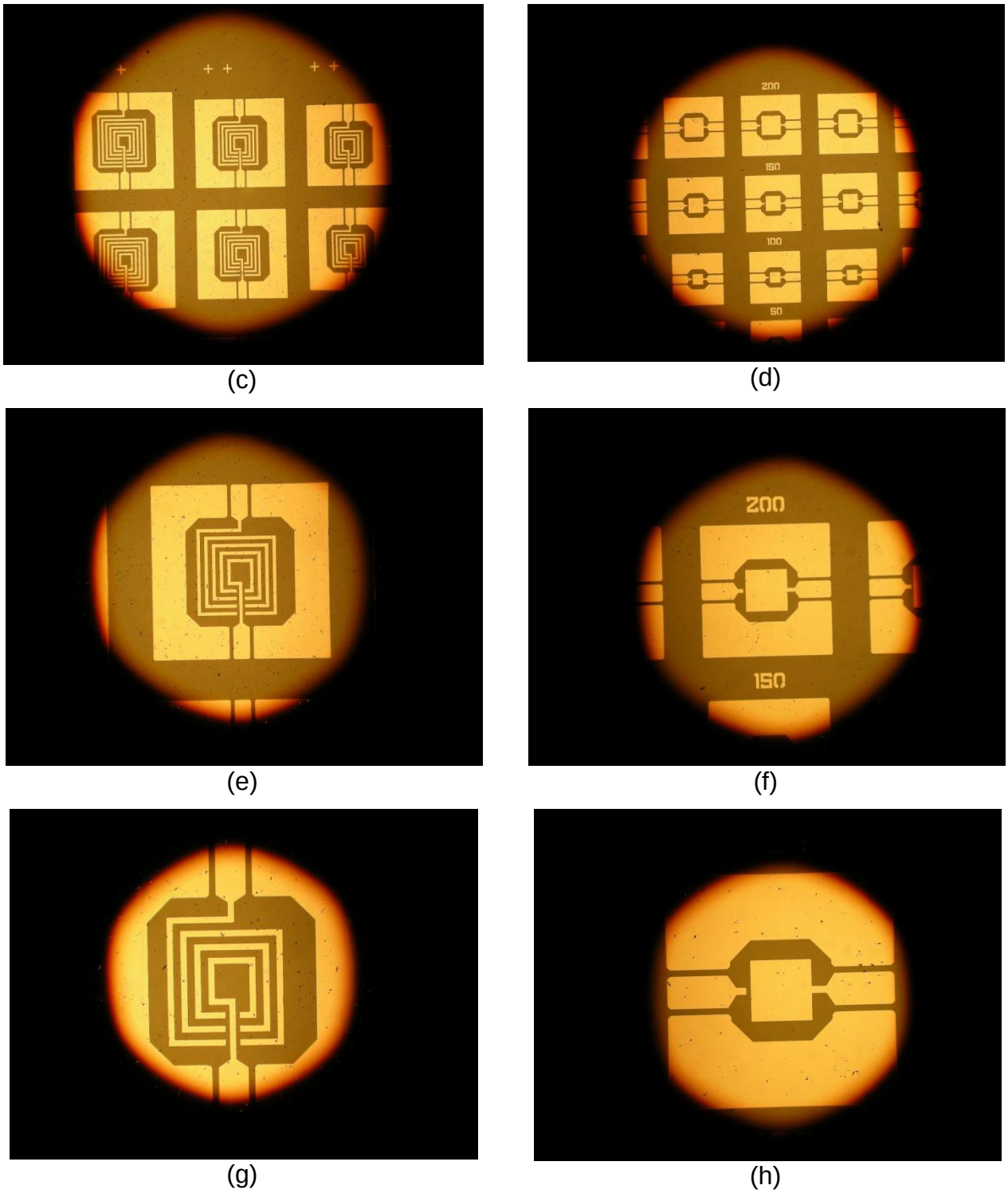
Figure 5.3 - Microscope photos of diamond samples after first step resist development. We can appreciate the coil inductor and squared capacitor.

Then we have evaporated 20 nm of Titanium and 30 nm of Gold using a *thermal evaporator* as first metal layer. Next step is the metal lift-off with acetone. This step is very critical especially for inductors because the narrow spacing between conductors makes acetone penetration inside the structure very difficult.

After lift-off we have the situation shown in Figure 5.4



(a) (b)



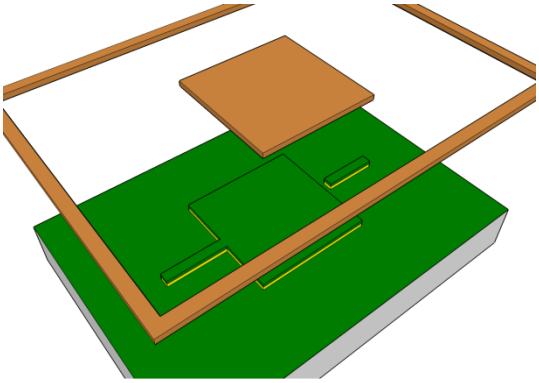
(c) (d) (e) (f) (g) (h)

Figure 5.4 - (a)(b) Schematic and (c)-(f) some microscope photos at different magnifications of diamond inductors and capacitors after Au evaporation and lift-off. We can see the classical multi-turn inductor structure.

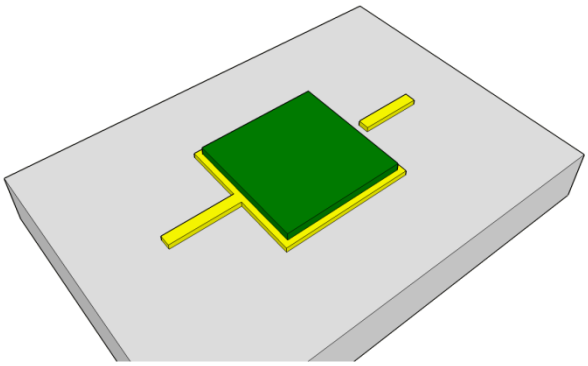
At this point we need a step applied only for capacitors. In fact we must deposit dielectric material to permit capacitors construction. At the beginning we have designed our process

to use Si_3N_4 as dielectric material, so we've divided the process into three steps (Figure 5.5):

- Si_3N_4 film deposition over the entire sample (PE-CVD: rate 250 nm/h)
- Si_3N_4 patterning using photoresist
- Si_3N_4 dry etching with RIE CF_4 + 8%O_2 (rate 1 μm every 30')



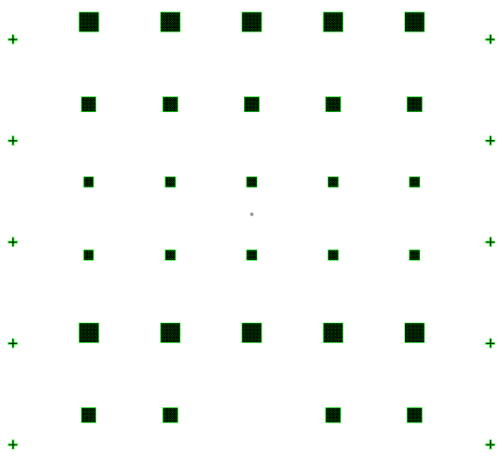
(a)



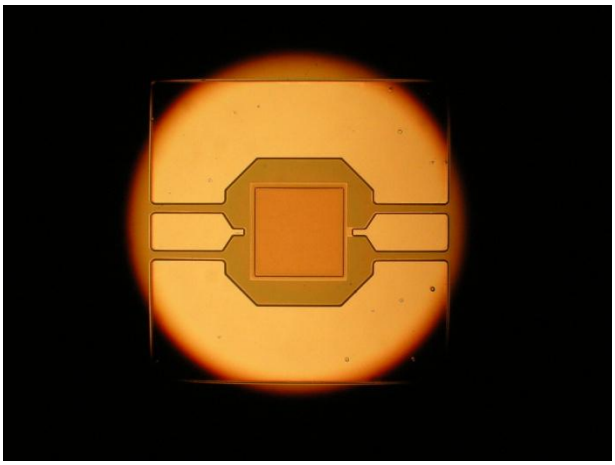
(b)

Figure 5.5 – Schematics of (a) lithographic process over Si_3N_4 layer and (b) final result after dry ething.

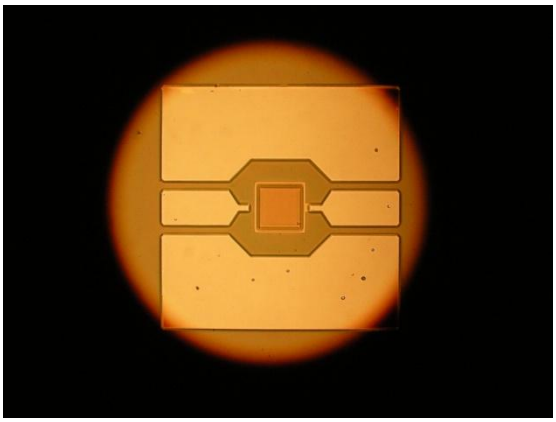
During devices manufacturing we had a problem with PE-CVD (Plasma Enhancement Chemical Vapour Deposition) so we decided to change our dielectric material and use photoresist. To make this, we have used the negative mask of dielectric step (in this case we define an area of material, in the previous one we etch an area and define it with etching) – Figure 5.6. We made the same process of Paragraph 4.4.4 except for Hard baking time that was of 30'. So at the end of the process we have 2 μm thick dielectric material made by optical photoresist with a dielectric constant $\varepsilon_r = 2.6$.



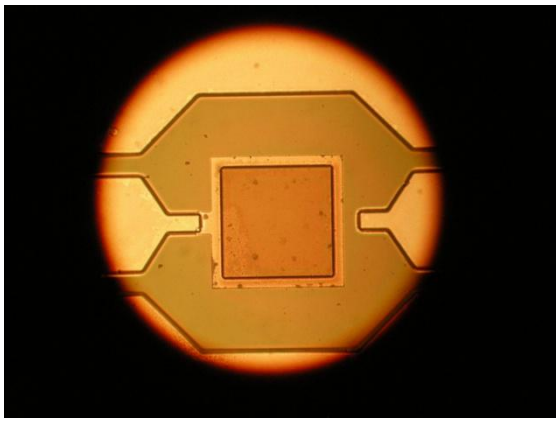
(a)



(b)



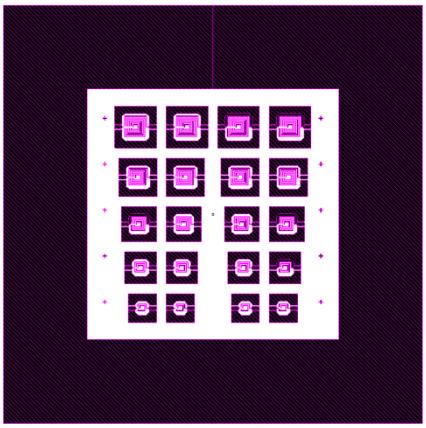
(c)



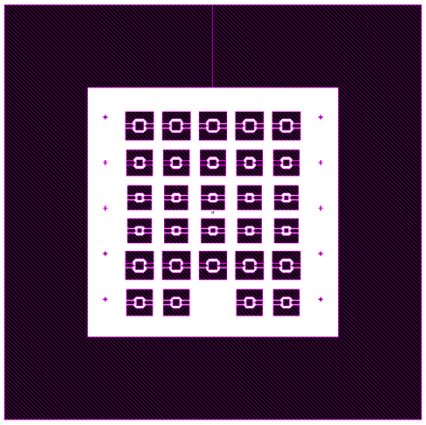
(d)

Figure 5.6 – (a) Dielectric mask an (b)-(d) photos at different magnifications of diamond capacitors after dielectric deposition step. The dielectric is made by 2 μm thick optical photoresist with dielectric constant ε_r = 2.6.

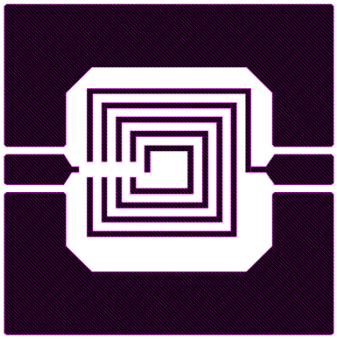
After this we can again process parallel either inductors or capacitors. So the next step, as far as inductors concern, it's used to define piers of air bridge and all the areas where we want to thicken metal while, for capacitors, it's used to define cap layer (top plate) in addition to thicken metal too.



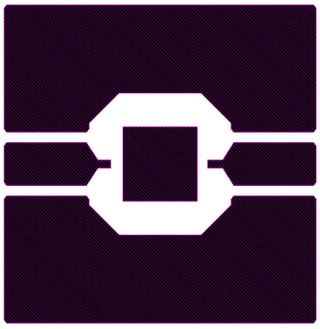
(a)



(b)



(c)



(d)

Figure 5.7 - (a) (b) piers definition total masks and (c) (d) devices details.

Now we need to realize a thin metal layer (seed layer) necessary to obtain the potential distribution for next electroplating growth: we evaporate a layer made by Chromium and Gold. The last one can be evaporated or sputtered.

Over this template we need to define the areas where we want grow the electroplating gold. So we expose the masks shown in Figure 5.8. In this way we select the areas where the bridge must be manufactured.

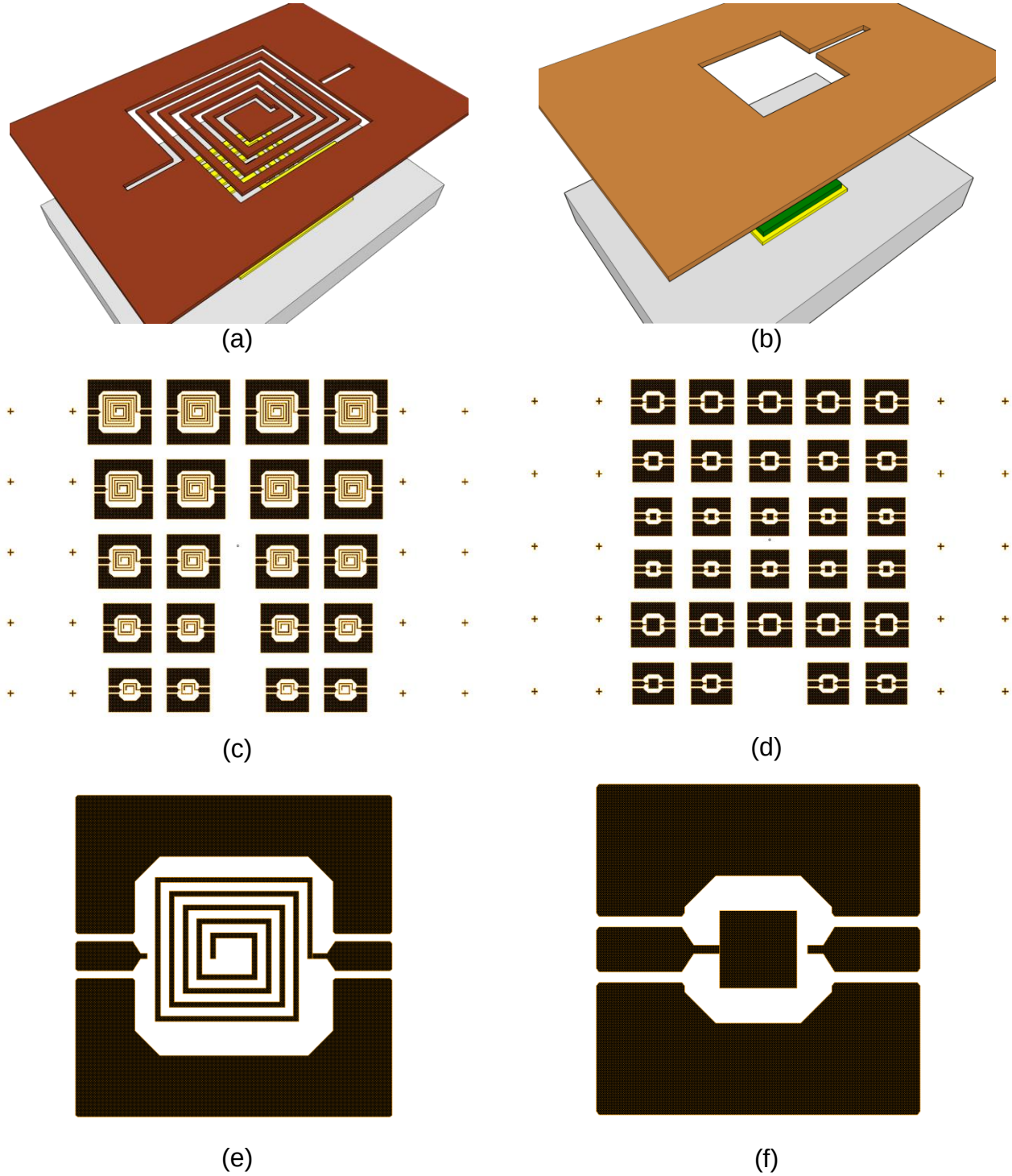
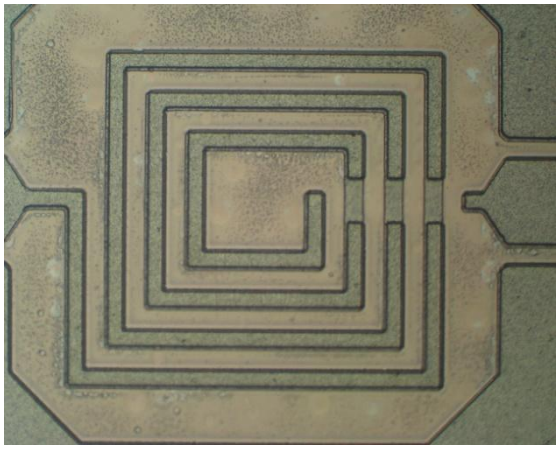
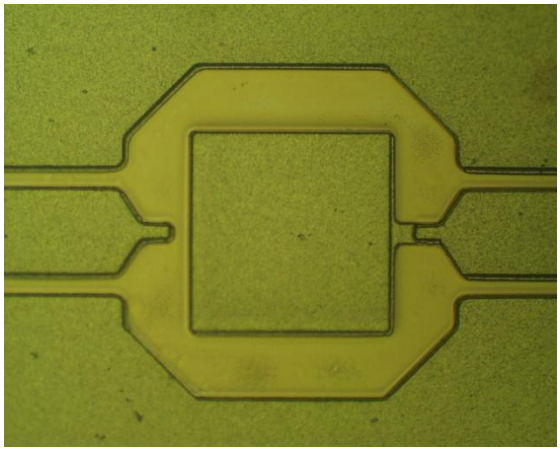


Figure 5.8 - (a) (b) Schematics of bridge definition (c)(d) total masks and (e)(f) devices details.

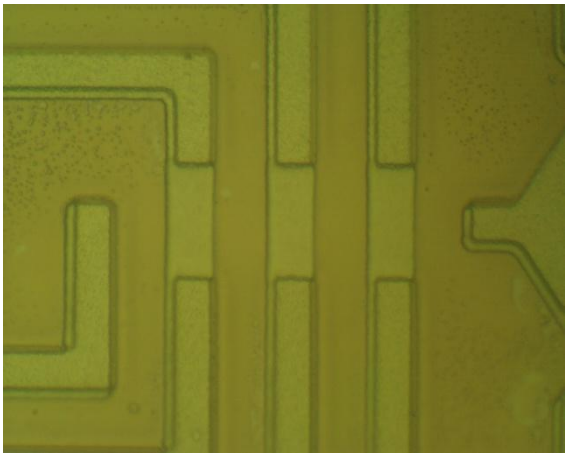
We are now ready to grow electroplating gold. After 15 minutes of growing we obtain the situation shown in Figure 5.9. We notice that electroplating gold is grown only when the template gold is unmasked.



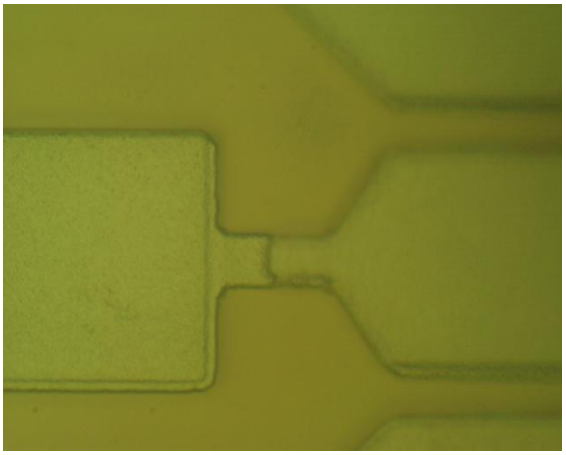
(a)



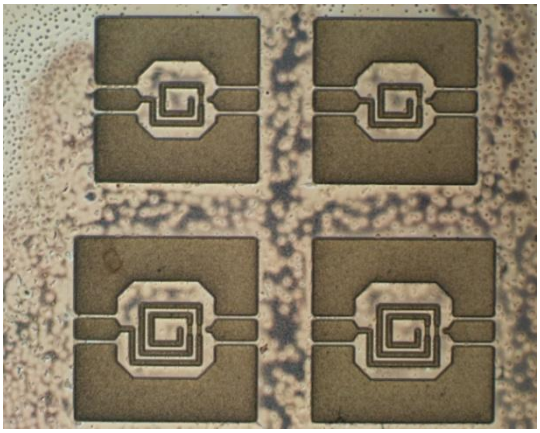
(b)



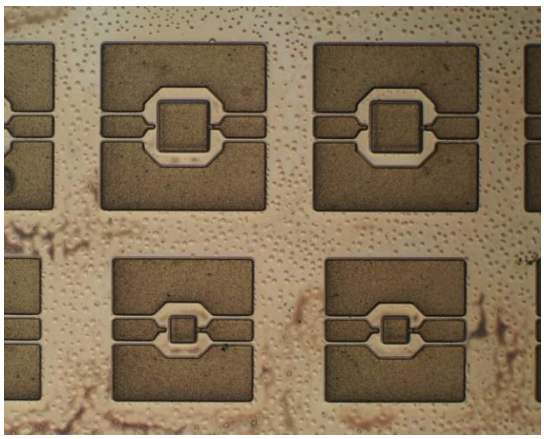
(c)



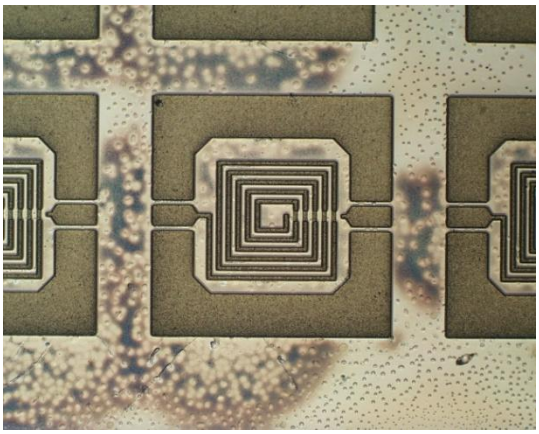
(d)



(e)



(f)

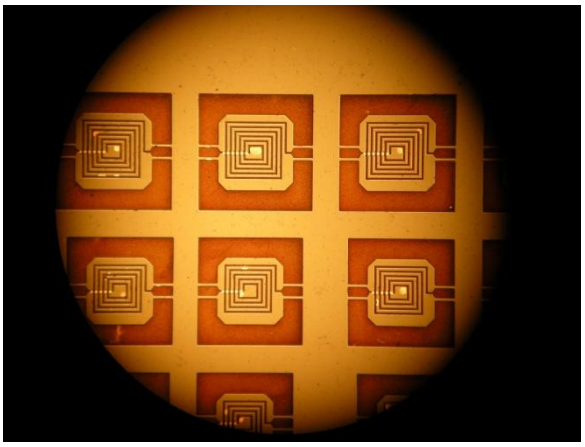


(g)

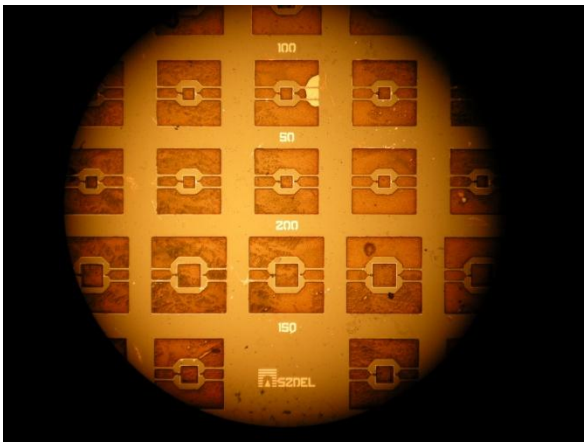
Figure 5.9 - (a) - (g) Microscope photos after Au electroplating. (c)(d) Details of bridge growth: we can note an alignment problem during the process.

With this step we have finished all the lithographic ones. Only wet processes remain. First of all we must remove the upper photoresist layer. That means photoresist used to define electroplating growth. For this we bathe our sample in acetone. Then we etch metallic template using wet etching for gold (400g:100g:400ml - I_2:KI:H_2O) and chrome (2:3:12 - $KMnO_4$:NaOH:H_2O).

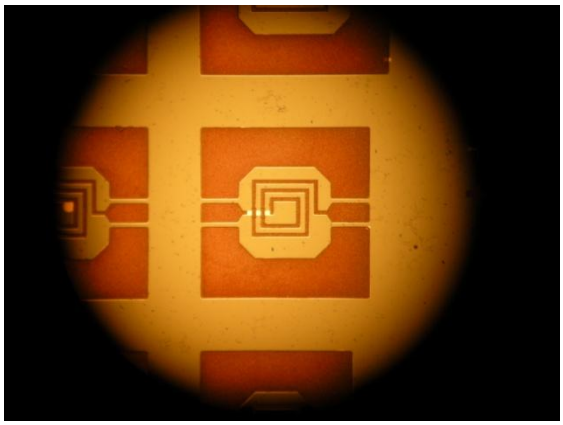
In this way we have broken electrical continuity (obtained by metallic template), so all devices are now separated. Last step is bathe again the sample in acetone to remove the first photoresist layer used to define piers of air bridges and all the areas where we want to thicken metal. Devices are now completed and the results are shown in Figure 5.10.



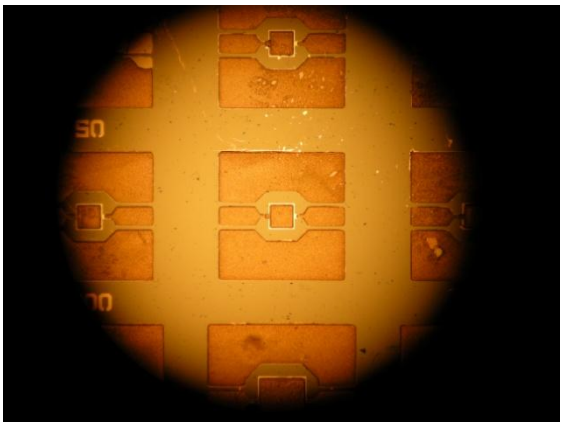
(a)



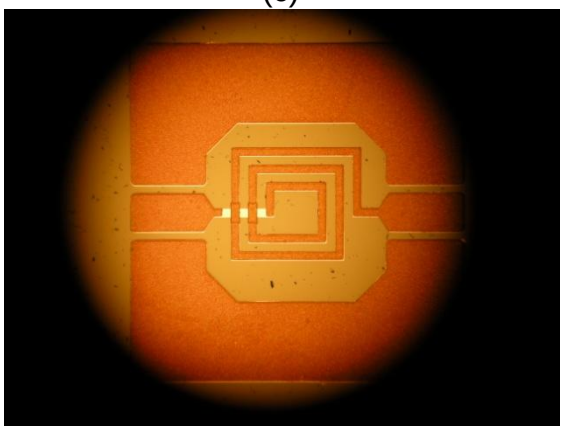
(b)



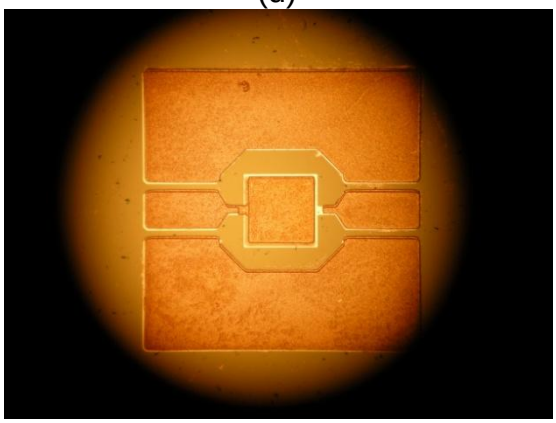
(c)



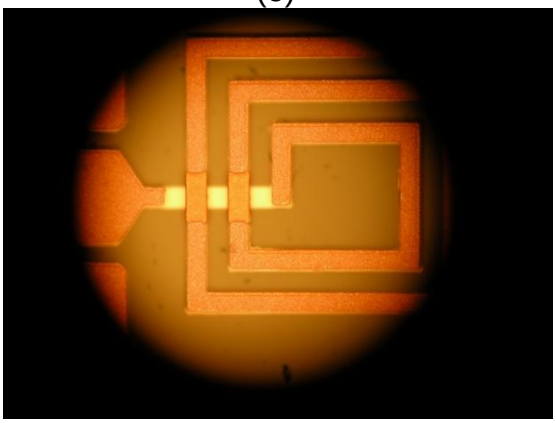
(d)



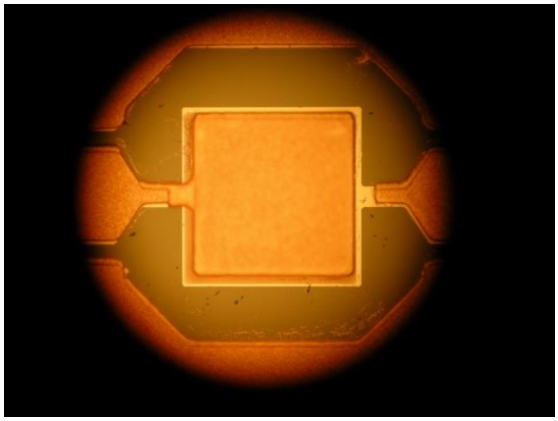
(e)



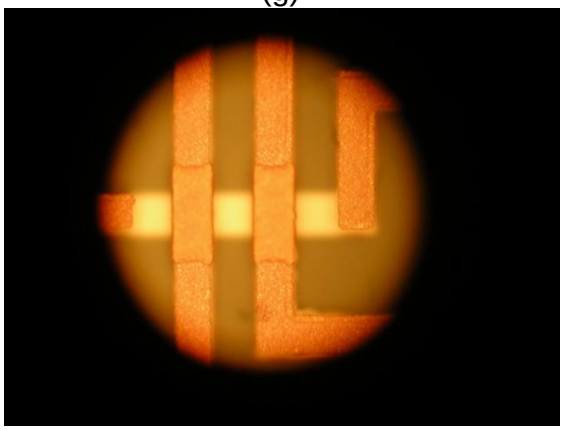
(f)



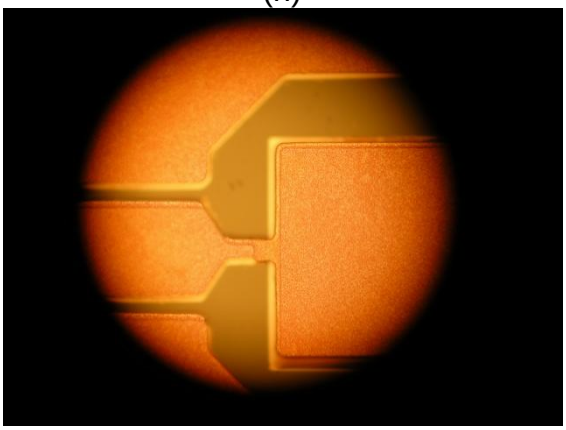
(g)



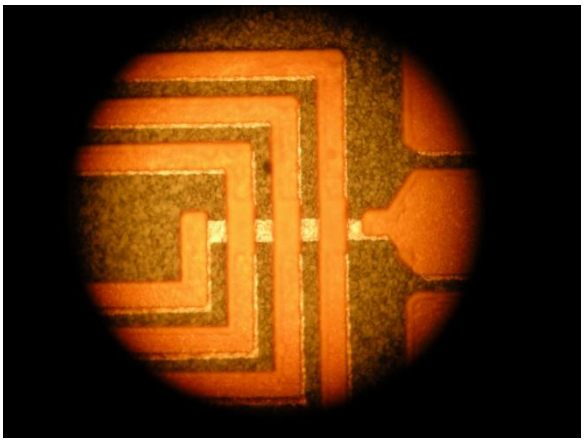
(h)



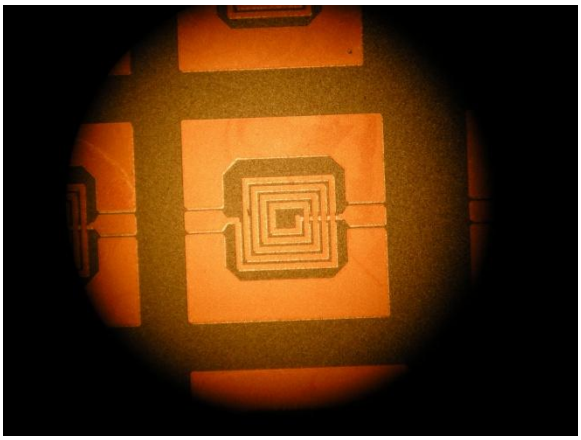
(i)



(l)



(m)

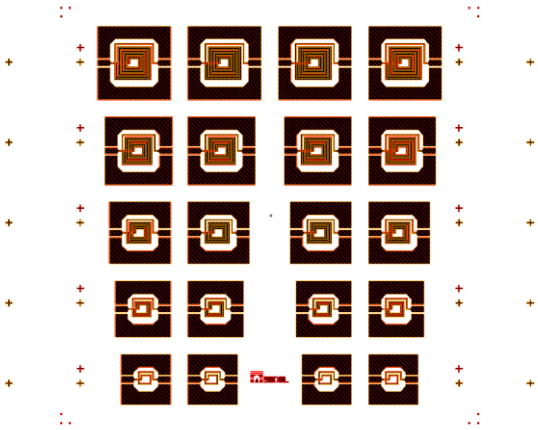


(n)

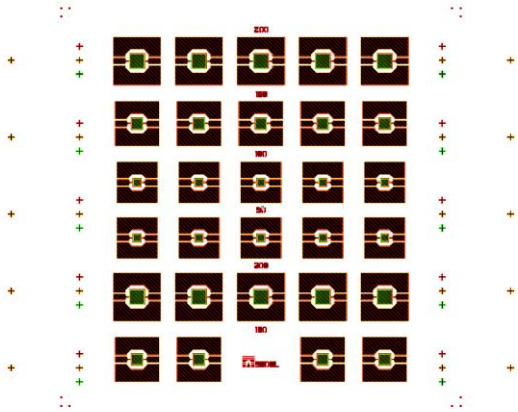
Figure 5.10 - (a) - (n) results of multi-turns inductors and capacitors process. We can see the use of air-bridge to connect turns each other and the capacitor top layer with external pad.

5.2 Process results

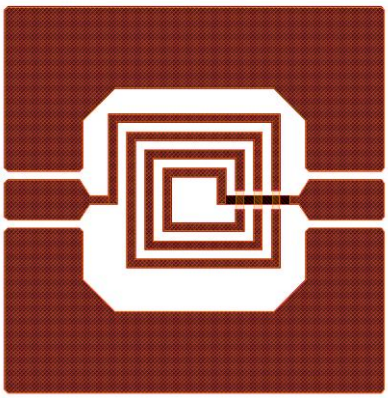
The group of steps previously listed has brought to the manufacturing of polycrystalline diamond inductors and capacitors. At the end of process we have the following situation shown in Figure 5.11:



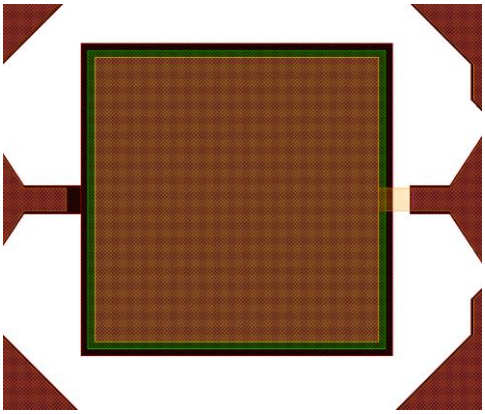
(a)



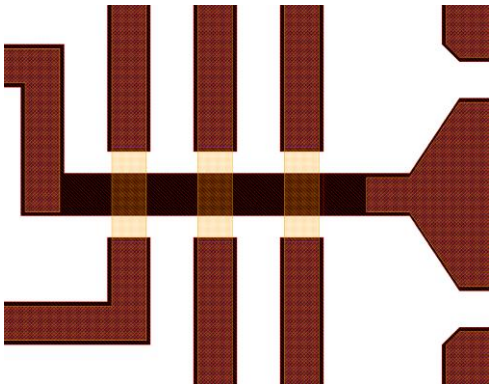
(b)



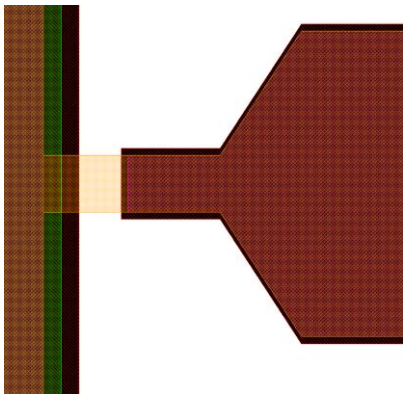
(c)



(d)



(e)

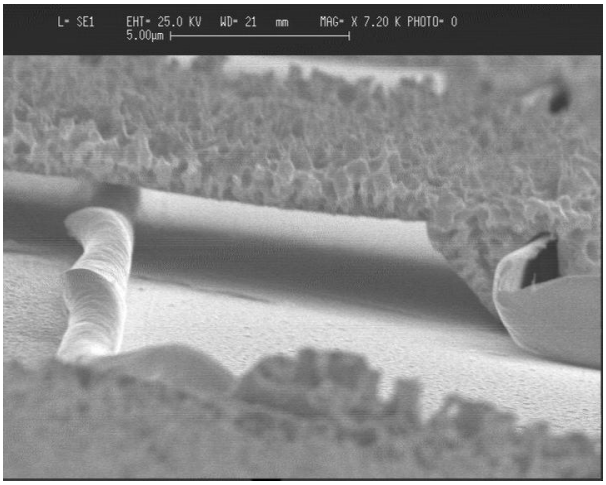


(f)

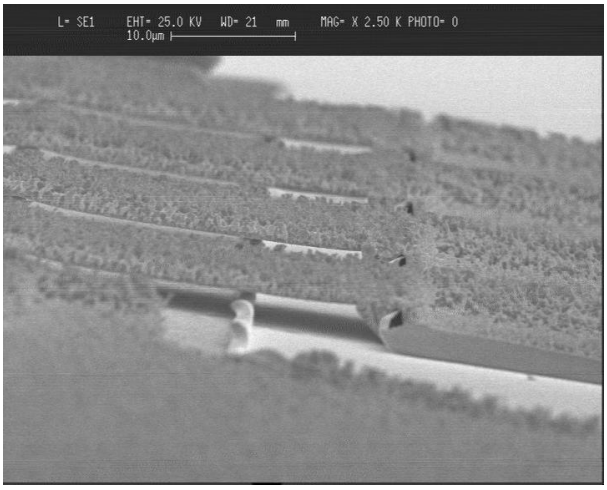
Figure 5.11 – INDUCTORS: (a) Inductors map. Final situation over a single diamond sample. We have 20 devices with different number of turns n but fixed conductor width W and spacing S (c) single Inductor device LASI 7 picture (e) Inductor air-bridge detail. CAPACITORS: (b) Capacitors map. Final situation over a single diamond sample. We have 29 devices with different plates areas but fixed dielectric height (d) single Capacitor device LASI 7 picture (f) Capacitor air-bridge detail.

INDUCTORS

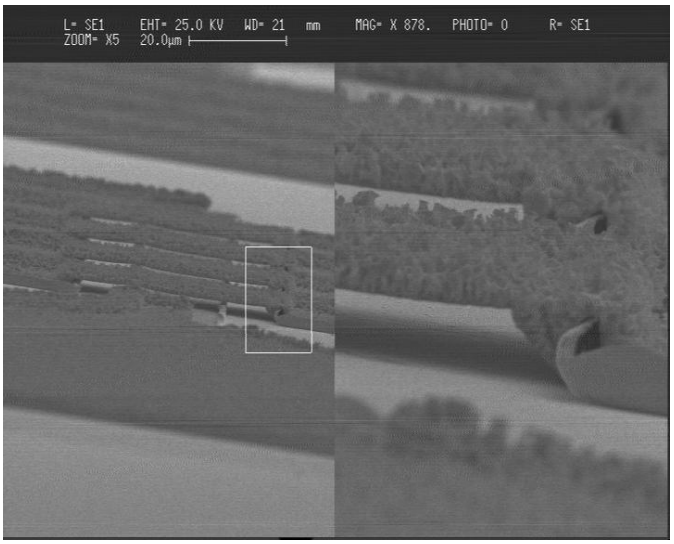
We can see 20 devices characterized by different number of turns. For all these passive elements we have the following parameters: conductor width *W*=20 μm, spacing between turns *S*=20 μm, inner diameter D_i=100 μm. The only parameter we change is the number of turns *n:* from the top of picture we have 5.5 turns and we arrive to 1.5 turns at the lower row, so going down the picture we subtract one turn each time. In Figure 5.12 we can see some images of inductors results.



(a)



(b)



(c)

Figure 5.12 – INDUCTORS: (a) - (c) Inductors final situation after all technological steps. In this case we can note a not perfect Ti/Au lift-off but a good removal of resist under bridges.

CAPACITORS

As far as capacitors concern, we have 29 devices with different plates areas. For these squared devices we have three basic parameters: plates area A, that we change from 50x50 μm^2 to 200x200 μm^2 , dielectric thickness *d* that we assume 2 µm height and material dielectric constant ε_r that is 2.6 for our material.

Chapter 6

Technological issues

6.1 Problems

During samples processing a lot of problems have been handled: sometimes they have caused remaking of steps and sometimes processes abort. This has been object of careful analysis and it has led us to the clearing of noticed problems. Here in after all the problems and their solutions are shown.

Meniscus effect. Due to the small sample surface used to device manufacturing (1x1 cm^2), during photoresist spinning we had no-perfect uniformity of resist deposition along the borders, where there is a slight swelling called *"meniscus effect"*. This reduces the work area: in fact we must exclude the peripheral area because here the lithographic process couldn't be fine. In Figure 6.1 this effect is shown.

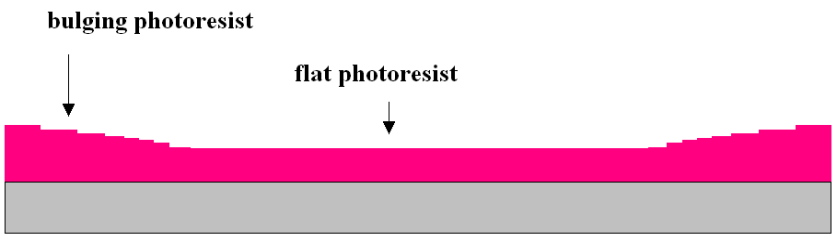


Figure 6.1 – Meniscus effect after photoresist spinning.

Gold adherence and contacts borders uplift. One of the most important problems noticed during all processes has been the gold adherence on diamond substrate. In fact the ohmic contact lift-off process using acetone has removed the gold of the contacts too. The bad adherence of gold over a large range of materials is a feature of this metal due to its intrinsic

properties as slow electronic affinity. A further cause could be the diamond surface cleaning, especially after hydrogen plasma step. We have overcome this problem making a deep cleaning of our sample and changing material for our ohmic contacts. In fact we used Ti/Au instead only Au. The first thin layer of Titanium (thick: 20 nm) is necessary to improve the adherence of contact: thanks to his properties Titanium has a good grip on diamond. (Figure 6.2)

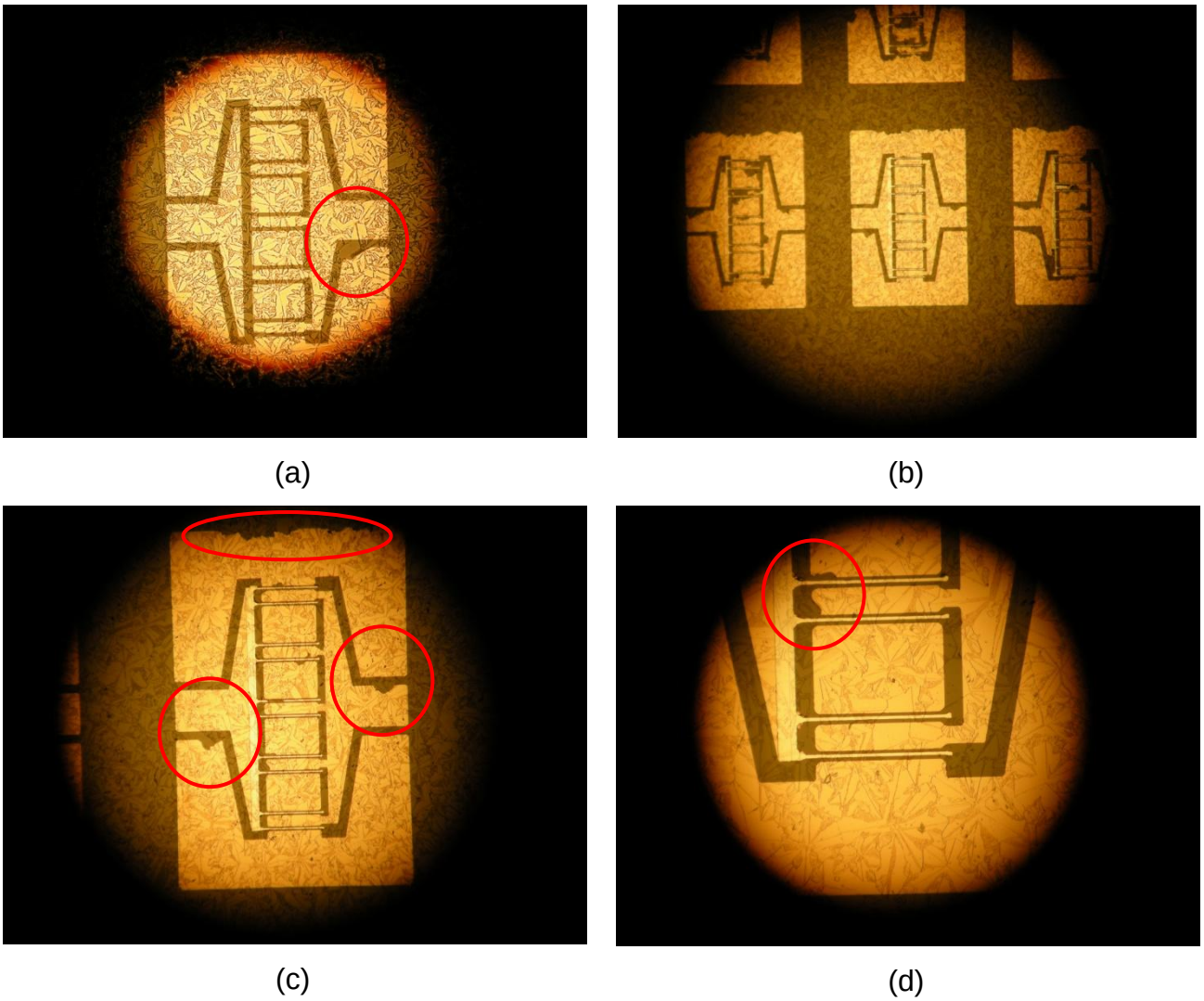


Figure 6.2 – Bad Gold adherence and contact borders uplift after Au lift-off for ohmic contact construction.

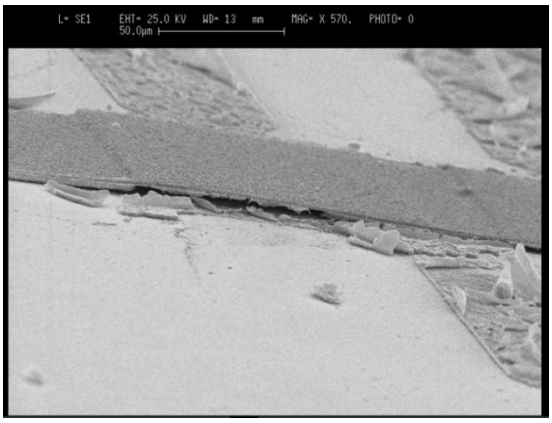
Lithographic limits. We have just said that we have used optical lithography with a mask aligner aid for all steps, except for E.B.L. gate. The machine resolution is about 1 um, so in theory there aren't problems for areas bigger than this dimension. We have to remember that we haven't used a diamond wafer but only a small sample (Area=1 cm^2), so we couldn't

exploit all the instrument potential. In fact there are severe problems for dimensions smaller than 4 um.

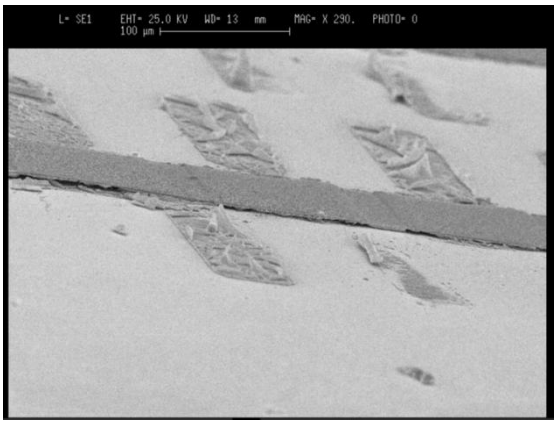
Structure collapse. The first approach to the air-bridge technique has been characterized by manufacturing different bridges under those there were several contacts (Figure 6.4.a and b). Because the length of these bridges between two consecutive piers was too long, we've observed the structure collapse. The solution to this problem has been the reduction of length bridge.

No good photoresist removal under the bridge. Repeating our process steps after we've modified the length bridge, we've encountered a new problem consisting in a no-good photoresist removal under the bridge (see Figure 6.4.c). It depends on no-good acetone penetration under the bridge caused by a too large dimension of width bridge: so we've reduced the bridge width too.

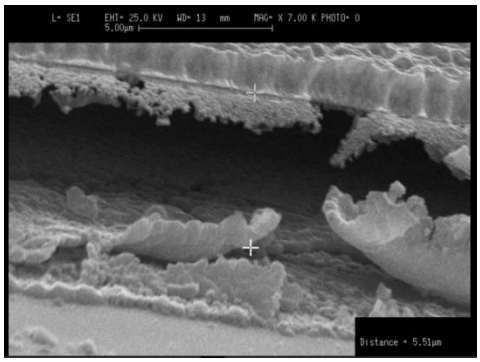
Substrate cleaning after wet etching. As described in the previous chapters 4 and 5, the last step to complete devices fabrication is the first layer photoresist removal. We have noticed that, after using acetone to eliminate this layer, some impurities remained over the substrate, as shown in Figure 6.4. To eliminate these organic residuals we use a wet etching with a greater mechanical and thermal perturbation and complete the process with 2' of oxygen plasma, with the same recipe used in paragraph 4.4.4.



(a)



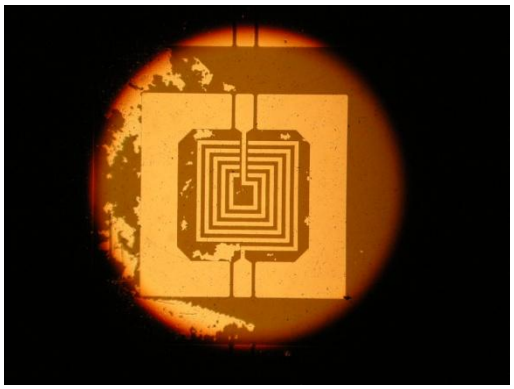
(b)



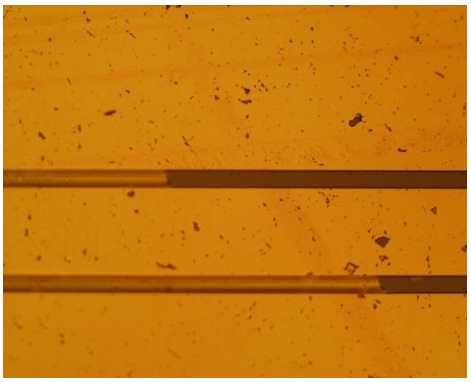
(c)

Figure 6.4 – (a) (b) organic residuals over sample after removing of first photoresist layer (c) no-good photoresist removal under the bridge: we can notice the presence of a lot of impurities.

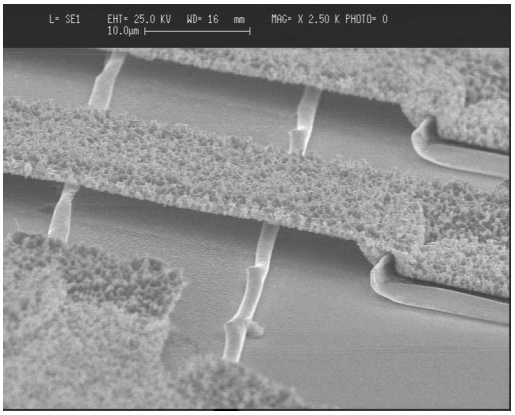
No good metal lift-off. Another problem we've met during device manufacturing has been a no-perfect metal lift-off for ohmic contact building step. In fact, as we can notice in Figure 6.5, there are some Ti/Au curls at the boundaries of ohmic contacts. This is due to a no-abrupt photoresist profile and an incisive lift-off. To solve this problem we have improved our lithography making a Post Exposition Bake just a little bit longer than the previous one and using an higher pressure lift-off processing and ultrasounds.



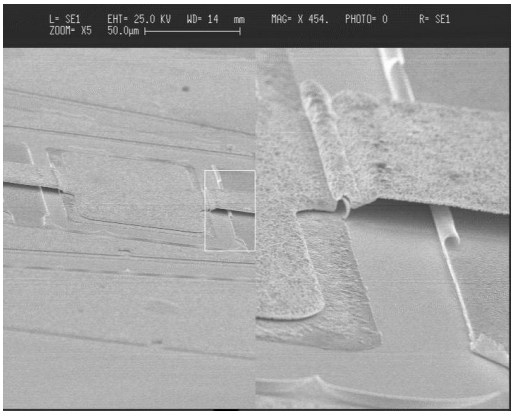
(a)



(b)



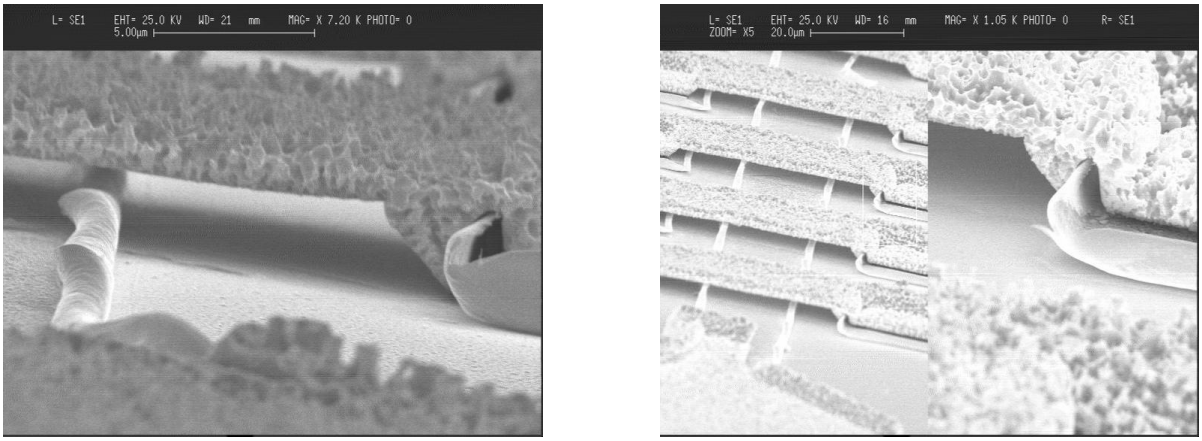
(c)



(d)

Figure 6.5 – No good metal lift-off results. (a) (b) We can see a not entire metal removal and (c) (d) metal curls at the contact boundaries.

Electroplating gold sponge effect. In Figure 6.6 is shown a not perfect electroplating gold, with a sort of sponge effect. It's due to two basic reasons: first of all we know that, to perform electroplated gold we need to a seed layer terminated by Au: this Au layer is made by using a sputtering process and not the evaporation process, so electroplated gold reflects the atomic disorder created by this process. Moreover, it should be generated by Au wet etching used to remove seed layer. Another reason could be the growth rate that depends on current flow, that was 30 mA. Reducing this flow and using evaporation instead of sputtering should minimize this effect.



(a) (b)

Figure 6.6 – Sponge effect of electroplating gold. At the same time we can see the curls at the contact boundaries.

MESFET gate stripping. A problem we encountered at the last step and only one time but it has aborted an entire MESFETs manufacturing process has been the gate-strip lift-off as shown in Figure 6.7. We can see that it has caused the electric discontinuity between the gate-fingers, that are well done and defined, and gate-pad. We don't know surely why this happened but we think about a joining of different reasons of which mechanical stress and no-perfect alignment of piers bridge definition.

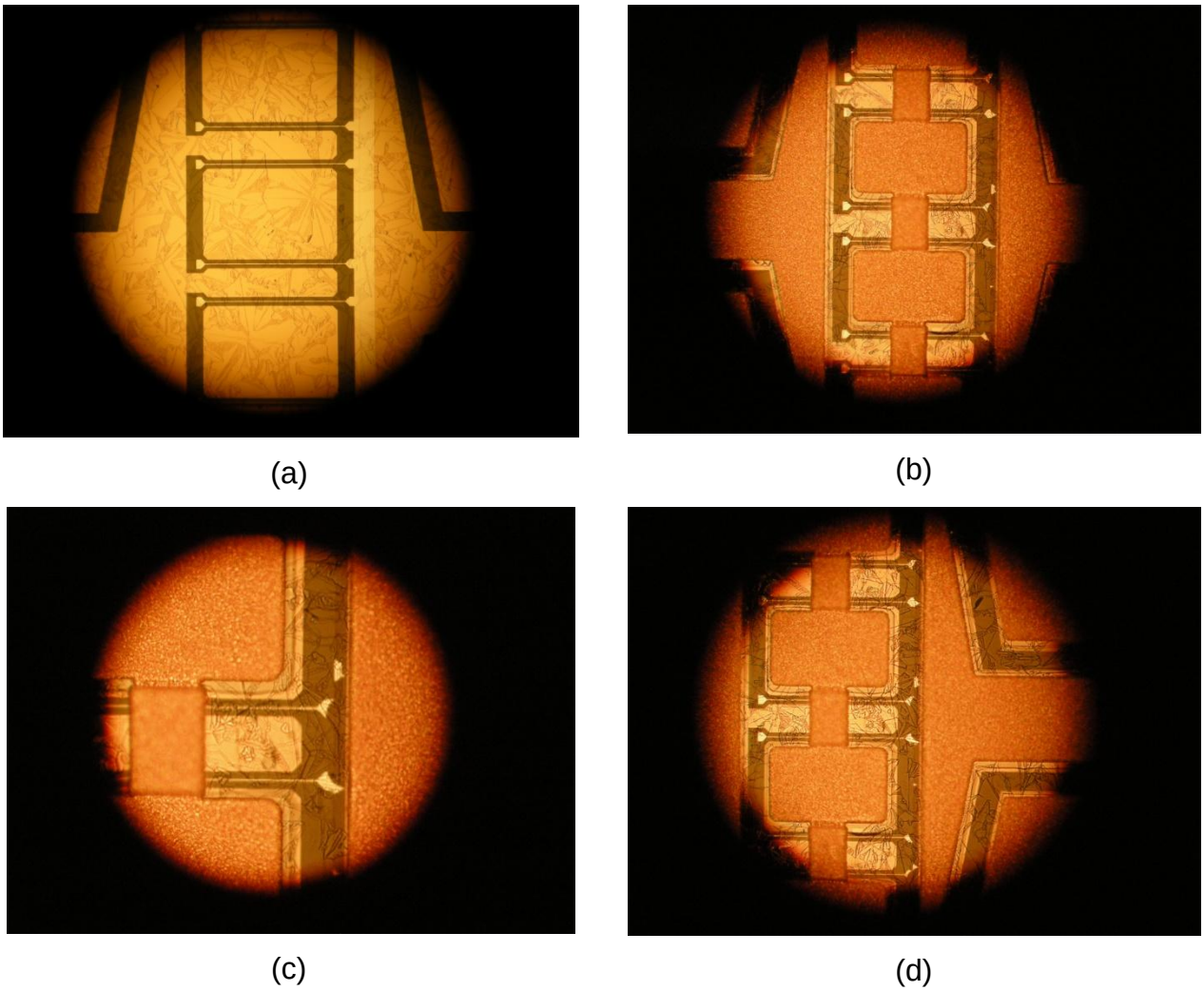


Figure 6.7 – (a) Gate stripe before electroplating growth (b)-(d) Gate stripe removal after wet etching process.

Chapter 7

Experimental systems

This chapter illustrates a series of systems and technologies used to manufacture either MESFETs devices or passive elements during this work. It's briefly described their working and their technical features.

7.1 Photoresist

Photoresist isn't a real instrumental system but it's so important to construct devices that we need to explain more information about it.

This substance is a light-sensitive polymer applied over the wafer surface in order to define areas that we must process and, at the same time, protect the rest of wafer.

Lithographic steps used to pattern photoresist can be summarized as follows:

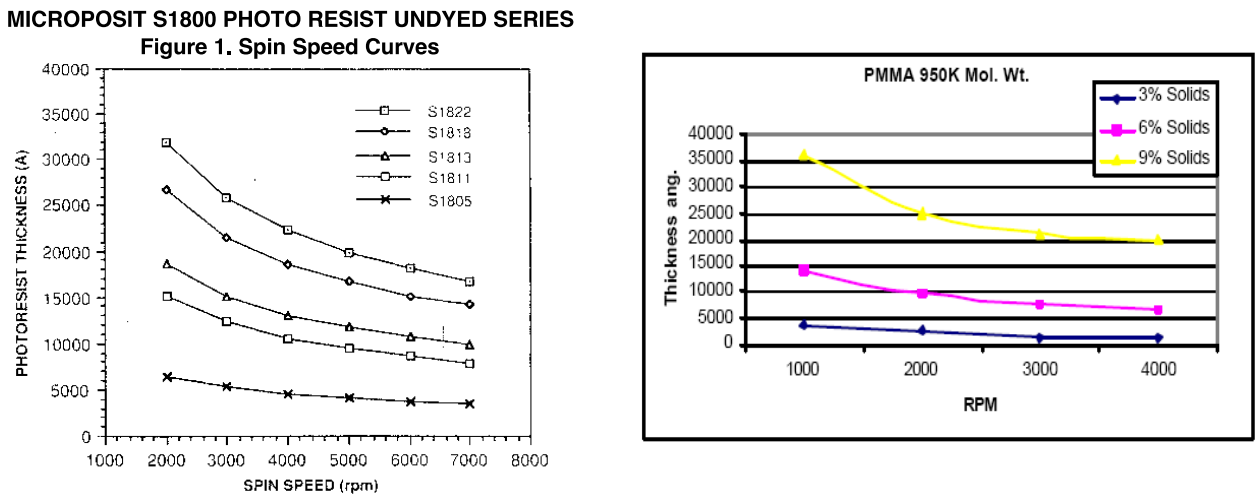
- photoresist spinning;
- soft-bake;
- exposure;
- post-exposition bake;
- development;
- hard-bake

Photoresist applying consists in the wafer insertion into the *spinner*, that is an instrument that put the wafer mounted on it in rotation, varying and controlling the velocity and processing time. During this rotation time photoresist will be spinned homogeneously over the entire surface: the thickness of this layer is a function of time and rotation speed.

A thin resist layer is used to have an higher resolution (as in the gate step), while a thick one is indicated in high energy steps (e.g. in isolation). Depending on requirements, it will be baked or not on an hot plate or oven at different times and temperatures to have:

- *soft-bake*: heating after photoresist applying on wafer, but pre-exposure, in order to evaporate the photoresist solvent;
- *post-exposition bake (PEB)*: heating after exposure, but pre-development, in order to obtain sharp photoresist borders; this step is very useful overall when we use a lift-off metal process, because we avoid continuity layer between metal deposited in the defined areas and that deposited over photoresist;
- *hard-bake*: final heating at high temperature to harden photoresist. It's useful when we submit the sample surface to molecular radiation or bombardment at high energy (e.g. ionic implantation). The secondary effect is rounding off pattern borders, reducing the spatial resolution and lift-off capability.

At this point the sample is ready to the UV exposure to provide photolithographic process.
In every photolithographic step based on optical lithography we have used SHIPLEY MICROPOSIT S1818, a positive photoresist with a resolution of < 0.48 μm if the exposure radiation has λ to the *g-line* (436 nm) at 150 mJ/cm^2, while for the gate electronic lithography we have used the FUJI-FILM PMMA resist, with a resolution better than 0.1 μm. In Figure 7.1 is illustrated the dependence of photoresist thickness with rotation velocity, for both kind of resist, as reported from their datasheets.



(a) (b)

Figure 7.1 - Dependence of photoresist thickness with rotation velocity, for (a) S1818 and (b) PMMA [13].

7.2 Mask aligner

The system used to allow phtolitographic process, so to expose and align masks, is the *mask-aligner Karl Suss MA 6*, of which some pictures are shown in Figura 8.2.

For the exposure we have used a light source, a mercury arc lamp, chilled by air, and powered by a system that secures a constant power of 275W [14].

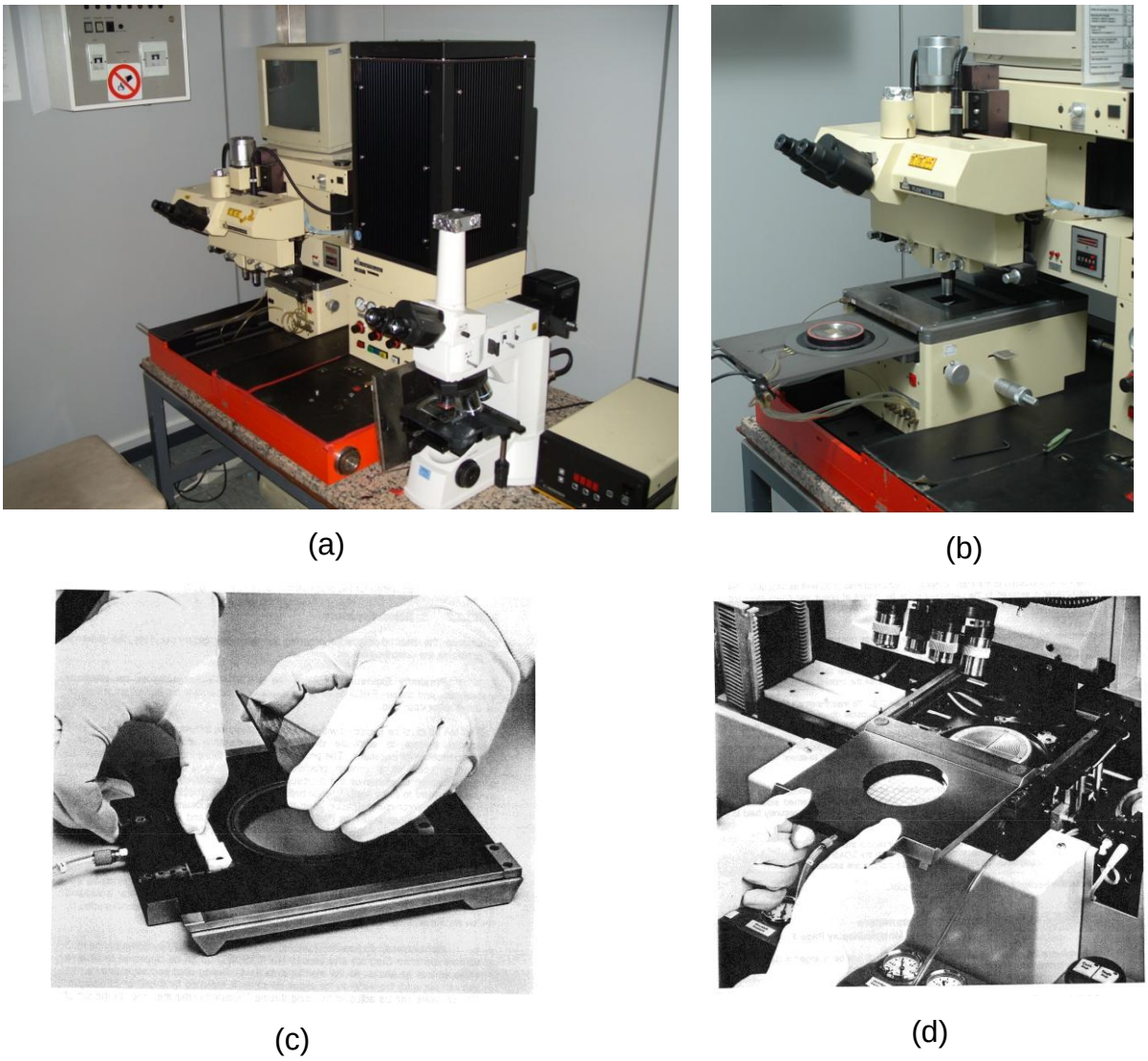


Figure 7.2 – (a) (b) Mask-aligner Karl Suss MA 6 pictures of Roma Tre Univeristy labs (c) Mask mounting on maskholder (d) Maskholder [14].

The mask aligner optical system is schematized in Figure Figura 7.3.

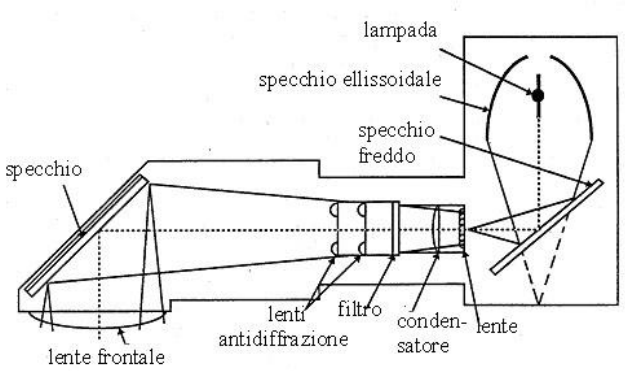


Figure 7.3 - Karl Suss MA 6 optical system draft.

To realize the alignment, Karl Suss MA 6 has an optical microscope with 10X lenses, a lighting system base on optic fiber and a movement system controlled by micrometric screws that allows freedom of movement in the X-Y plane up to ±10 mm and a rotational movement up to 3 degrees.

As far as resist exposure concern, the Karl Suss MA 6 permits two function modes:

1. *Hard contact exposure.* In hard contact mode, once the wafer is in contact with the mask and the exposure cycle starts, the vacuum that ensure wafer to the chuck is removed and the nitrogen is introduced under the wafer, in order to press the wafer to the mask.
2. *Soft contact exposure.* In this mode, the vacuum that provides to join the wafer to the chuck remains during exposure.

For our processes we have used the soft contact mode. In Figure 7.4 two kind of optical lithography are shown.

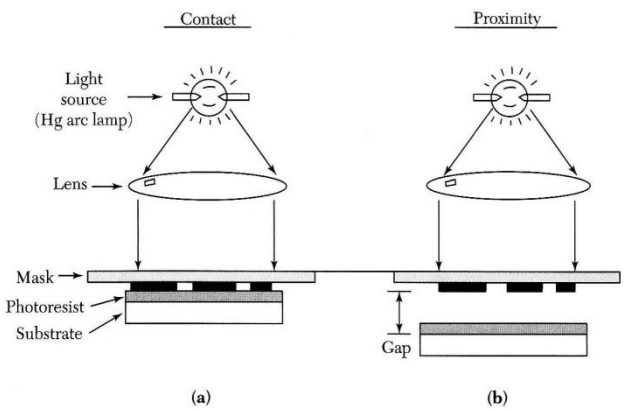


Figure 7.4 – (a) Contact and (b) proximity lithography.

7.3 Thermal evaporator (Au)

For the Ti-Au applying, we have used a thermal evaporator, that is an evaporation chamber as shown in Figure 7.5. It's constituted by a steel cylinder in which we realize an high vacuum level using rotative and cryogenic pumps. Before starting process we need to reach a pressure of about $8*10^{-7}$ mbar: this value is reached after 3 hours from pumps activation.

This low pressure value is fundamental to have a good evaporation process. In fact we must remove from the chamber either water vapour or hydrogen and helium residuals as well as the other materials ones. Moreover we have to verify that the particles medium free path *l* is by far greater than chamber dimension *L*. With these conditions the metal atom, during his flight through the vacuum, doesn't hit other atoms, so it doesn't deflect his trajectory, so it will fly straight (light rays theory).

The expression of the evaporating particles medium free path *l* is given by:

$$l = \frac{kT}{\sqrt{2}p\pi d^2}$$

where *k* is the Boltzmann constant, *T* the absolute vapour temperature, *p* the chamber pressure and *d* the medium particles diameter.

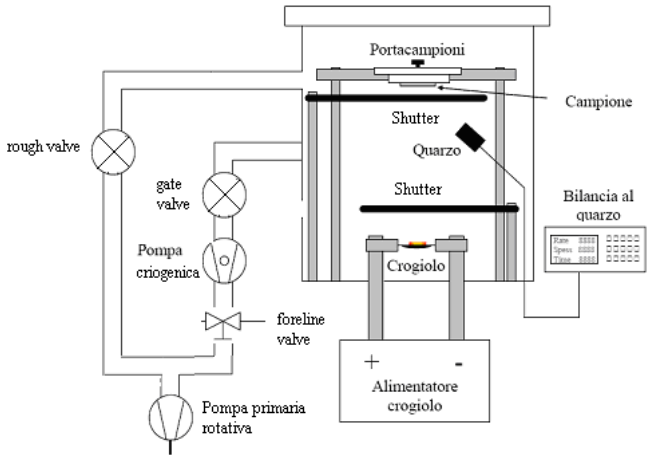


Figure 7.5 – Thermal evaporator draft.

On the bottom of chamber the crucible (melting pot) is situated, in which we put the material to evaporate. Crucible will be made by different materials and shapes depending on depositing substance, because it must neither react with it nor evaporate itself.

Material evaporation is realized by heating the crucible for Joule effect, it means we let flow a current in it. On the top of chamber an aluminium support is situated and the samples are fixed over it with appropriate clamps. The growth rate and the deposited film thickness are controlled by an electronic balance. Inside the balance there is a piezoelectric crystal that varies his resonance frequency with deposited material type and quantity: an appropriate electronic system, using these inputs and other data (material density, Z-ratio) obtains material thickness and growth rate values. For our process we have used a deposition rate of 3 nm/s.

Under the sample holder a shutter is situated to avoid contaminations of other materials. The shutter is opened when we are sure that the evaporation process is started, because before this moment other materials over the crucible could evaporate.

In Figure 7.6 (a) used thermal evaporator is shown.

(a)

(b)

(c)

Figure 7.6 – (a) Thermal evaporator used to evaporate ohmic contacts (b) Samples attacked on the holder (c) Evaporation phase.

7.4 E-beam evaporator (Al)

To manufacture MESFETs gates we have used an *e-beam evaporator*. It's structure is quite similar to the thermal evaporator, but the main difference is the way to obtain material evaporation.

Disadvantages of material evaporation using heated crucibles are the possible contaminations from crucible and the low power heating that makes very hard the evaporation of materials with high fusion point. The use of e-beam evaporation deletes these limits.

The operation principle is based on a hot tungsten filament that generates electrons for thermoionic effect; these electrons are accelerated by an electric field and then focalized on the metal to evaporate using magnets, so the Lorentz force.

Modulating the field or the current we raster the metal surface with the electron beam. These energetic electrons heat the material up to evaporate it: the advantage of this technique is that, in every moment, the beam hit only a small point of surface, avoiding an useless loss of energy.

In order to eliminate shadow effects and ensure an uniform covering, the substrate is put in rotation during evaporation.

In Figure 7.7 we show the e-beam evaporator used during this thesis while in Figure 7.8 its working is shown.

Figure 7.7 – E-beam evaporator used to manufacture Al gate contacts.

Before starting process we need to reach a pressure of about $1*10^{-7} \div 8*10^{-8}$ mbar: this value is reached after 3 hours from pumps activation.

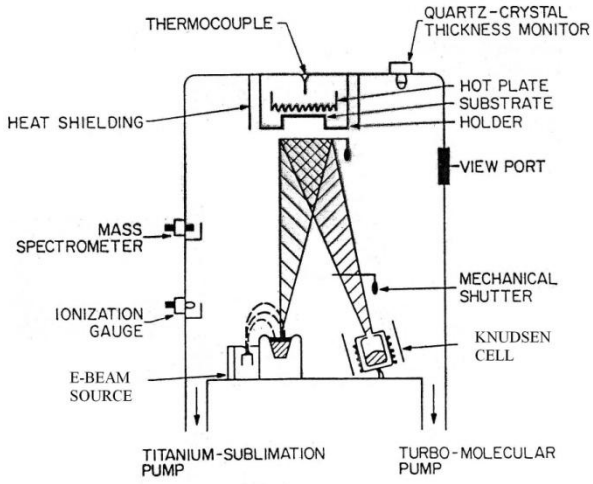


Figure 7.8 – E-beam evaporator working draft.

7.5 RIE (Reactive Ion Etching)

Plasma is the fourth matter state where this one occurs constituted by gas mixed to ions and electrons, those are very reactive with other gasses or solids.

Inside the plasma there is a high density of metastable and chemically active species that cause oxidation and/or reduction of other species in contact with them. When these reactions take place on solid materials, and the produced species are volatile so that they can be removed from the surface, we speak of RIE (*Reactive Ion Etching*). In order to the etching takes place selectively according to defined patterns, lithographic processes with optical masks are used. In our process, we have used this step to remove the conductive channel on the hydrogenated diamond. In Figure 7.9 is schematized the structure of this machine and the RIE system used for this thesis is shown in Figure 7.10.

The reaction chamber can contain substrates up to 4 inches and allows to execute processes with CF_4, O_2 e Ar. Process gas are controlled by a flow mass meter and the vacuum is obtained by a turbo-molecular pump.

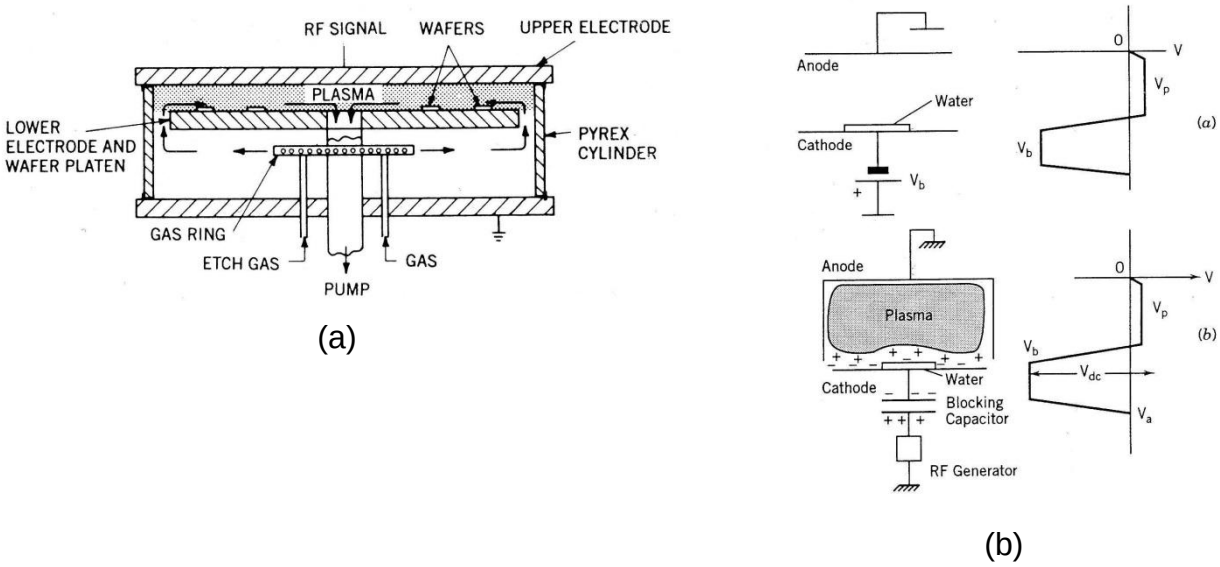
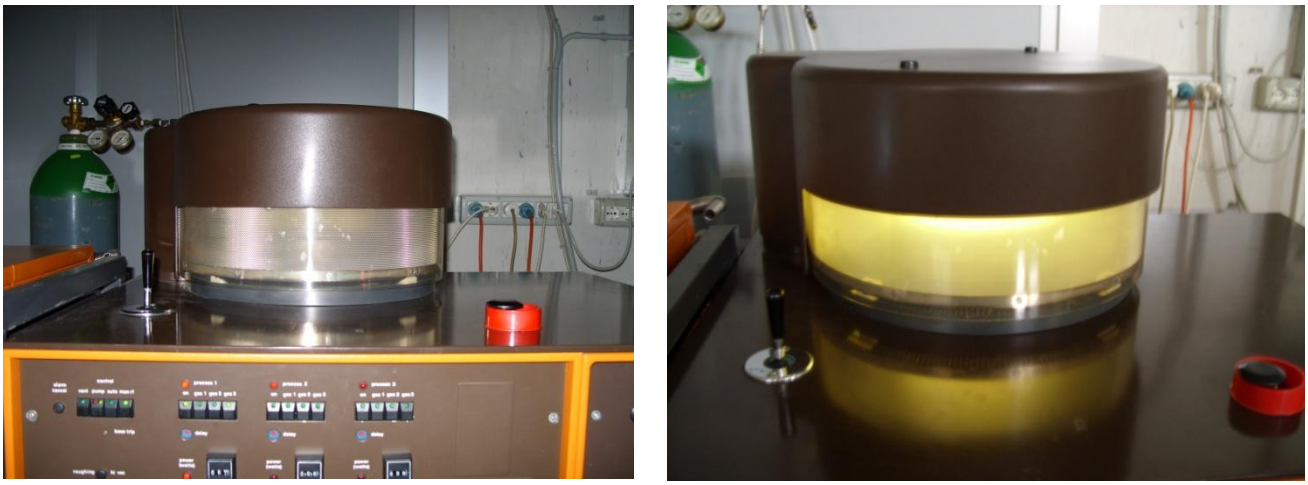


Figure 7.9 – (a) Working draft and (b) potential distribution in a RIE system.

The working principle is easy: an RF generator (at 13.56 MHz) polarizes the gas in the RIE chamber, that in our case are O_2 e Ar_2 - ratio 5:1. Emitted electrons from cathode excite gas atoms, those ionize. So these ions are accelerated by electric field and they hit the substrate, that is over the anode, with an energy proportional to the applied electric field intensity. The Ar bombardment generates the surface hydrogen loss, that is replaced by oxygen (attend in big quantity in the chamber). Naturally, only the free diamond surface (without gold and photoresist) is reached by Ar ions.



(a) (b)

Figure 7.10 – RIE system used in Roma Tre labs to remove conductive channel on hydrogenated diamond.

Generally a RIE system has a peak to peak RF potential from 1 to 3 kV and a pressure from 10 to 100 mTorr; the excitation is commonly obtained to 13.56 MHz. The symmetrical nature of applied voltage brings to an equal voltage drop over each plate of plasma. Anyway the system can be made asymmetric varying the relative dimension of electrodes.

7.6 EBL (Electron Beam Lithography)

Electron Beam Lithography (EBL) it's a lithographic process that uses a focused beam of electrons to form the desired patterns on the substrate, in contrast with optical lithography which uses light for the same purpose. Electron lithography offers higher patterning resolution than optical lithography because of the shorter wavelength possessed by the 10-50 keV electrons that it employs.

An EBL system doesn't need physic masks to perform its task (unlike optical lithography, which uses photomasks to project the patterns): in fact it simply 'draws' the pattern previously designed by software over the resist wafer using the electron beam as its drawing pen.

A typical EBL system consists of the following parts: an electron gun or electron source that supplies the electrons; an electron column that 'shapes' and focuses the electron beam; a mechanical stage that positions the wafer under the electron beam; a wafer handling system that automatically feeds wafers to the system and unloads them after processing; and a computer system that controls the equipment (see Figure 7.11).

The resolution of optical lithography is limited by diffraction, while an electron lithography system may be constrained by other factors, such as electron scattering in the resist and by various aberrations in its electron optics.

When electrons strike a material, they penetrate the material and lose energy from atomic collisions. These collisions can cause the striking electrons to 'scatter', a phenomenon that is aptly known as 'scattering'. The scattering of electrons may be backward (or back-scattering, wherein electrons 'bounce' back), but it is often forward through small angles with respect to the original path.

During electron beam lithography, scattering occurs as the electron beam interacts with the resist and substrate atoms. This electron scattering has two major effects: 1) it broadens the diameter of the incident electron beam as it penetrates the resist and substrate; and 2) it gives the resist unintended extra doses of electron exposure as back-scattered electrons from the substrate bounce back to the resist.

Thus, scattering effects during e-beam lithography result in wider images than what can be ideally produced from the e-beam diameter, degrading the resolution of the EBL system. In fact, closely-spaced adjacent lines can 'add' electron exposure to each other, a phenomenon known as 'proximity effect.'

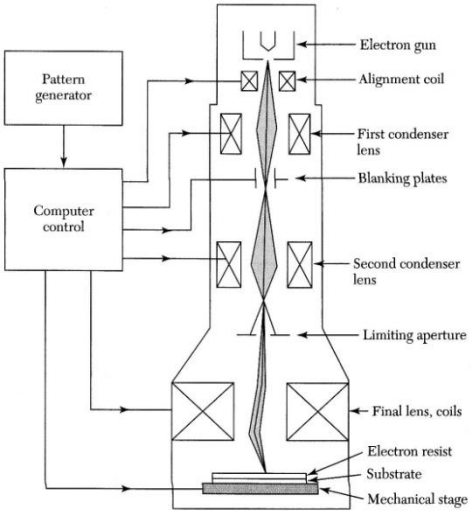
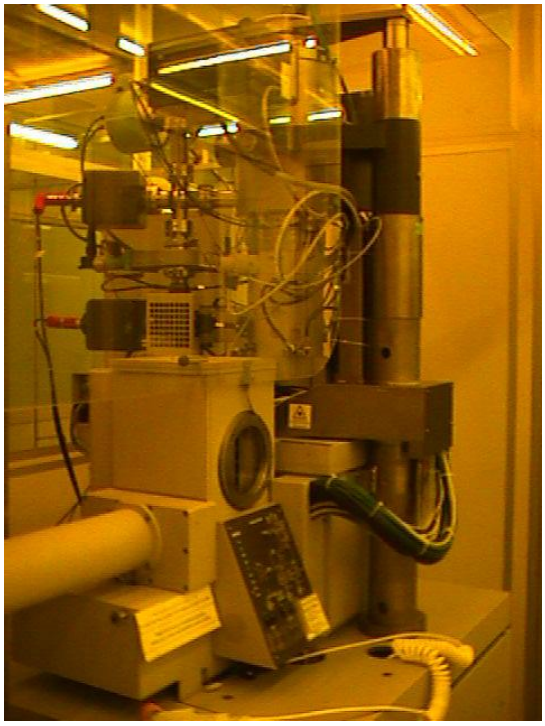


Figure 7.11 – EBL system draft.

In Figure 7.12 the CNR-IFN E.B.L. system used to construct either MESFETs gate contacts or optical masks is shown.



(a)

(b)

Figure 7.12 – (a) (b) CNR-IFN EBL system used to construct masks and MESFETs gate contacts.

7.7 Gold electroplating

Electroplating is a plating process in which metal ions in a solution are moved by an electric field to coat an electrode. The process uses electrical current to reduce cations of a desired material from a solution and coat a conductive object with a thin layer of the material, such as a metal. Electroplating is primarily used for depositing a layer of material to bestow a desired property to a surface that otherwise lacks that property or to build up thickness on undersized parts.

The process used in electroplating is called electrodeposition. It is analogous to a galvanic cell acting in reverse. The part to be plated is the cathode of the circuit. In one technique, the anode is made of the metal to be plated on the part. Both components are immersed in a solution called an electrolyte containing one or more dissolved metal salts as well as other ions that permit the flow of electricity. In our case, we use sodium dicyanoaurate $Na[Au(CN)_2]$. A power supply supplies a direct current to the anode, oxidizing the metal atoms that comprise it and allowing them to dissolve in the solution. At the cathode, the dissolved metal ions in the electrolyte solution are reduced at the interface between the solution and the cathode, such that they "plate out" onto the cathode (see Figure 7.13). The rate at which the anode is dissolved is equal to the rate at which the cathode is plated, as the current flowing through the circuit. In this manner, the ions in the electrolyte bath are continuously replenished by the anode. Other electroplating processes may use a non-consumable anode such as lead. In these techniques, ions of the metal to be plated must be periodically replenished in the bath as they are drawn out of the solution. In Figure 7.14 is shown gold electroplating system used by IFN-CNR labs of Rome.

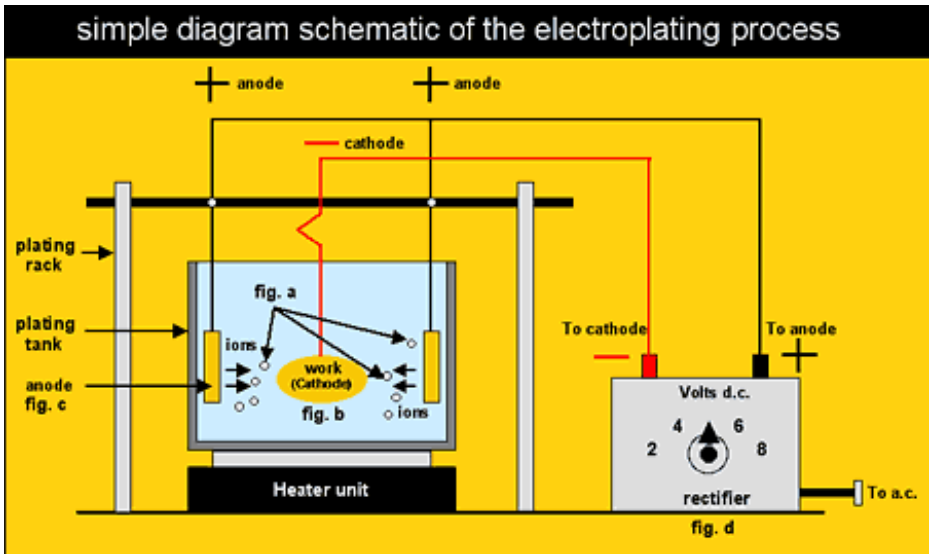
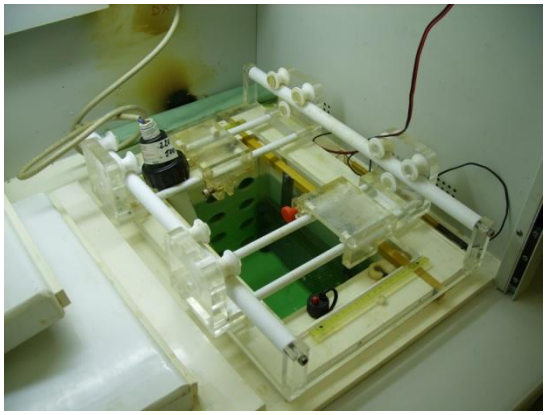
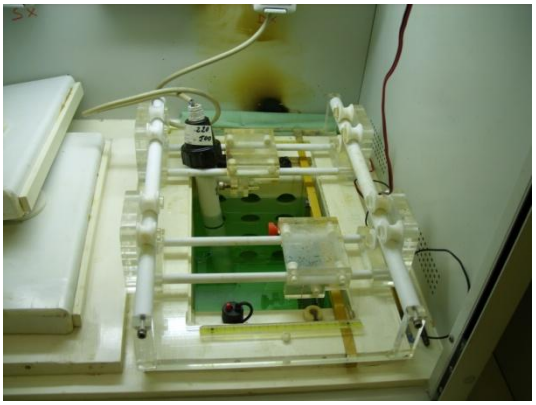


Figure 7.13 – Electroplating process diagram schematic.

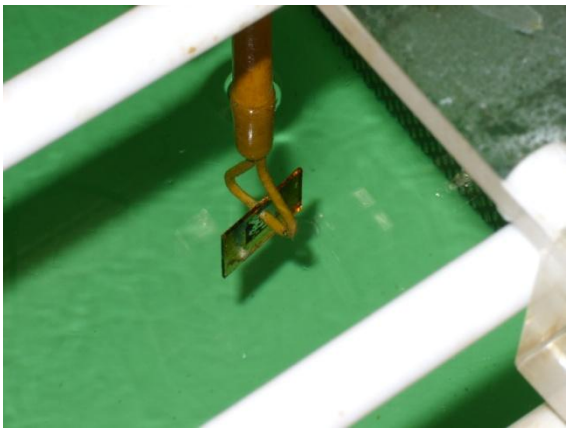
The current density (current of the electroplating current divided by the surface area of the part) in this process strongly influences the deposition rate, plating adherence, and plating quality. This density can vary over the surface of a part, as outside surfaces will tend to have a higher current density than inside surfaces (e.g., holes, bores, etc.). The higher the current density, the faster the deposition rate will be, although there is a practical limit enforced by poor adhesion and plating quality when the deposition rate is too high. Obtaining a uniform thickness with electroplating can be difficult depending on the geometry of the object being plated. The plating metal is preferentially attracted to external corners and protrusions, but unattracted to internal corners and recesses. These difficulties can be overcome with multiple anodes or a specially shaped anode that mimics the object geometry, however both of these solutions increase cost. The ability of a plating to cover uniformly is called *throwing power*; the better the "throwing power" the more uniform the coating.



(a)



(b)



(c)

Figure 7.14 – Gold electroplating system used in IFN - CNR labs to plate diamond substrate.

Chapter 8

Simulation results

8.1 Introduction

Recent advances in workstation computing power and user-friendly software make it possible to develop EM field simulators. These simulators play a significant role in the simulation of single and multilayer passive circuit elements such as transmission lines and their discontinuities, inductors, capacitors, resistors, via holes, airbridges, packages, and so on and passive coupling between various circuit elements. Accurate evaluation of the effects of radiation, surface waves and interaction between components on the performance of densely packed MMICs can only be calculated using *three-dimensional* (3-D) EM simulators.

Numerical methods, implemented in EM simulators, simulate devices adequately and also provide additional flexibility in terms of layout, complexity (i.e., 2-D or 3-D configuration) and versatility. EM simulations automatically incorporate junction discontinuities, airbridge or crossover effects, substrate effects (thickness and dielectric constant), strip thickness, and dispersion and higher order modes effects.

The most commonly used technique for planar structures is the method of moments (MoM), and for 3-D structures, the finite element method (FEM) is usually used. Both of these techniques perform EM analysis in the frequency domain. FEM can analyze more complex structures than can MoM, but requires much more memory and longer computation time. There are also several time-domain analysis techniques; among them are the transmission-line matrix method (TLM) and the finite-difference time-domain (FDTD) method. Fast Fourier transformation is used to convert time-domain data into frequency-domain results. Typically, a single time-domain analysis yields *S*-parameters over a wide frequency range. An overview of commercially available EM simulators is given in Table 8.1.

Table 2.2
An Overview of Some Electromagnetic Simulators Being Used for MMICs

Company	Software Name	Type of Structure	Method of Analysis	Domain of Analysis
Agilent	Momentum HFSS	3-D planar 3-D arbitrary	FEM	Frequency
Sonnet Software	Em	3-D planar	MoM	Frequency
Jansen Microwave	Unisim SFMIC	3-D planar 3-D planar	Spectral domain MoM	Frequency
Ansoft Corporation	Maxwell-Strata Maxwell SI Eminence	3-D planar 3-D arbitrary	MoM FEM	Frequency
MacNeal-Schwendler Corp.	MSC/EMAS	3-D arbitrary	FEM	Frequency
Zeland Software	IE3-D	3-D arbitrary	MoM	Frequency
Kimberly Communications Consultants	Micro-Stripes	3-D arbitrary	TLM	Time
Remco	XFDTD	3-D Arbitrary	FDTD	Time

Table 8.1 - An Overview of Some Electromagnetic Simulators Being Used for MMICs.

In EM simulators, Maxwell's equations are solved in terms of electric and magnetic fields or current densities, which are in the form of integrodifferential equations, by applying boundary conditions. Once the structure is analyzed and laid out, the input ports are excited by known sources (fields or currents), and the EM simulator solves numerically the integrodifferential equations to determine unknown fields or induced current densities. The numerical methods involve discretizing (meshing) the unknown fields or currents. Using FEMs, six field components (three electric and three magnetic) in an enclosed 3-D space are determined while MoMs give the current distribution on the surface of metallic structures.

All EM simulators are designed to solve arbitrarily shaped strip conductor structures and provide simulated data in the form of single or multiport *S*-parameters that can be read into a circuit simulator. To perform an EM simulation, the structure to be simulated is defined in terms of dielectric and metal layers and their thicknesses and material properties. After creating the complete circuit/structure, ports are defined and the layout file is saved as an input file for EM simulations. Then the EM simulation engine is used to perform an electromagnetic analysis. After the simulation is complete, the field or current information is converted into *S*-parameters and saved to be used with other CAD tools.

EM simulators, although widely used, still cannot handle complex structures such as an inductor efficiently due to its narrow conductor dimensions, large size, and 3-D geometry. One has to compromise among size, speed, and accuracy.

8.2 Sonnet software 11.54

Sonnet's suites of high-frequency electromagnetic (EM) Software are aimed at today's demanding design challenges involving predominantly planar (3D planar) circuits and antennas such as microstrip, stripline, coplanar waveguide, planar spiral inductors, RFIC & MMIC circuits, PCB (single and multiple layers) and combinations with vias, vertical metal sheets (z-directed strips), and any number of layers of metal traces embedded in stratified dielectric material.

The Sonnet Suites develop precise RF models (S-, Y-, Z-parameters or extracted SPICE model) for planar circuits and antennas. The software requires a physical description of your circuit (arbitrary layout and material properties for metal and dielectrics), and employs a rigorous Method-of-Moments EM analysis based on Maxwell's equations that includes all parasitic, cross-coupling, enclosure and package resonance effects.

The suite of Sonnet analysis tools is shown in Figure 8.2. Using these tools, Sonnet provides an open environment to many other design and layout programs.

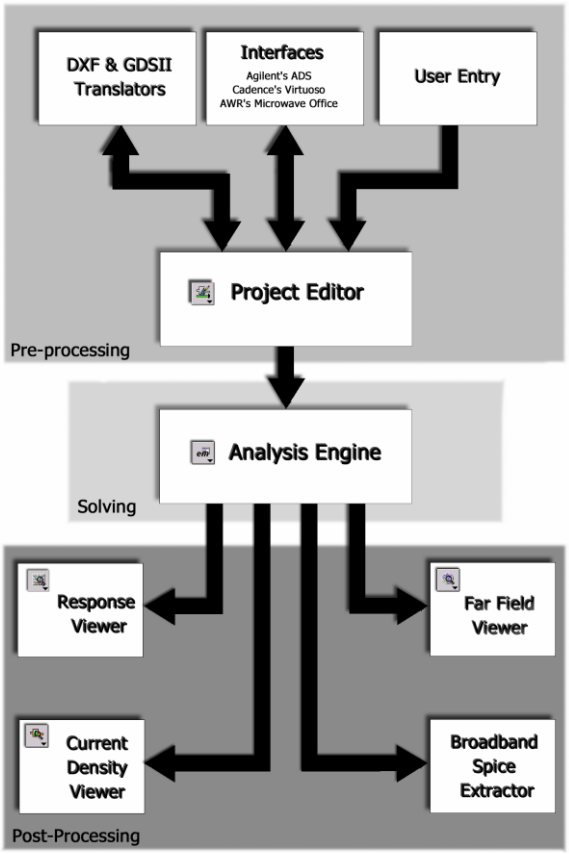


Figure 8.2 - The suite of Sonnet analysis tools: using these tools, Sonnet provides an open environment to many other design and layout programs.

There are two types of projects in Sonnet: the Geometry Project and the Netlist Project: we have used the first one. A geometry project contains a circuit whose properties are entered by the user or provided by translating a file to the Sonnet environment. The geometry project contains the layout and material properties of a circuit and any internal components. When you analyze a geometry project, ***em*** performs an electromagnetic simulation of your circuit. For both types of projects, the analysis controls (such as analysis frequencies, run options, etc.) and analysis data are stored in the project. In addition to viewing your response within Sonnet, you may also export data files for use in other tools.

The Sonnet EM analysis is performed inside a six-sided metal box as shown in Figure 8.3. This box contains any number of dielectric layers which are parallel to the bottom of the box. Metal polygons may be placed on levels between any or all of the dielectric layers, and vias may be used to connect the metal polygons on one level to another.

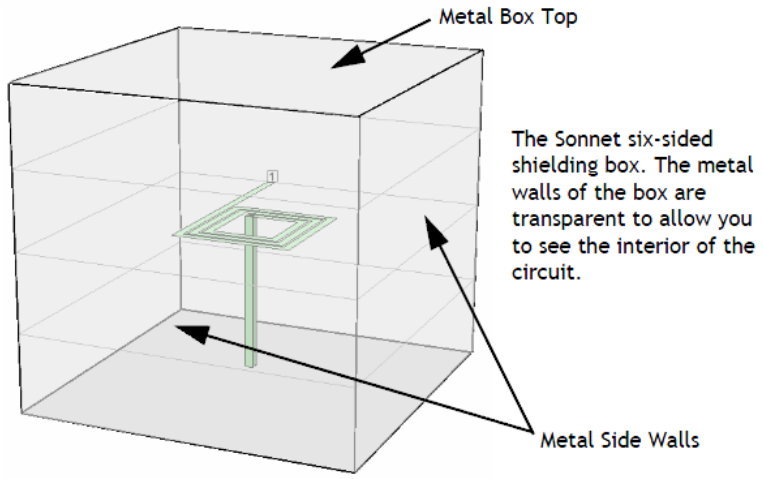


Figure 8.3 - The suite of Sonnet analysis tools: using these tools, Sonnet provides an open environment to many other design and layout programs.

The four sidewalls of the box are lossless metal, which provide several benefits for accurate and efficient high frequency EM analysis:

• The box walls provide a perfect ground reference for the ports and Sonnet's sidewall ground references make it possible for us to provide S-parameter dynamic range that routinely exceeds 100 dB.

• Because of the underlying EM analysis technique, the box walls and the uniform grid allow us to use fast-Fourier transforms (FFTs) to compute all circuit cross-coupling. FFTs are fast, numerically robust, and map very efficiently to computer processing.

• There are many circuits that are placed inside of housings, and the box walls give us a natural way to consider enclosure effects on circuit behavior.

As an example, a microstrip circuit can be modeled in Sonnet by creating two dielectric layers: one which represents your substrate, and one for the air above the substrate. The metal polygons for the microstrip would be placed on the metal level between these two dielectric layers. The bottom of the box is used as the ground plane for the microstrip circuit. The top and bottom of the box may have any loss, allowing you to model ground plane loss.

Since the four sidewalls of the box are lossless metal, any circuit metal which is close to these walls can couple to the walls - just like what would happen if you fabricated and measured a real circuit with the same box. If you do not want to model this coupling (for example, your real circuit does not have sidewalls), then you must keep the circuit metal far away from the box sidewalls. A good rule to use is at least three to five substrate thicknesses as shown below.

All Sonnet geometry projects are composed of two or more dielectric layers. There is no limit to the number of dielectric layers in a Sonnet geometry project, but each layer must be composed of a single dielectric material. Metal polygons are placed at the interface between any two dielectric layers and are usually modeled as zero-thickness, but can also be modeled using Sonnet's thick metal model. Vias may also be used to connect metal polygons on one level to metal on another level.

The total height of the box is determined by the sum of the thicknesses of the dielectric layers since metal is either modeled as zero-thickness or protrudes into the dielectric layer above [15].

8.3 Diamond inductors results

In general numerous papers have been published in the literature describing lumped inductor models over Silicon and GaAs substrates. Models be developed using analytical, physics and EM, and measurement-based methods. The analytical/semiempirical models are based on three approaches: the lumped-element method, the microstrip coupled-line method, and the mutual inductance method [16-17]. The lumped-element approach uses frequency-independent formulas for free-space inductance with ground plane effects. These formulas are useful only when the total length of the inductor is a small fraction of the operating wavelength and when the inter-turn capacitance can be ignored. In the coupled-line approach, an inductor is analyzed using multi-conductor coupled microstrip lines. This

technique predicts the spiral inductor's performance reasonably well for up to two turns and frequencies up to 18 GHz. For more than three turns, we need to analyze three or more parallel coupled lines. The analytical semi-empirical models are good for approximating the electrical performance of inductors. Accurate characterization of inductors including the effects of radiation, surface waves, and interaction between components on the performance of densely packed inductors in MMICs can only be calculated using 3-D EM simulators.

In the following paragraph we discuss only about the lumped-element method.

8.3.1 Analytical Models

Lumped-element EC models of printed inductors are shown in Figure 8.4. Approximate expressions for inductance L, resistance R_S, and parasitic capacitances for microstrip sections, circular loops, and circular coils are given next [18].

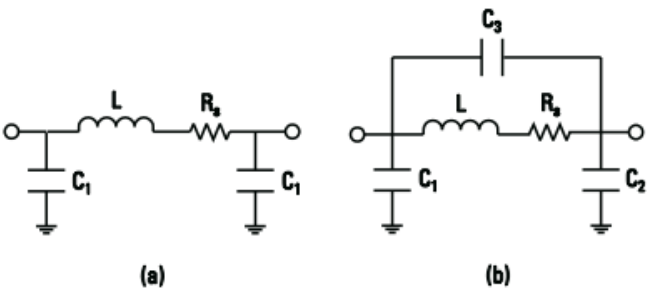


Figure 8.4 - EC models: (a) microstrip section and loop and (b) coil.

Circular and arbitrary shape spiral

$$L(nH) = 0.03937 \frac{a^2 n^2}{8a + 11c} \cdot K_g \qquad (8.1)$$

$$a = \frac{D_0 + D_i}{4}, c = \frac{D_0 - D_i}{2}, R_S(\Omega) = \frac{K \pi a n R_{sh}}{W} \qquad (8.2)$$

$$C_3(pF) = 3.5 \times 10^{-5} D_0 + 0.06 \qquad (8.3)$$

where all dimensions are in microns and

$$K_g = 0.57 - 0.145 \ln \frac{W}{h}, \frac{W}{h} > 0.05 \qquad (8.4)$$

$$K = 1 + 0.333\left(1 + \frac{S}{W}\right) \quad \text{for a spiral} \qquad (8.5)$$

The term K_g accounts for the presence of a ground plane and decreases as the ground plane is brought nearer. Another term K is a correction factor that takes into account the crowding of the current at the corners of the conductor. The terms W, t, h, a and R_{sh} are the line width, line thickness, substrate thickness, mean radius of the loop, and sheet resistance per square of the conductor, respectively. Moreover n is the number of turns, D_i is the inductor's inside diameter, D_o is the inductor's outside diameter, and S is the spacing between the turns. The effect of ground plane on the inductance value can be reduced by keeping $S < W$ and $S << h$.

A more general expression for inductance of arbitrary shape has been reported in the literature [19, 20] and reproduced as follows:

$$L = \frac{\mu_0 n^2 D_{av} c_1}{2}\left[\ln\left(c_2 / \rho\right) + c_3\rho + c_4\rho^2\right] \qquad (8.6)$$

where coefficients c_i for various geometries are given in Table 8.2, ρ is the fill ratio, and D_{av} is the average diameter of the inductor. Their expressions are given here:

$$\rho = \frac{D_0 - Di}{D_0 + Di} \qquad (8.7)$$

$$D_{av} = \frac{1}{2}\left(D_0 + Di\right) \qquad (8.8)$$

Inductor Geometry	c_1	c_2	c_3	c_4
Square	1.27	2.07	0.18	0.13
Hexagonal	1.09	2.23	0.00	0.17
Octagonal	1.07	2.29	0.00	0.19
Circle	1.00	2.46	0.00	0.20

Table 8.2 - Coefficients for General Inductance Expression [19].

Because these formulas are useful only when the total length of the inductor is a small fraction of the operating wavelength, as in our case, using the equations (8.6) - (8.8) we can quickly simulate the expected value of diamond inductances applying the following fixed parameters (Table 8.3):

- Conductor width W : 20 µm;
- Spacing between turns S : 20 µm;
- Inner diameter D_i : 100 µm;

The other parameters D_{av}, D_o, ρ are a function of number of turns n.

Number of turns	5.5	4.5	3.5	2.5	1.5
Inductance [nH]	9.94	6.05	3.32	1.54	0.51

Table 8.3 – Diamond inductance estimated value for different number of turns.

This has been only the first approach used to determine a quantitative analysis of our devices. The following step has been the use of *SONNET* EM simulator to have a qualitative analysis of their behavior with frequency.

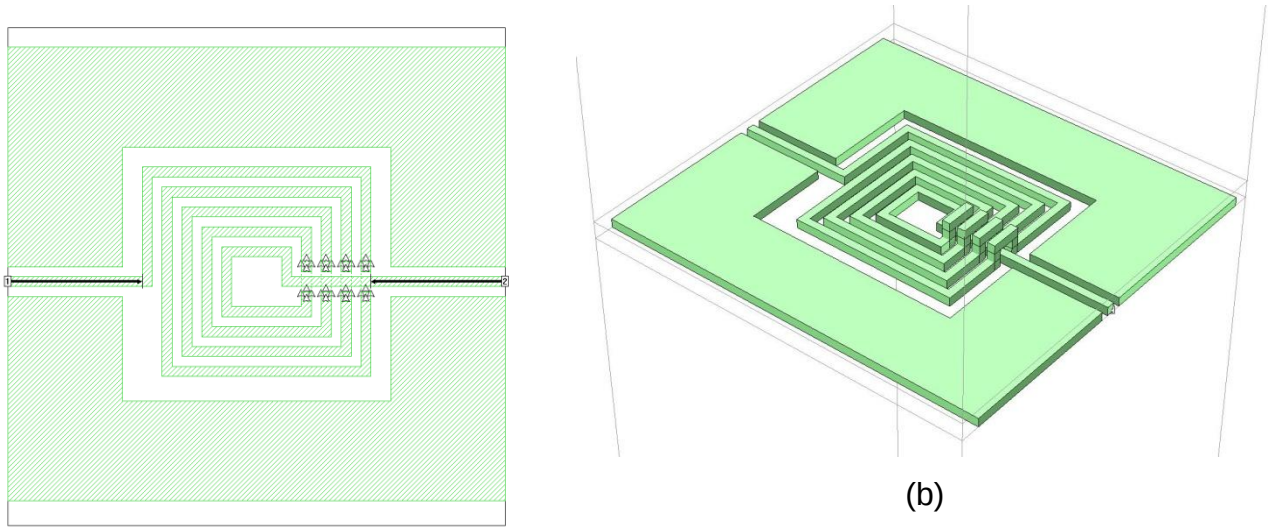
8.3.2 EM simulations

Before showing the results of inductors simulations, we need to show the input parameters used to analyze our devices. In fact either geometry layout or these parameters influence simulation results.

As far as layout concern, it is shown in Figures 8.5 (top and 3D view). In these pictures we can see a squared inductor with 5.5 turns. Design parameters are shown in Table 8.4.

Number of turns	*W [µm]*	*S [µm]*	*D_i [µm]*
From 1.5 up to 5.5	20.0	20.0	100.0

Table 8.4 – Geometric parameters used for diamond electromagnetic simulations.



(a) (b)

Figure 8.5 – (a) Top and (b) 3D view of inductor as designed with SONNET software.

Writing about simulation parameters, we have insert inputs listed in table 8.5. Conductor metal was used with losses.

Substrate thickness [µm]	*Diamond ε_{rel}*	*Conductor material*	*Bridge height h [µm]*	*Metal conductivity [S/m]*	*Metal thickness [µm]*
500	**5.7**	**Gold**	**2.0**	**$40.9*10^6$**	**1.0**

Table 8.5 – Sonnet input parameters used for diamond electromagnetic simulations.

In figure 8.6 the variation of inductance value *L* with frequency *f*, for different numbers of turns, is shown. As supposed, increasing the number of turns we obtain a higher value of inductance *L* because we are increasing the magnetic flux. Data are shown up to the first resonance.

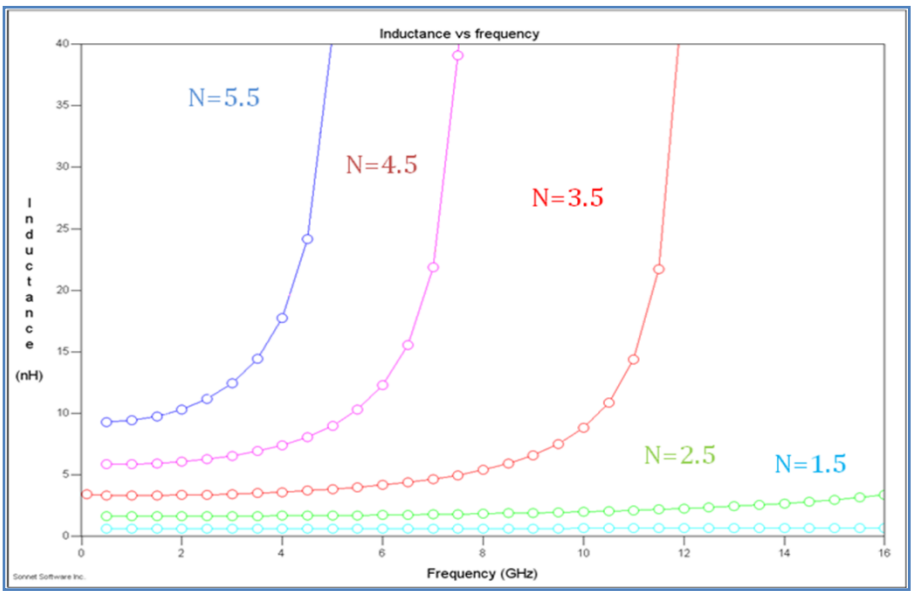


Figure 8.6 - Inductance L with frequency changing the number of turns n.

In table 8.8 there is a comparison between data of Table 8.3 obtained with formula 8.6 and data obtained with EM simulator. As we can see, results are very similar.

Number of turns	**5.5**	**4.5**	**3.5**	**2.5**	**1.5**
Inductance [nH] **with formula 8.6**	**9.94**	**6.05**	**3.32**	**1.54**	**0.51**
with EM simulator (@0.5 GHz)	**9.32**	**5.86**	**3.36**	**1.67**	**0.65**

Table 8.8 – Comparison between data obtained with formula 8.6 and data obtained with EM simulator

In figure 8.7 the variation of *Q*-factor with frequency *f*, for different numbers of turns, is shown. *Q* peak value decreases with the increase in number of turns because of increased RF resistance due to eddy currents and the increase of parasitic capacitance.

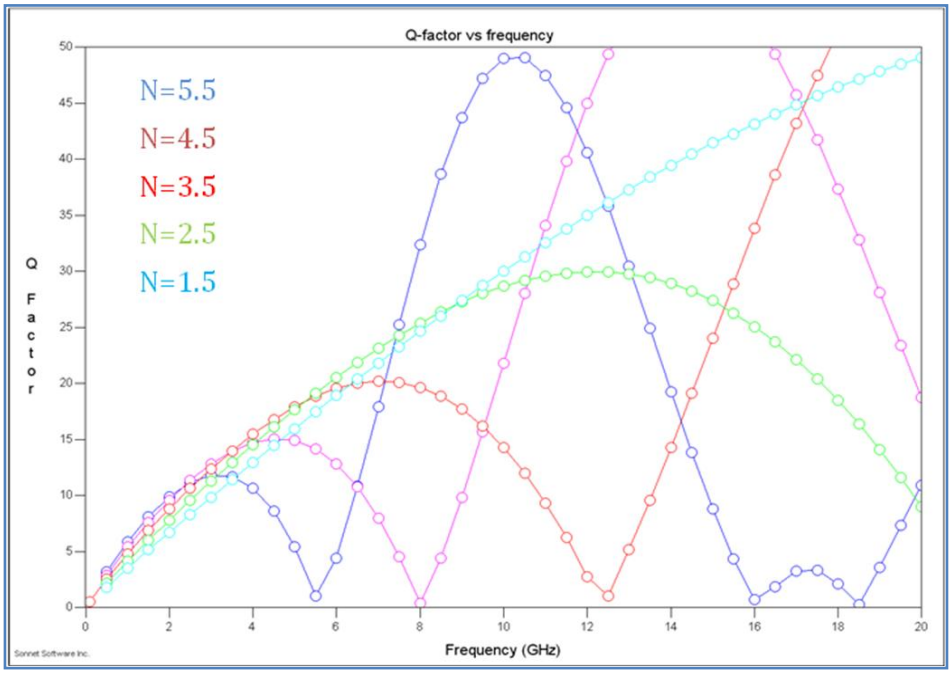


Figure 8.7 – Q-factor with frequency changing the number of turns n.

In Figure 8.8 the inductance value *L* with frequency *f*, for different numbers of inner diameter D_i and fixed *n*=3.5 is shown. As expected, the inductance increases with increasing inner diameter (D_i) due to increased inductor area.

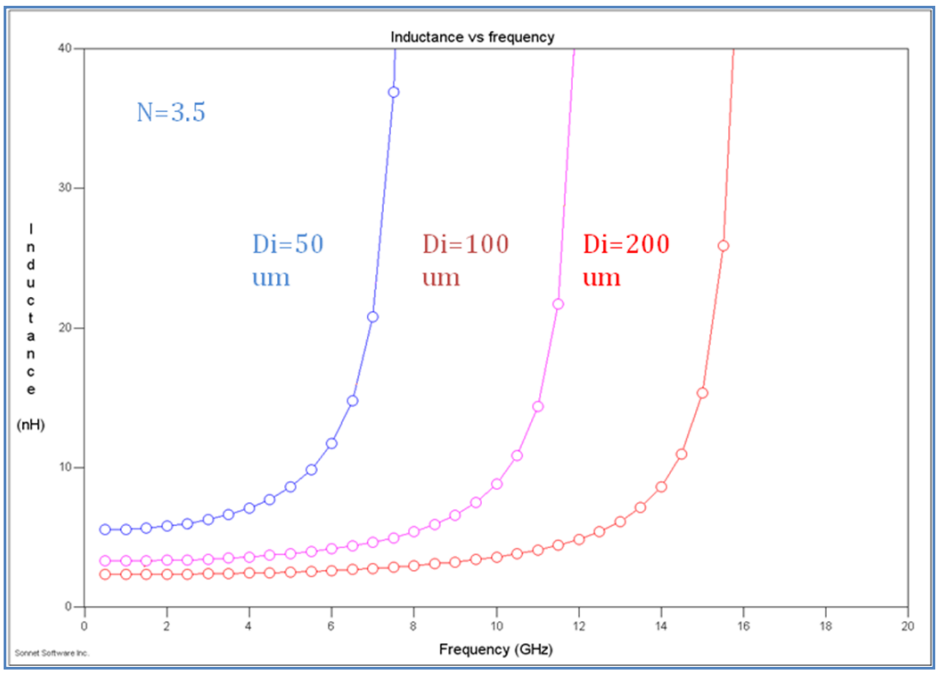


Figure 8.8 - Inductance value L with frequency f, for fixed n= 3.5 and different numbers of inner diameter D_i (50 um, 100 um and 200 um).

In Figure 8.9 and 8.10 inductance and Q-factor values with frequency for a 3.5-turns Silicon, Gallium arsenide and diamond inductors are illustrated. Increasing frequency, we have an higher value for both L and Q parameters in the diamond inductors.

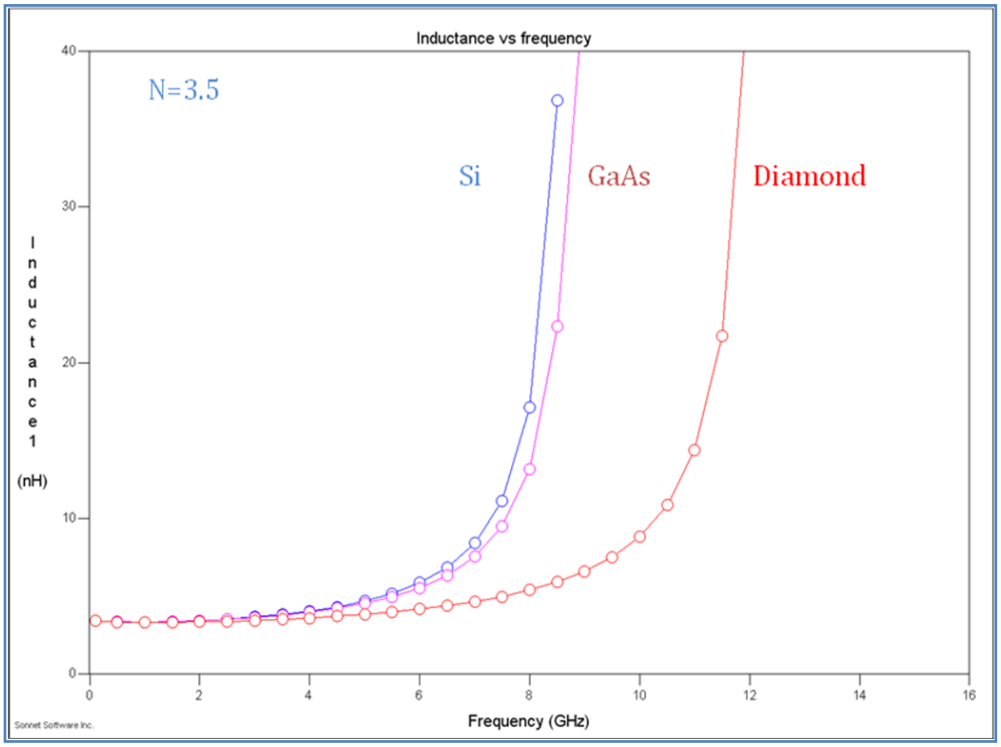


Figure 8.9 – Comparison between GaAs, Silicon and Diamond Inductance of 3.5-turns Inductors.

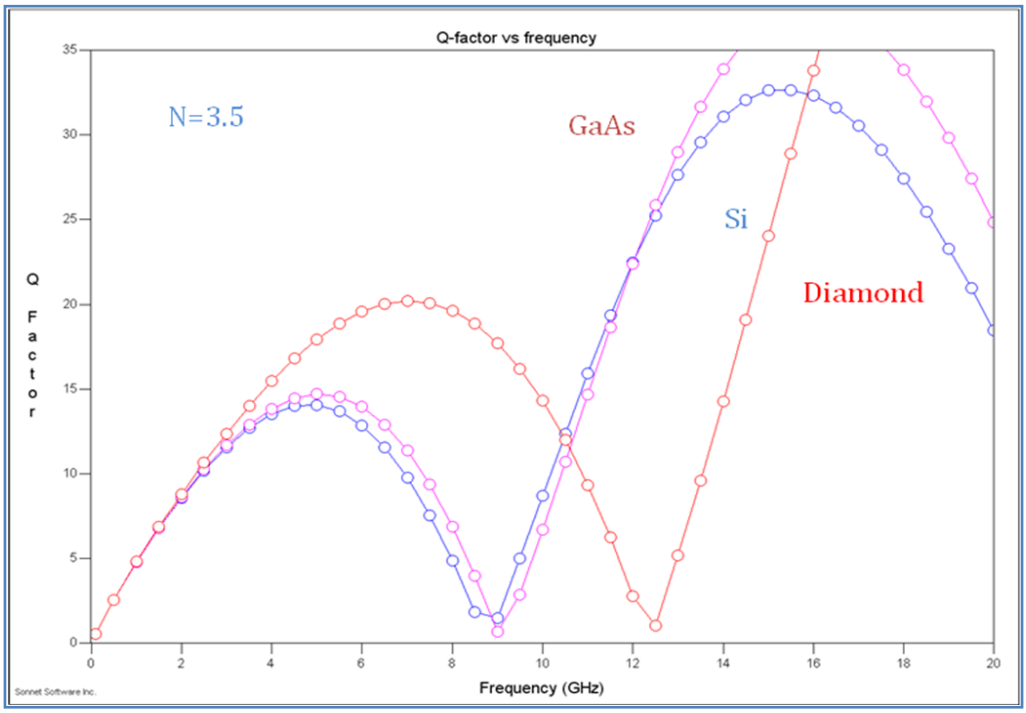
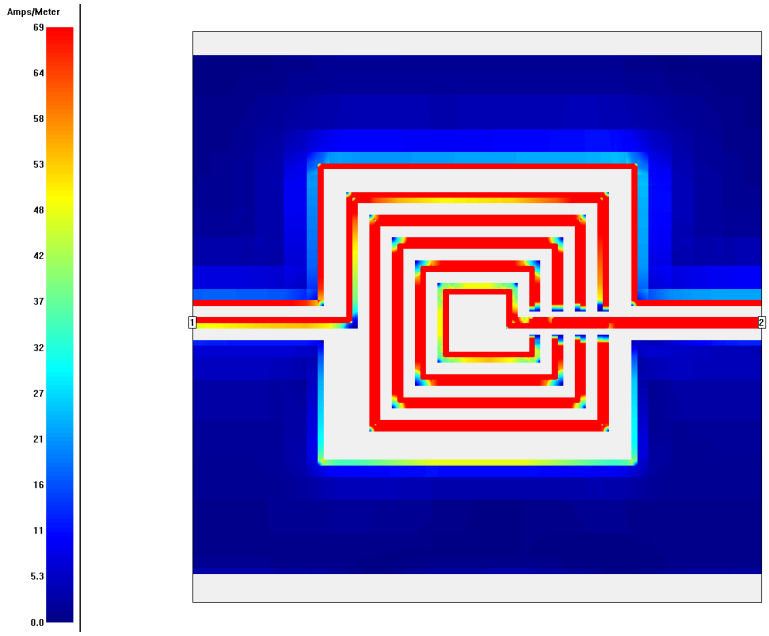
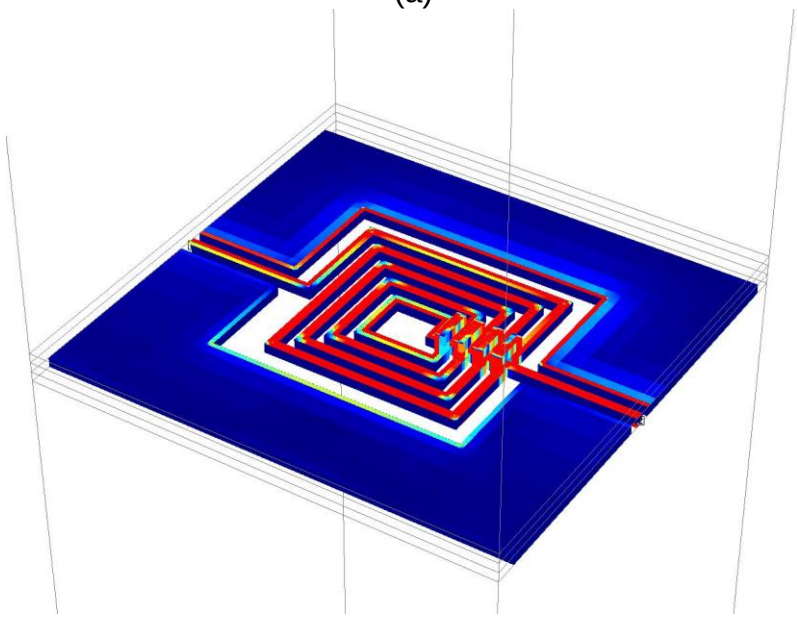


Figure 8.10 - Comparison between GaAs, Silicon and Diamond Q-factor of 3.5-turns Inductors.

In Figure 8.11 the current flow in a 4-turns inductor @ 5 GHz is shown.



(a)



(b)

Figure 8.11 – Current flow in a 4-turns inductor @ 5 GHz

8.4 Diamond capacitors results

Several models for MIM capacitors on GaAs substrate have been described in the literature [21], that include both EC and distributed models. We try to apply the simple MIM circuit model as previously described in paragraph 3.3.

When the largest dimension of the MMIC capacitor is less than $\lambda/10$, in the dielectric film at the operating frequency, the capacitor value can be approximated by the following relation:

$$C = \varepsilon_0 \varepsilon_{rd} \frac{Wl}{d} = \frac{\varepsilon_{rd} 10^{-15}}{36\pi} \frac{Wl}{d} \text{ (F)} \qquad (8.9)$$

where ε_{rd} is the dielectric constant of the dielectric film, *W* is the width of plate, *l* is the length of plate and *d* is the film thickness.

Because these formulas are useful only when the condition previously written is true, as in our case, using the equations (8.9) we can quickly simulate the expected value of diamond capacitors applying the following fixed parameters (Table 8.9):

- Conductor area *Wxl* : 200x200 µm^2, 150x150 µm^2, 100x100 µm^2, 50x50 µm^2;
- Dielectric film thickness : 2.0 µm (PMMA), 0.2 µm (Si_3N_4);
- Dielectric constant ε_{rd} : 2.6 µm (PMMA), 6.8 (Si_3N_4);

Capacitor Area	200x200 µm^2		150x150 µm^2		100x100 µm^2		50x50 µm^2	
Dielectric constant ε_{rd}	**2.6**	**6.8**	**2.6**	**6.8**	**2.6**	**6.8**	**2.6**	**6.8**
Thickness d [µm]	**2.0**	**0.2**	**2.0**	**0.2**	**2.0**	**0.2**	**2.0**	**0.2**
Capacitance [pF]	**0.46**	**12**	**0.26**	**6.77**	**0.11**	**3.0**	**0.03**	**0.75**

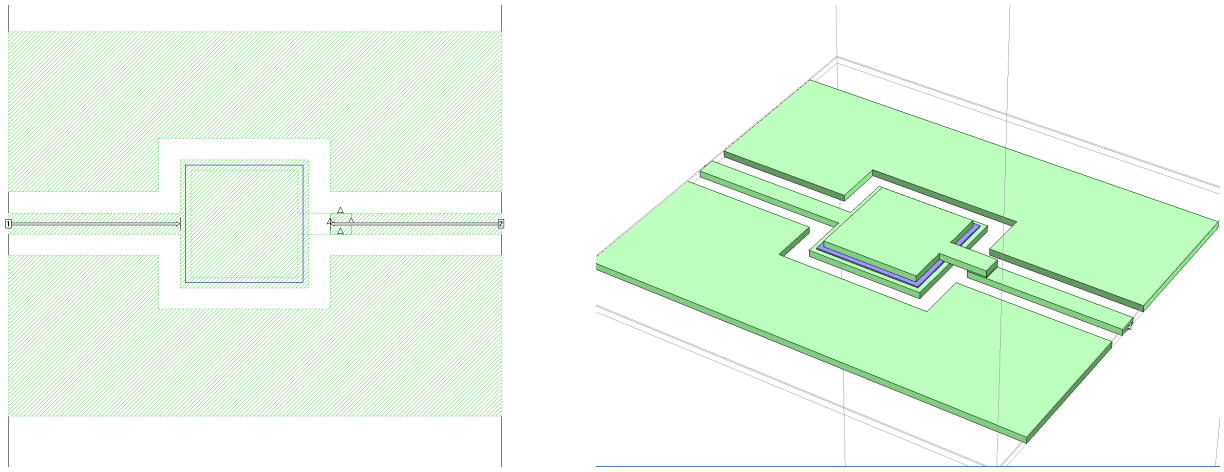
Table 8.9 – Diamond capacitance estimated value for different layout and material parameters.

This has been only the first approach used to determine a quantitative analysis of our devices. The following step has been the use of *SONNET* EM simulator to have a qualitative analysis of their behavior with frequency.

8.4.1 EM simulations

Before showing the results of capacitors simulations, we need to show the input parameters used to analyze our devices. In fact either geometry layout or these parameters influence simulation results.

As far as layout concern, it is shown in Figures 8.12 (top and 3D view). In these pictures we can see a squared capacitor with A=100 µm^2. Design parameters are the same shown in Table 8.9.



(a) (b)

Figure 8.12 - (a) Top and (b) 3D view of capacitor as designed with SONNET software.

Writing about simulation parameters, we have insert inputs listed in the previous table 8.5. Again, conductor metal was used with losses.

In figure 8.13 the variation of inductance value *C* with frequency *f*, for different areas, is shown. As supposed, increasing the number plates area we obtain a higher value of capacitance *C* because we are increasing the product *W*x*L*.

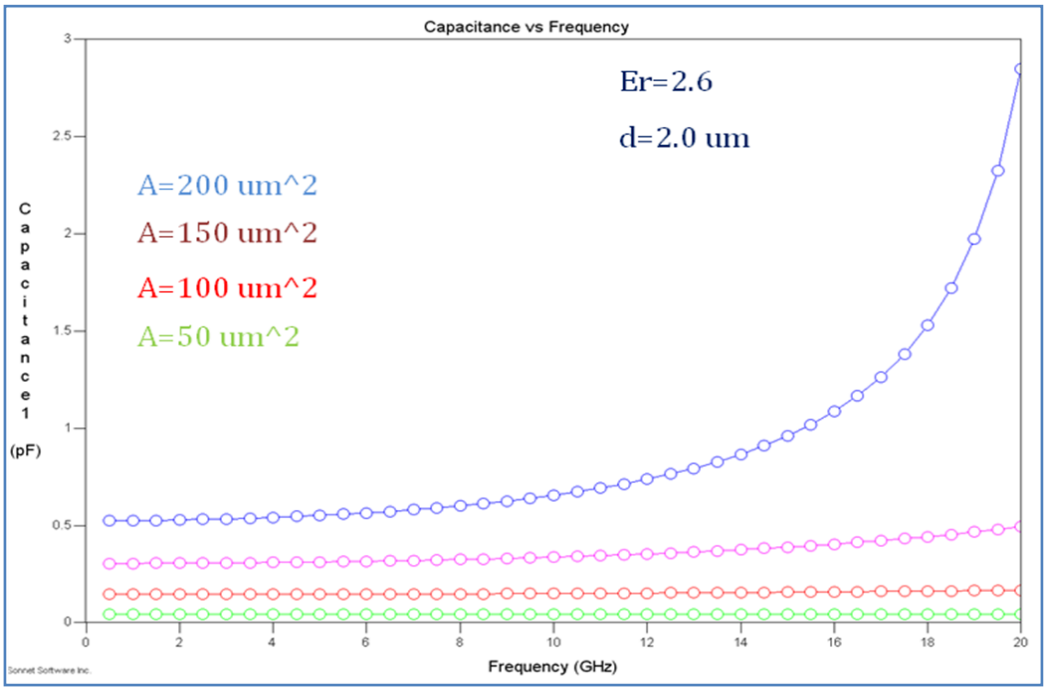


Figure 8.13 - Capacitance C with frequency changing capacitors area.

In table 8.10 there is a comparison between data of Table 8.9 obtained with formula 8.9 and data obtained with EM simulator. As we can see, results are very similar.

Capacitor Area	200x200 μm^2		150x150 μm^2		100x100 μm^2		50x50 μm^2	
Dielectric constant ε_{rd}	**2.6**	**6.8**	**2.6**	**6.8**	**2.6**	**6.8**	**2.6**	**6.8**
Thickness d [μm]	**2.0**	**0.2**	**2.0**	**0.2**	**2.0**	**0.2**	**2.0**	**0.2**
Capacitance [pF] with formula 8.9	**0.46**	**12**	**0.26**	**6.77**	**0.11**	**3.0**	**0.03**	**0.75**
with EM simulator (@0.5 GHz)	**0.52**	**-**	**0.3**	**-**	**0.14**	**3.0**	**0.04**	**0.8**

Table 8.10 – Comparison between data obtained with formula 8.9 and data obtained with EM simulator

In figure 8.14 the variation of *Q*-factor with frequency *f*, for different areas, is shown. Because *Q*-factor is in inverse proportion to capacitance value and *f*, fixing frequency bigger is capacitor area and smaller is *Q*-factor while, fixing area, with increasing of *f* we have a decreasing of *Q*.

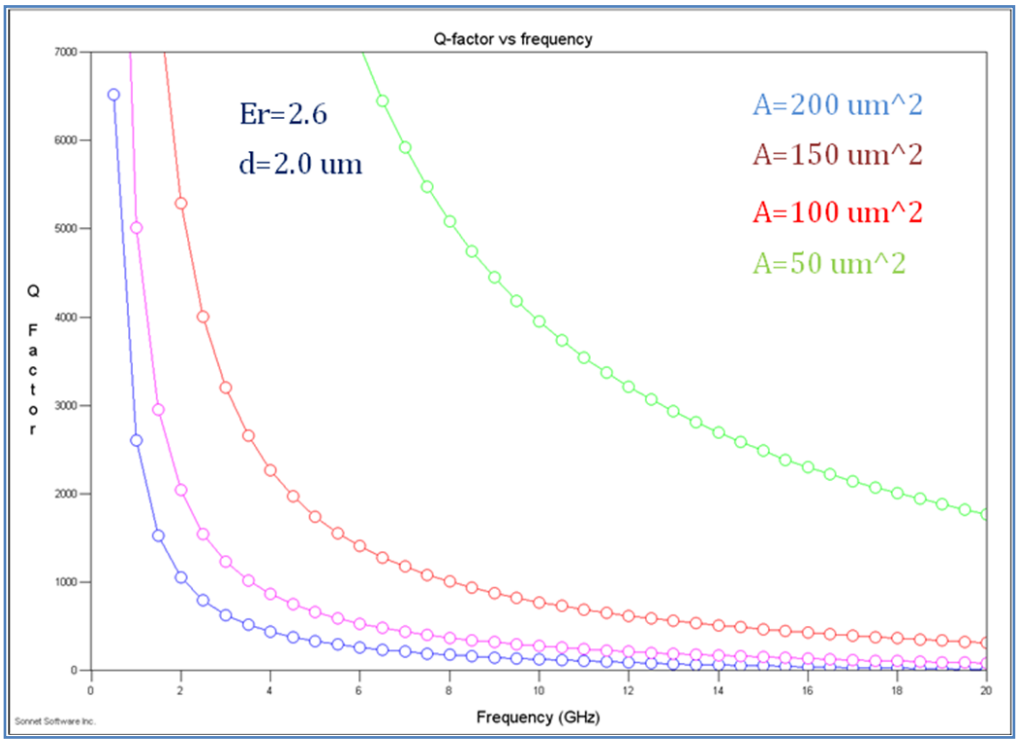


Figure 8.14 - Q-factor with frequency changing capacitors area.

In figure 8.15 and 8.16 we've illustrated the trend with frequency of *C* and *Q*-factor for capacitors with different aspect ratio *W/L*. As explained in paragraph 3.4, changing the aspect ratio is used to increase Q-factor.

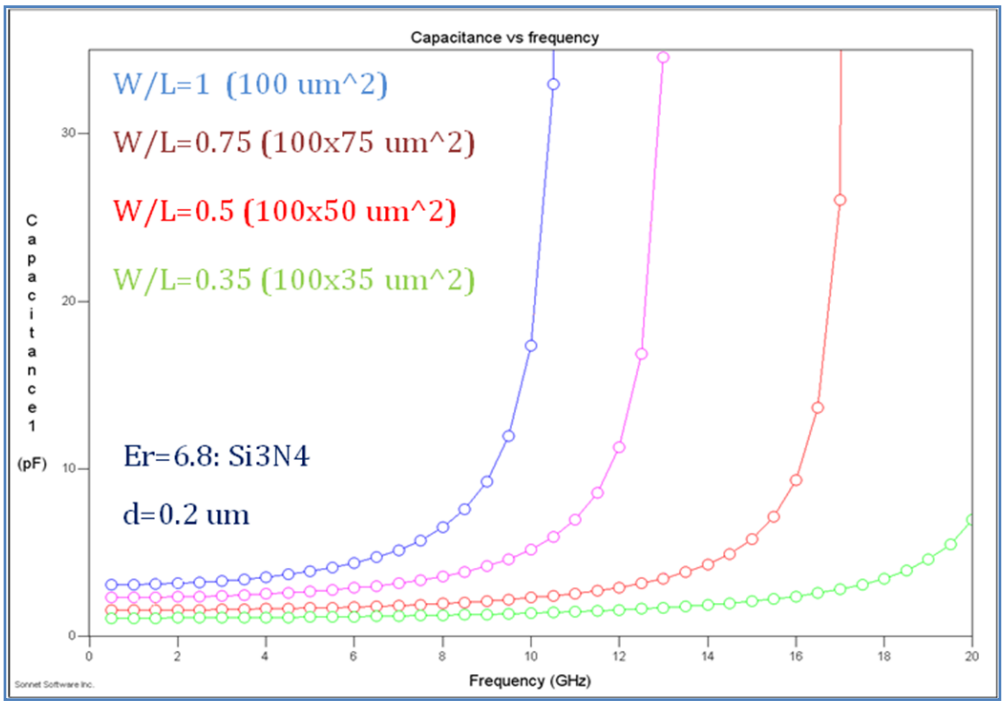


Figure 8.15 - Capacitance with frequency changing aspect ratio W/l = 1.0, 0.75, 0.5, 0.33.

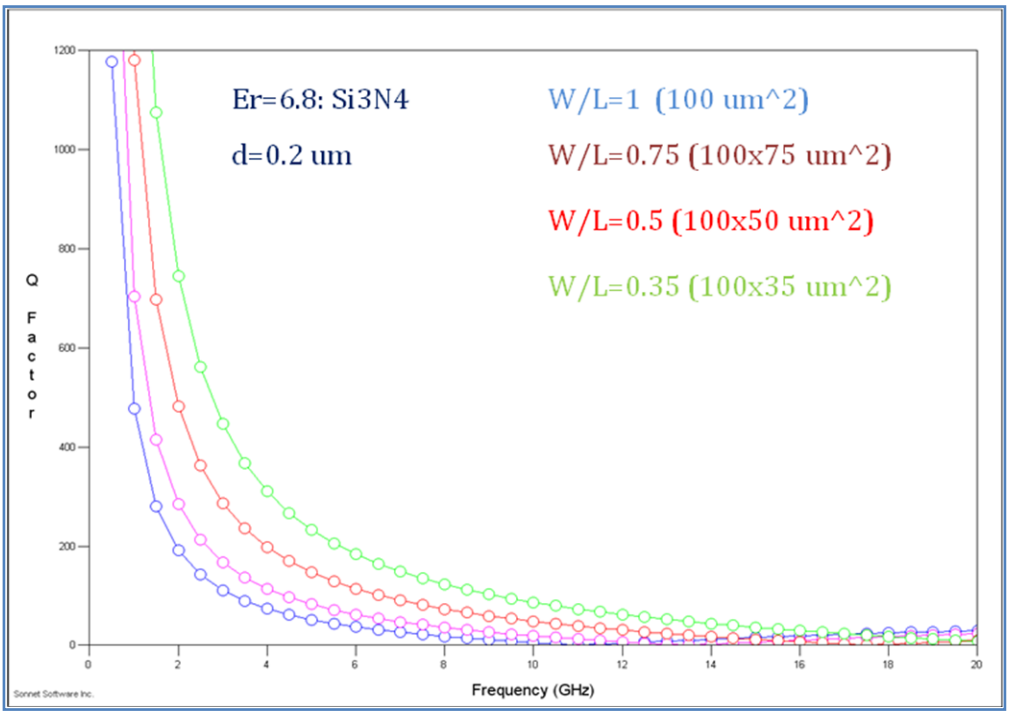
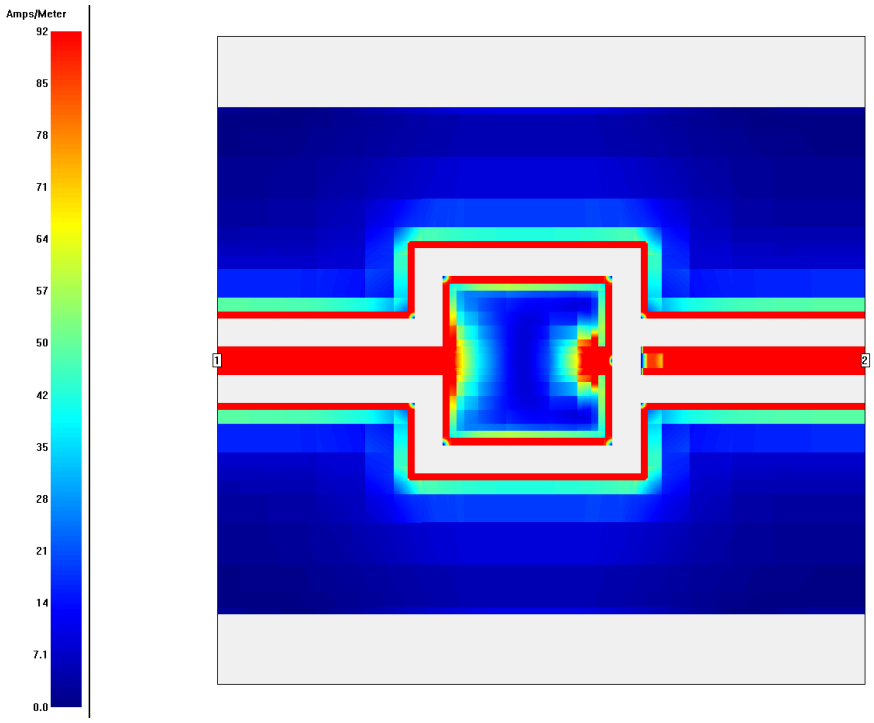
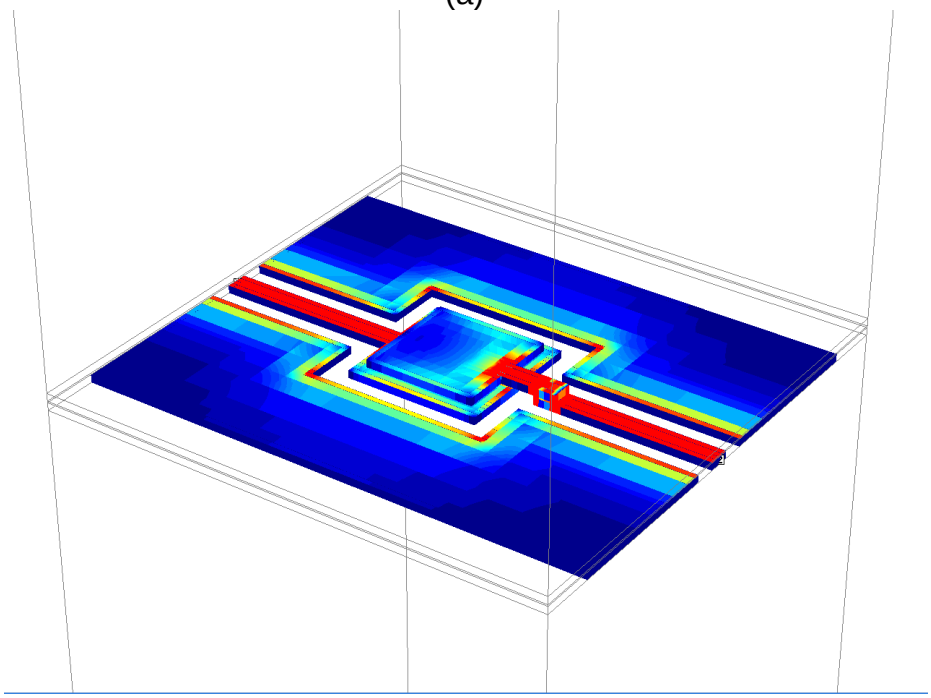


Figure 8.16 - Q-factor with frequency changing aspect ratio W/l = 1.0, 0.75, 0.5, 0.33.

In Figure 8.17 the current flow in a 4-turns inductor @ 5 GHz is shown.



(a)



(b)

Figure 8.17 – Current flow in a 100x100 um^2 @ 5 GHz (a) top (b) 3D view.

Chapter 9

Bi-finger MESFETs results and calibration kit

In this chapter we expose what has been product during the first half of doctorate. In fact, before focusing our attention on passive elements and multi-finger MESFET, we've treated either bi-finger MESFETs or calibration kit.

In the following experimental results of bi-finger MESFETs DC and RF characterization and on-wafer calibration kit are briefly shown.

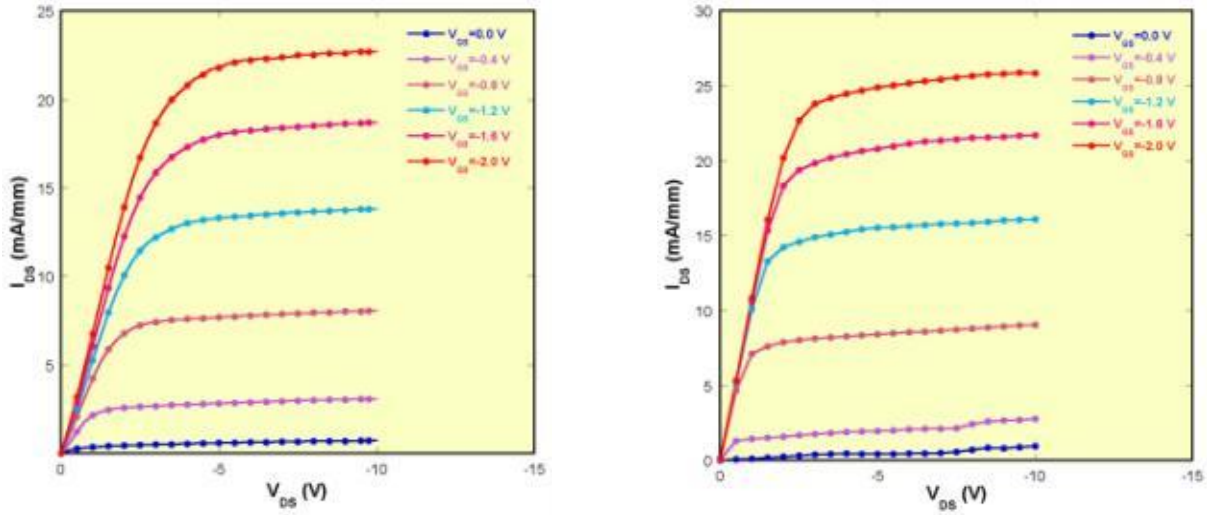
9.1 Bi-finger MESFETs

As far as this typology of MESFETs concern, we don't show process steps again because they are the same as shown in Chapter 4 except for all steps needed to construct air-bridge (so referring to Figure 4.9 we use only the first five points) and we go straight towards their characterization.

We've made measurements of output characteristics for different gate voltages, from which we've obtained input characteristics and transconductance trends.

S-parameters measurements have allowed us to determine RF performances of our MESFETs. DC characterization has been performed using HP4140B. It has two generators with a common ground and one pico-current meter. An external circuit, inserted in a metal box, is used to obtain the desired configuration. In this way we can change continuously drain voltage and measure output current, fixing gate voltage. Data acquisition is made by using a LabView interface and a HPIB board.

Using this measurement setup, we have obtained the bi-finger MESFETs output characteristics I_{ds}-V_{ds}, as shown in Figure 9.1. It's clear, from the sign of supplied polarizations and current, that what is presented is related to a p-channel FET. We are referring to gate dimensions of 0.2x25 μm^2 and 0.5x50 μm^2.



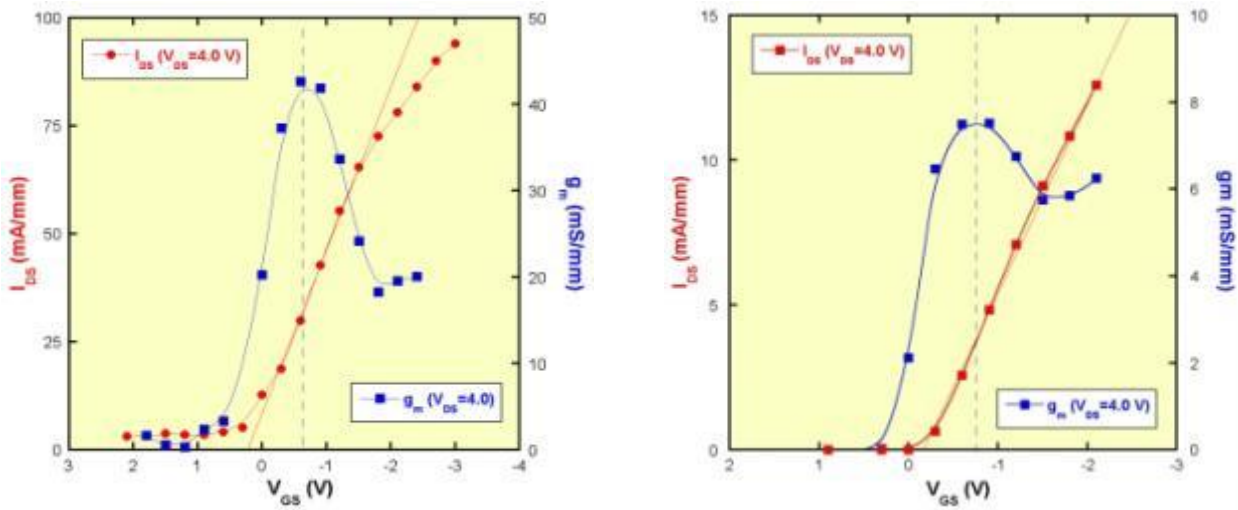
(a) (b)

Figure 9.1 - Output characteristics for different gate-source voltages of (a) 0.2x25 μm^2 MESFET and (b) 0.5x50 μm^2 MESFET.

Device saturation current, with a low V_{GS} level, can be approximated with the following expression:

$$I_{DSsat} = k\left(V_{GS} - V_{th}\right)^2 \qquad (9.1)$$

where V_{th} is the threshold voltage (where we have the complete channel depletion). From the square root of drain current I_{ds} with V_{gs} voltage we can extrapolate V_{th} value.



(a) (b)

Figure 9.2 - Input characteristics for different gate-source voltages and fixed drain-source voltage of (a) 0.2x25 μm^2 MESFET and (b) 0.5x50 μm^2 MESFET.

In Figure 9.2 the curves of two different transistors are represented. The first one (a) is referred to a 0.2x25 μm^2 self-aligned FET where we have a threshold voltage V_{th} = -0.2 V, while the second one (b) is referred to a 0.5x50 μm^2 fixed drain-source distance with a V_{th} = 0.1 V. For both of devices we've chosen a drain voltage V_{ds}= -4 V.

As far as device breakdown concern, we have polarized our devices with V_{ds} = -90V and V_{gs} = 0V, as shown in Figure 9.3. We must note that, with these voltages, we are still in saturation zone.

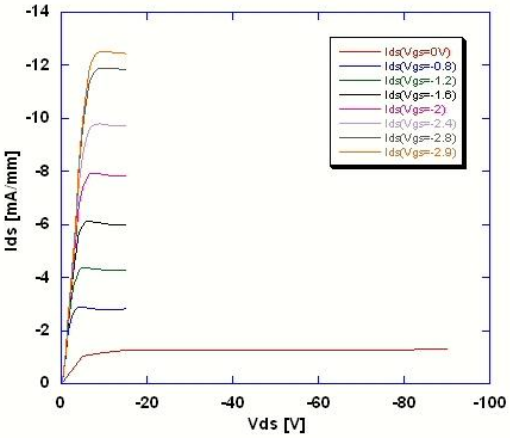
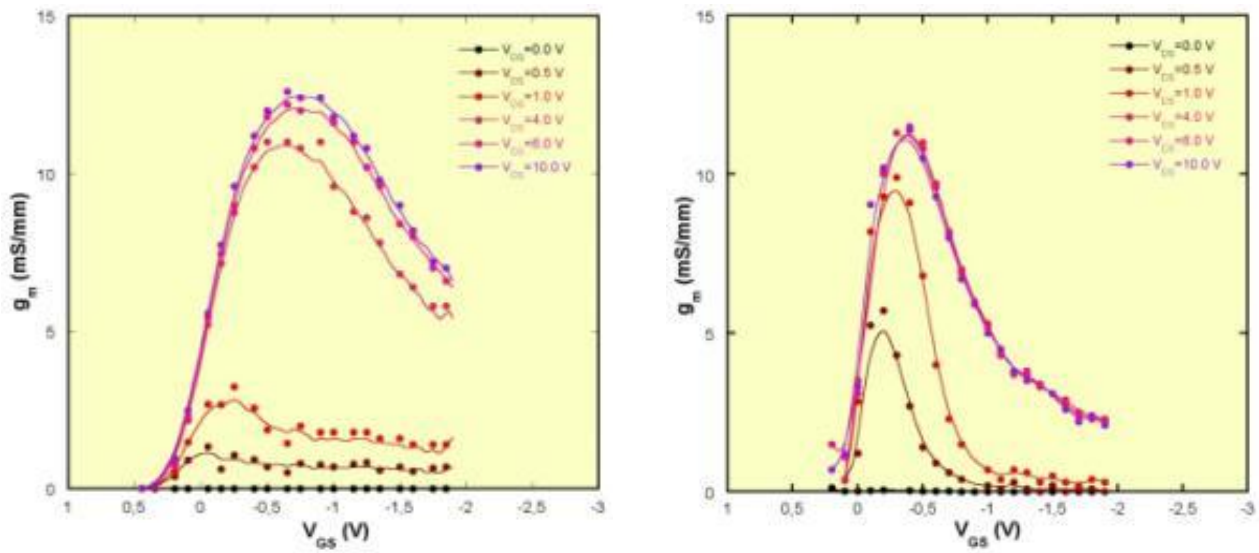


Figure 9.3 – Ouput characteristic of 0.5x50 μm MESFET: we have polarized our devices with V_{ds} = -90V and V_{gs} = 0V but, with these voltages, we are still in saturation zone.

From input characteristic data we can obtain, from numerical derivation, the transconductance trend, remembering that:

$$g_m = \left.\frac{\partial I_d}{\partial V_{gs}}\right|_{V_{ds}=\mathrm{cost}} \tag{9.2}$$

In Figure 9.4 the g_m with V_{gs} of 0.5x50 μm^2 and 0.5x25 μm^2 MESFETs for different V_{ds} values are shown. The maximum of g_m was obtained for a 0.5x50 μm^2 MESFET, for V_{ds} = -10V e V_{gs} = -0.4V and its value is 12.5 mS/mm.



(a) (b)

Figure 9.4 – Transconductance of (a) 0.5x50 μm^2 and (b) 0.5x25 μm^2 for different V_{ds} voltages.

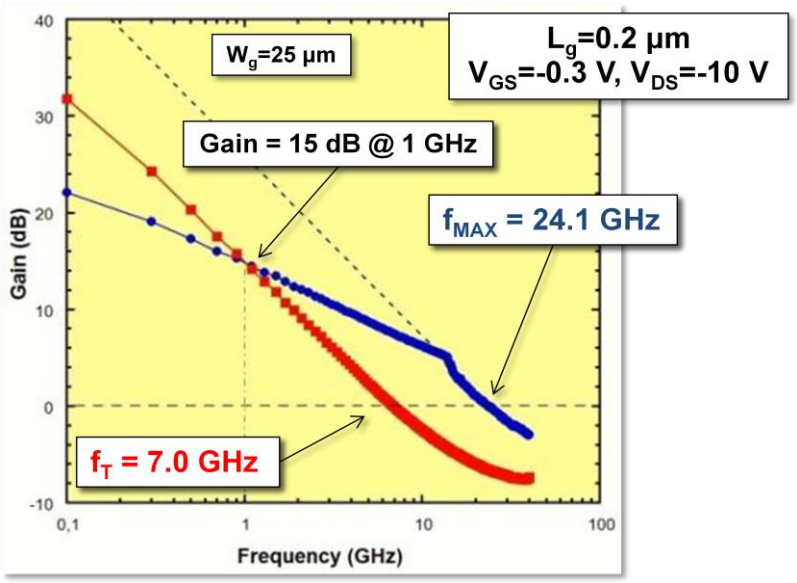
RF characterization was made at Tor Vergata University labs using a two-port vector network analyzer, where we've measured S-parameters real and imaginary part of our MESFETS. With these parameters we've obtained input-output reflection coefficients ($|s_{11}|$, $|s_{22}|$), direct and inverse power gain ($|s_{21}|^2$, $|s_{12}|^2$), current gain ($|h_{21}|^2$) and maximum available gain (*MAG*) trends, in a frequency range from 100 MHz to 100 GHz.

Very interesting for RF device performances is the transition frequency (f_T), defined as the frequency where the current gain is equal to one. There is an important relation, as first approximation, between f_T and DC MESFET characteristics, given by the following expression:

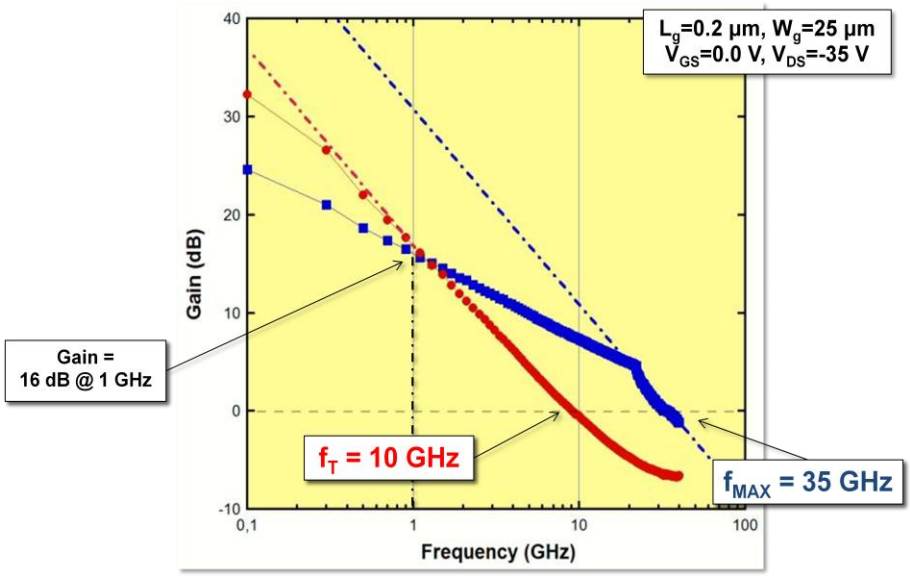
$$f_T = \frac{g_m}{2\pi C_{gs}} \tag{9.3}$$

Where g_m is the transconductance and C_{gs} is the capacitance between gate and source electrodes. *MAG* and $|h_{21}|^2$ best results were obtained, as predictable, on devices with gate length L= 0.2 μm e gate width W= 25 μm, with a polarization of V_{gs}= 0V and V_{ds}= -35V. In Figure 9.5

we can appreciate either *MAG* or $|h_{21}|^2$ for two different polarization on the same device: the dimensions were 0.2x25 μm^2 and the voltages were (a) V_{gs}= -0.3V and V_{ds}= -10V and (b) V_{gs}= 0V and V_{ds}= -35V.



(a)



(b)

Figure 9.5 – Current gain and maximum available gain for a 0.2x25 µm^{2}device at different polarizations.

As it's shown in Figure 9.5, as our best performances we've obtained G_{max}= 35 GHz and f_T = 10 GHz. All measured devices have a current gain included between 30 and 35 dB and a maximum available gain between 22 and 25 dB @ 0.1 GHz.

Figure 9.6 shows where our results are set in the scientific world and how we're improving, year by year, our technology and comprehension of diamond MESFETs working.

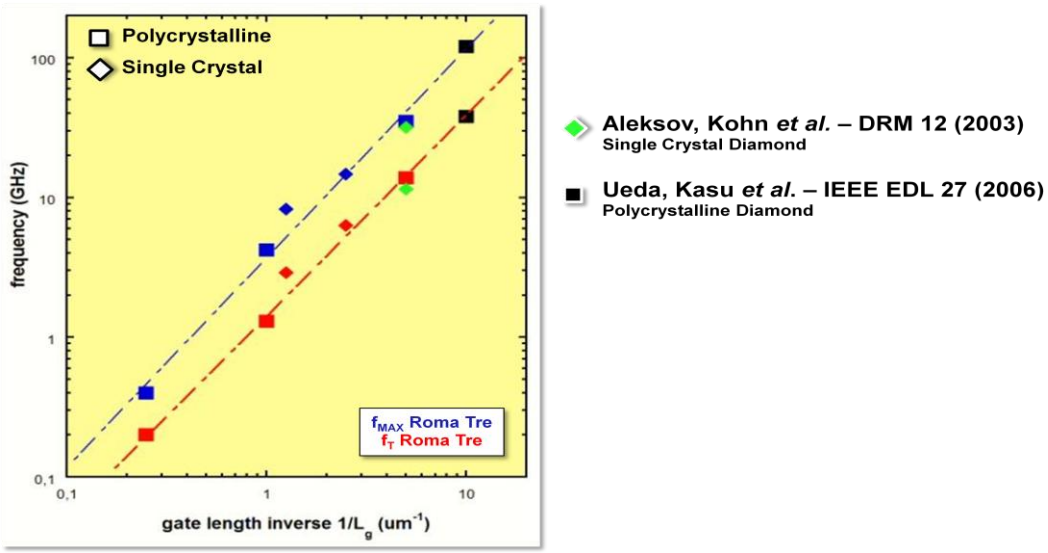


Figure 9.6 – Diamond Roma Tre lab and world research history.

9.2 Calibration kit

The application of H-terminated diamond for high frequency MESFETs construction requires accurate on-wafer S parameters measurement by planar probe and Vector Network Analyzer (VNA). Therefore, a calibration procedure able to remove systematic errors due to measurement set-up non-idealities (related to VNA, cables, connectors and planar probes) is required. To reach this goal, a measurement of proper calibration standard (partially or fully know) is required in order to define the error box parameters used for non-idealities correction. This can be simply performed by using a commercial (off-wafer) calibration impedance substrate kit, or more precisely through a on-wafer calibration kit realized on the same substrate of device under test. Difference between the two approaches relies on the ability to remove the parasitic contribution introduced by the probe-pad transition, for a particular substrate and geometrical structure.

So a custom calibration kit has then designed for accurate RF MESFET characterization and equivalent circuit identification. The main motivation that imposes the on-wafer choice is the necessity of remove the impedance discontinuity and influence of parasitic contribution to the measurement of intrinsic MESFET. In such a way, reference planes are placed in a uniform transmission line section beyond the contact pad. On the contrary, the off-wafer approach places the reference planes at the probe tips, as depicted in Figure 9.7. On-wafer calibration ensures the possibility to access the intrinsic device without implementing de-embedding procedure, obtaining more accurate information on active device characteristics and performance.

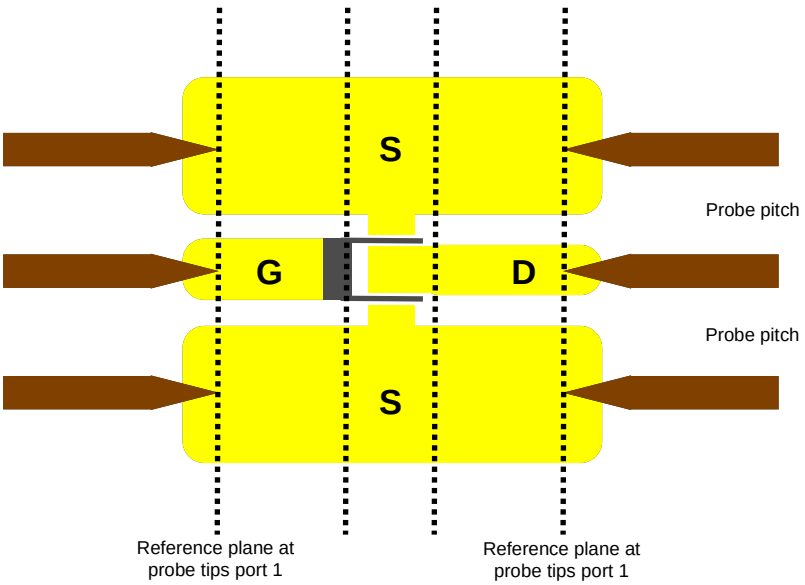


Figure 9.7 - Reference planes for different calibration approaches.

The solution proposed for this task is to implement a Line-Reflect-Reflect-Match (LRRM) [22] calibration which uses a space conservative standard set which consist of a matched Line (Thru) of short delay, two Reflection standard (Open and Short) partially unknown (only the phase is needed) and a Match that must be known only in the DC resistance component of its impedance.

In fact, by the measurement of the two reflection standards is possible to characterize the reactive component of the Match standard impedance described by the RL series (DC resistance - accurately known - and inductance – unknown) [23]. In particular, it is also possible to determine the line propagation constant and move the reference plane without loss of accuracy [24,25].

The main aspects regarding the four standards (shown in Figure 9.8) are:

- LINE (CPW – Coplanar Waveguide): it is based on the MESFET layout and employs metal layers (200 nm thick Au layer). The delay introduced by the line must be less than 1 ps, with a 50 Ω characteristic impedance.
- REFLECT$_{1,2}$: Short and open realized with a metallic stripe and pad respectively, with the same characteristics of the MESFET metallization.
- MATCH: only one match is required by the algorithm. For this standard it's mandatory to have exactly 50 Ω of DC resistance value. In CPW technology this is realized by two 100 Ω resistors in parallel. The resistance are realized with thin film technology by CVD deposition on Ni-Cr (80%-20%) film on oxygenated diamond.

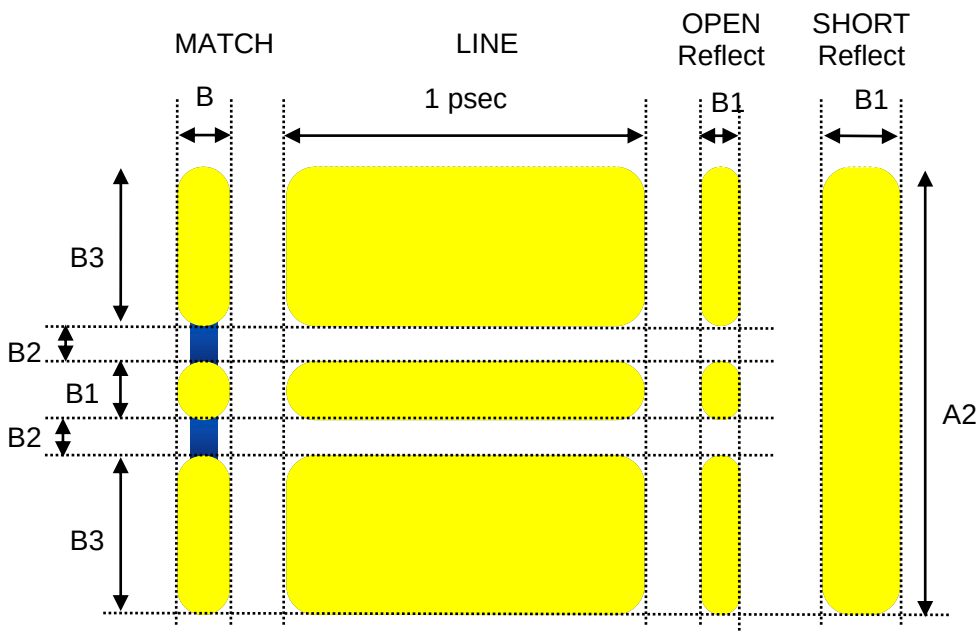
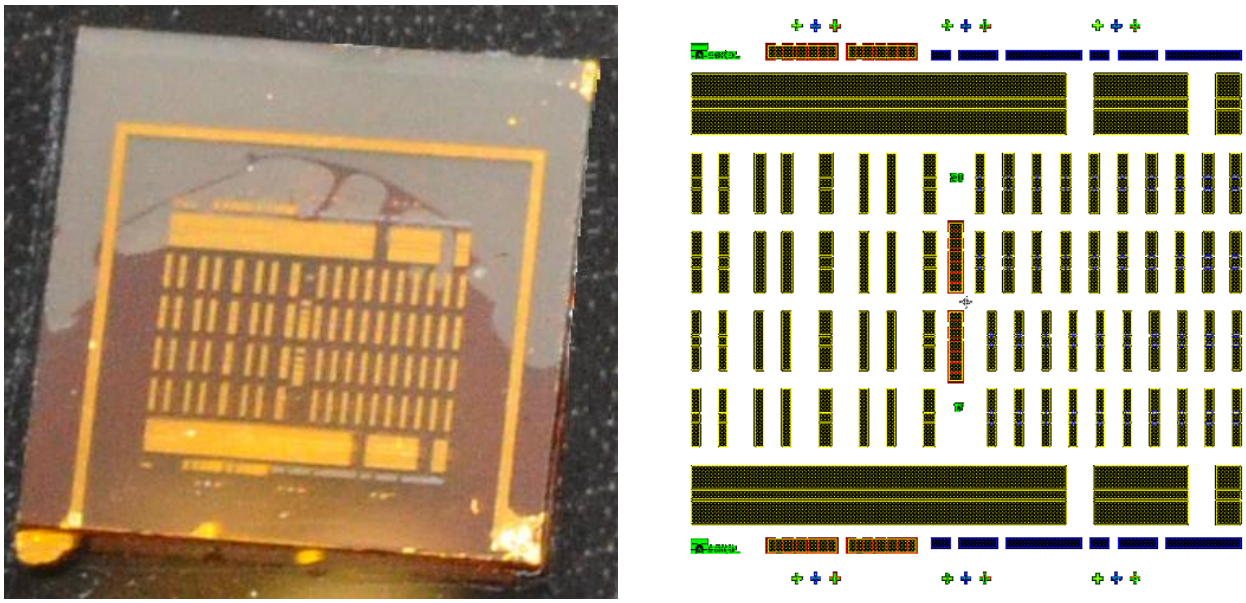


Figure 9.8 - LRRM Calibration standard layout referred to geometrical characteristics of MESFET reported in Figure 9.7

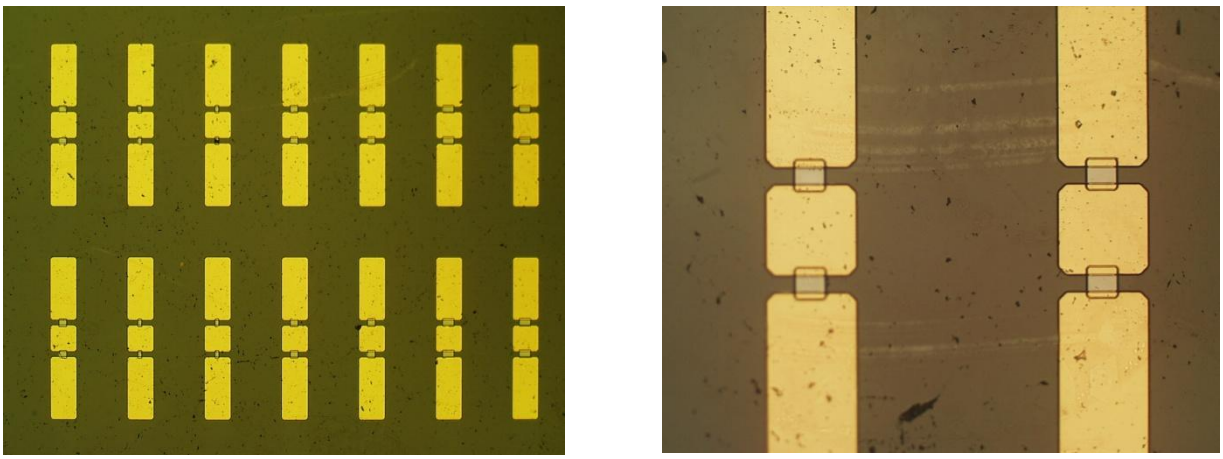
In Figure 9.9 we show either (a) the actual diamond calibration kit or (b) designed mask using LASI 7 software. For ohmic contacts we've used 200 nm of Au, while for resistors we have used a thin Ni-Cr film of 25 nm.



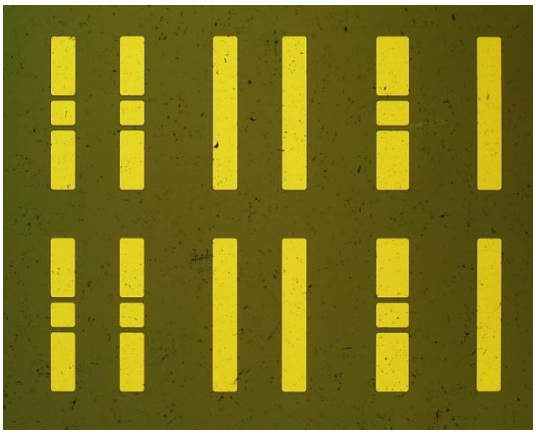
(a) (b)

Figure 9.9 - Manufactured diamond calibration kit and (b) designed mask using LASI 7 software.

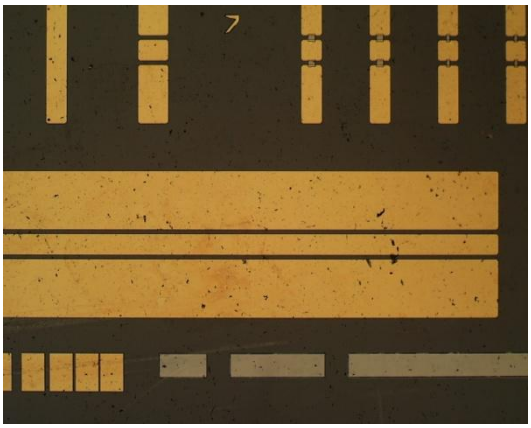
In Figure 9.10 some details are shown. In particular we can see (a) (b) Ni-Cr resistors with different values , (c) open and short standards and (d) (e) lines and Ni-Cr strips.



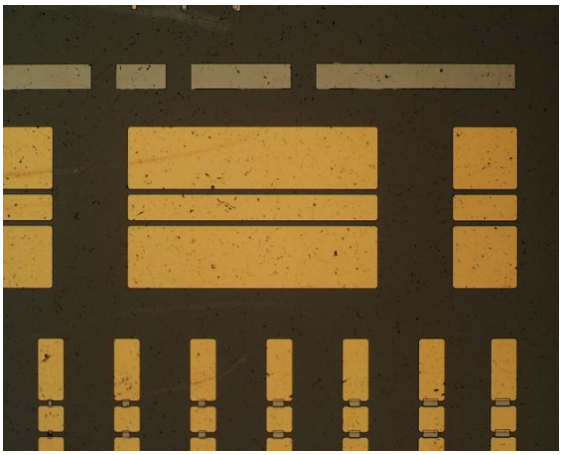
(a) (b)



(c)



(d)



(e)

Figure 9.10 - Some details of diamond calibration kit. In particular we can see (a) (b) Ni-Cr resistors with different values , (c) open and short standards and (d) (e) lines and Ni-Cr strips.

Conclusions and future works

During the doctorate research activity we've developed and optimized the use of air-bridge technique and gold electroplating on small dimensions polycrystalline diamond substrate (1 cm^2). This technique is a standard process in MMIC GaAs and Si manufacturing, but it was never used before on diamond devices. Thanks to this process we've constructed either polycrystalline diamond multi-finger MESFETs or passive elements like inductors and capacitors.

As far as diamond MESFETs concern, we've constructed and optimized all process steps, starting from the "simpler" bi-finger MESFETs, those have brought us DC and frequency domain remarkable results, and arriving to multi-finger MESFETs (ten fingers). We've fixed the gate width W at 100 μm, while we've used different gate lengths L as 0.5, 1.0, 2.0, 4.0 μm.

Referring to polycrystalline diamond inductors, we've constructed multi-turn devices with conductor width W=20 μm, spacing between turns S=20 μm and inner diameter D_i =100 μm, varying the number of turns n from 1.5 to 5.5, while for diamond capacitors, we've chosen the square configuration having the following parameters: dielectric thickness d = 2 μm height, material dielectric constant ε_r =2.6 (PMMA) and plates area that varies from 50x50 μm^2 to 200x200 μm^2.

In order to allow the doctorate project we've used polycrystalline diamond samples bought from Element Six Company (E6). For multi-finger MESFETs substrates we have used a polycrystalline diamond sample labeled TM180. Its thickness and dimensions are, respectively, 250 μm and 1 cm^2. Its surfaces have been submitted to mechanical polishing to reduce surface roughness in order to allow lithographic processes. At the end of this process the roughness is less than 50 nm. Instead, for passive elements substrate, we have used the TM100 polycrystalline diamond. The main differences between this sample and

the previous one are the different thickness (500 μm for TM100 vs 250 μm for TM180) and different thermal conductivity ($1000Wm^{-1}K^{-1}$ vs $1800Wm^{-1}K^{-1}$). The medium grain size of both kind of material is about 20 μm and their "electronic quality" is not so good as that used for bi-finger MESFET, so we couldn't expect high performance devices. But it's not a problem because, with this work, our goal was only the construction of devices without heading to performances.

If a high resistive substrate is a necessary condition to obtain high performance passive devices, as in our case, for MESFETs construction we need high conductivity areas where the transistor channel takes effect. To make conductive the diamond surface we've use an hydrogen plasma, making this step at CNR – IMIP lab (Istituto di Metodologie Inorganiche e Plasmi) of Montelibretti. To remove this conductive channel, for device isolation process we've used a RIE process with a mixture of oxygen and argon.

During all diamond devices processes made up to now by our lab, one of the most important problems noticed during all processes has been the gold adherence on diamond substrate (hydrogenated and oxygenated). As previously described in Chapter 6, the bad adherence of gold over a large range of materials is a feature of this metal due to its intrinsic properties as slow electronic affinity. With this work we've tested a new solution for ohmic/first metal layer, and overcome this problem, changing from only Au to Ti/Au evaporation. In fact this first thin layer of Titanium (20 nm) is necessary to improve the adherence of contact.
Instead, for gate contact, we've used Al evaporation as in the previous work because it allows a good Schottky diode.

At the time of writing this thesis, we are waiting for measurement results on passive devices from Selex S.I. As far as bi-finger MESFETs concern, we've manufactured RF devices with gate lengths L of 0.2 μm having good DC and RF performances: in fact we've reached a maximum transconductance g_m of 70 mS/mm, a maximum drain current I_D of 100 mA/mm, f_T = 10.5 GHz, f_{max} = 35 GHz and output power = 1W/mm @ 1GHz.
Instead, for multi-finger MESFETs, we're constructing another batch to make measurements on it, because we've had an unfortunate problem, as described in Chapter 7, that hasn't allow us to evaluate devices performances.

We've simulated the frequency behavior [0-20 GHz] either of diamond inductors or capacitors using the SONNET electromagnetic simulator. For inductors having W=S=20 μm and D_i =100 μm, we expect inductance values from 0.66 nH (for 1,5 turns) to 9.3 nH (for 5.5 turns) while for diamond capacitors with square configuration and d = 2 μm, ε_r =2.6 (PMMA) we expect capacitance values from 0.04 pF (for 50x50 μm^2 area) to 0.52 pF (for 200x200 μm^2area).

In order to allow an accurate on wafer S-parameters measurement by planar probe and Vector Network Analyzer and equivalent circuit identification of diamond MESFETs and passive elements, we've realized a diamond calibration kit based on a LRRM standard. The main motivation that imposes the on-wafer choice is the necessity of remove the impedance discontinuity and influence of parasitic contribution to the measurement of intrinsic device without implementing de-embedding procedure, obtaining more accurate information on device characteristics and performance.

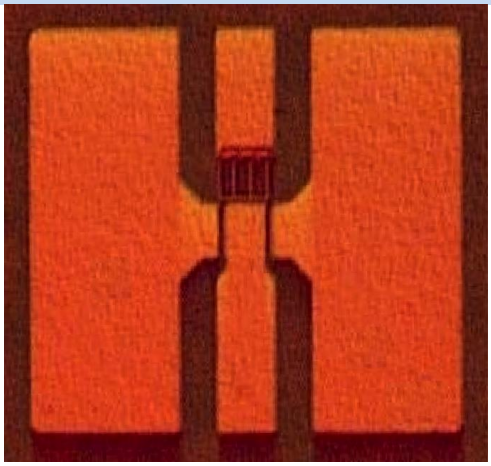
Let we understand, after we've summarize our results, where this doctorate work is set in the scientific world. First of all, talking about bi-finger MESFETs, there are only two groups in the world (Prof. Kasu's and Prof.Kohn's groups) those have constructed devices with better performances than ours.

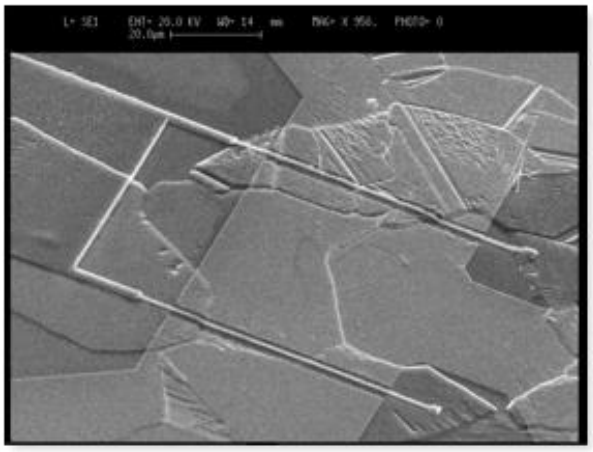
As far as other devices concern, so multi-finger MESFETs, inductors, capacitors and calibration kit, a research made about these devices on a poly/mono-crystalline diamond substrate has product no results, so officially we are the first group in the world that has implemented the air-bridge technique on diamond and constructed this kind of devices. For this reason the realization of this project could be bring our lab to assume a prime importance role on diamond technology and it should open new industrial horizons.

In Figure A we can see the evolution of our technological process applied to bi/multi-fingers MESFETs, inductors and capacitors.

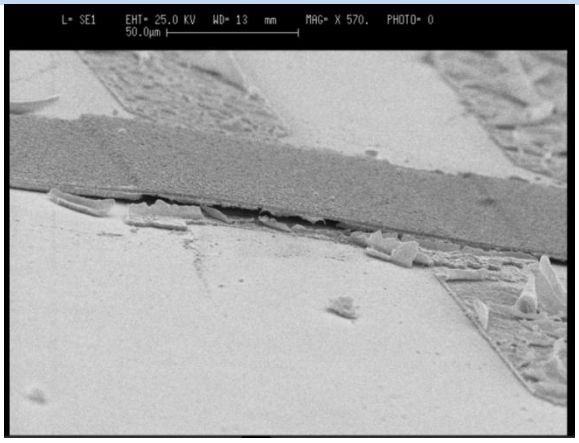
START	ARRIVAL

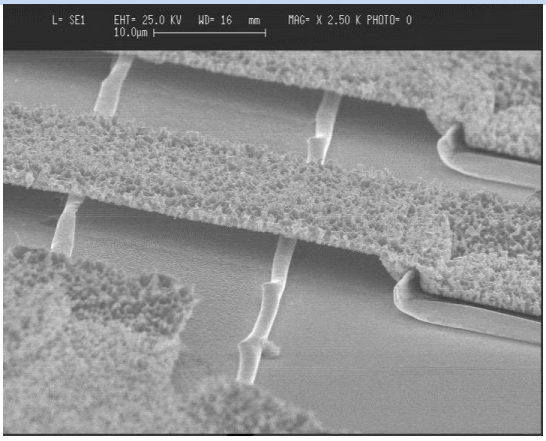
BI-FINGER MESFETs

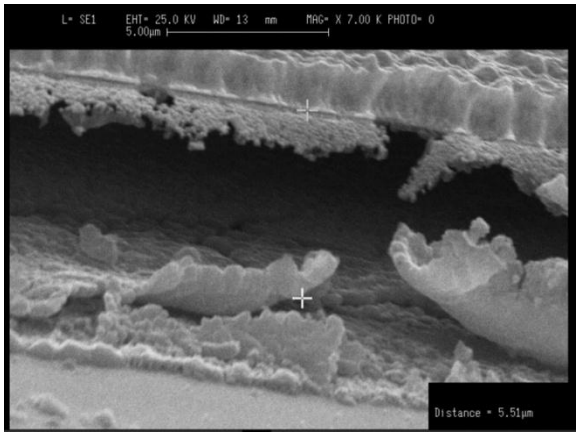


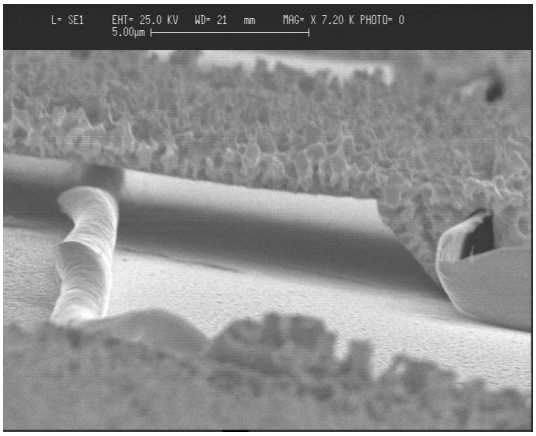


AIR-BRIDGEs

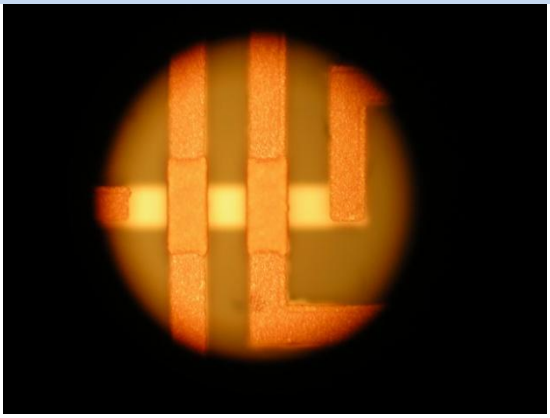


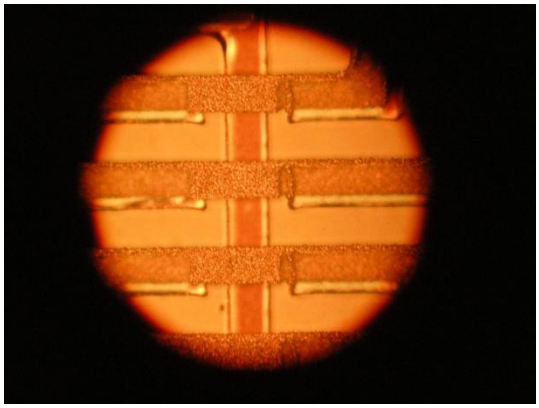


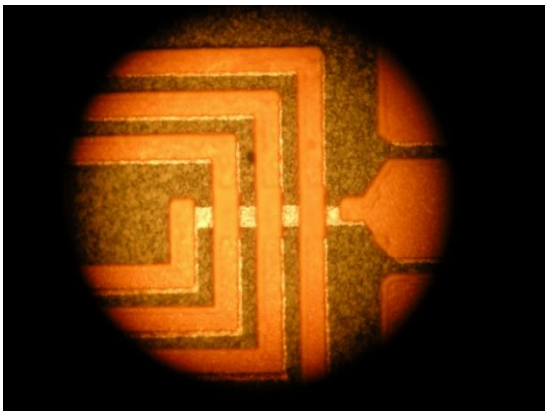


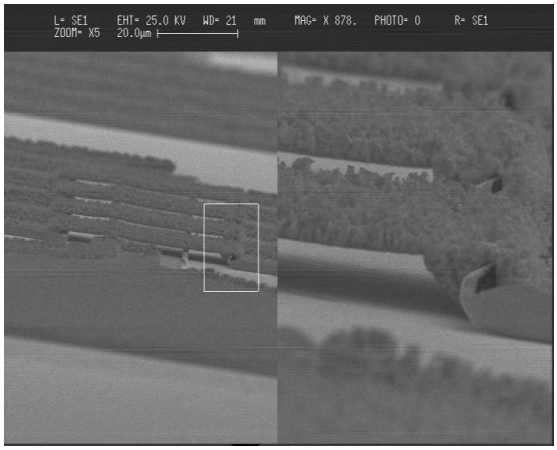


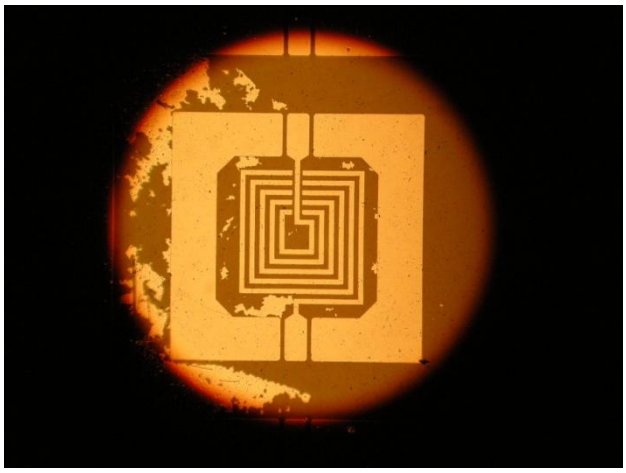
INDUCTORs

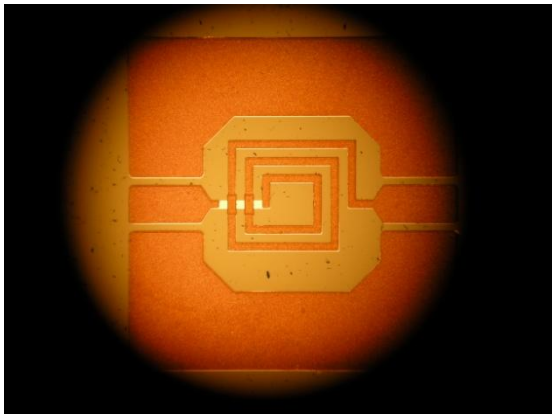




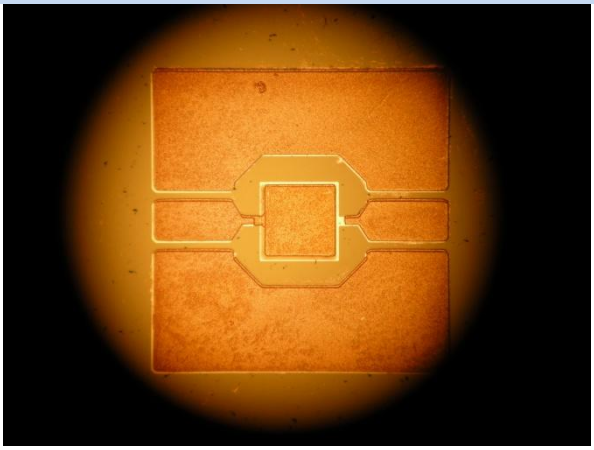


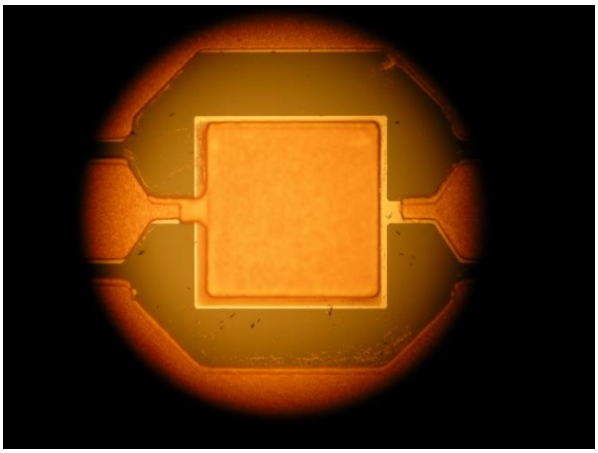




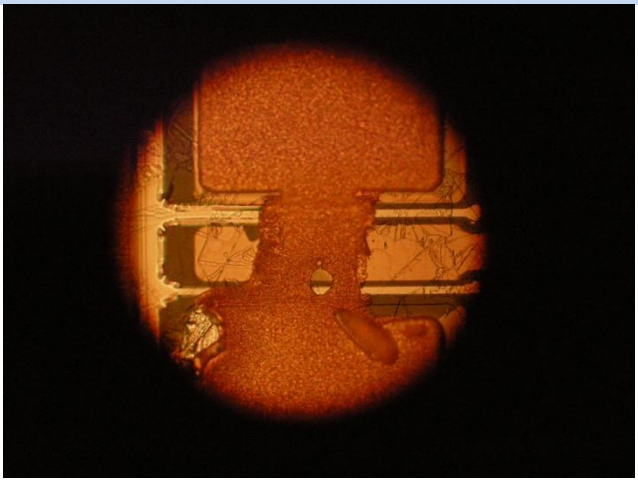


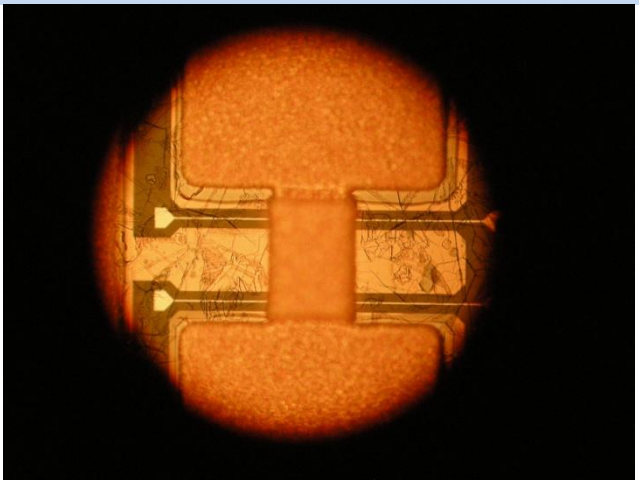
CAPACITORs





MULTI-FINGER MESFETs





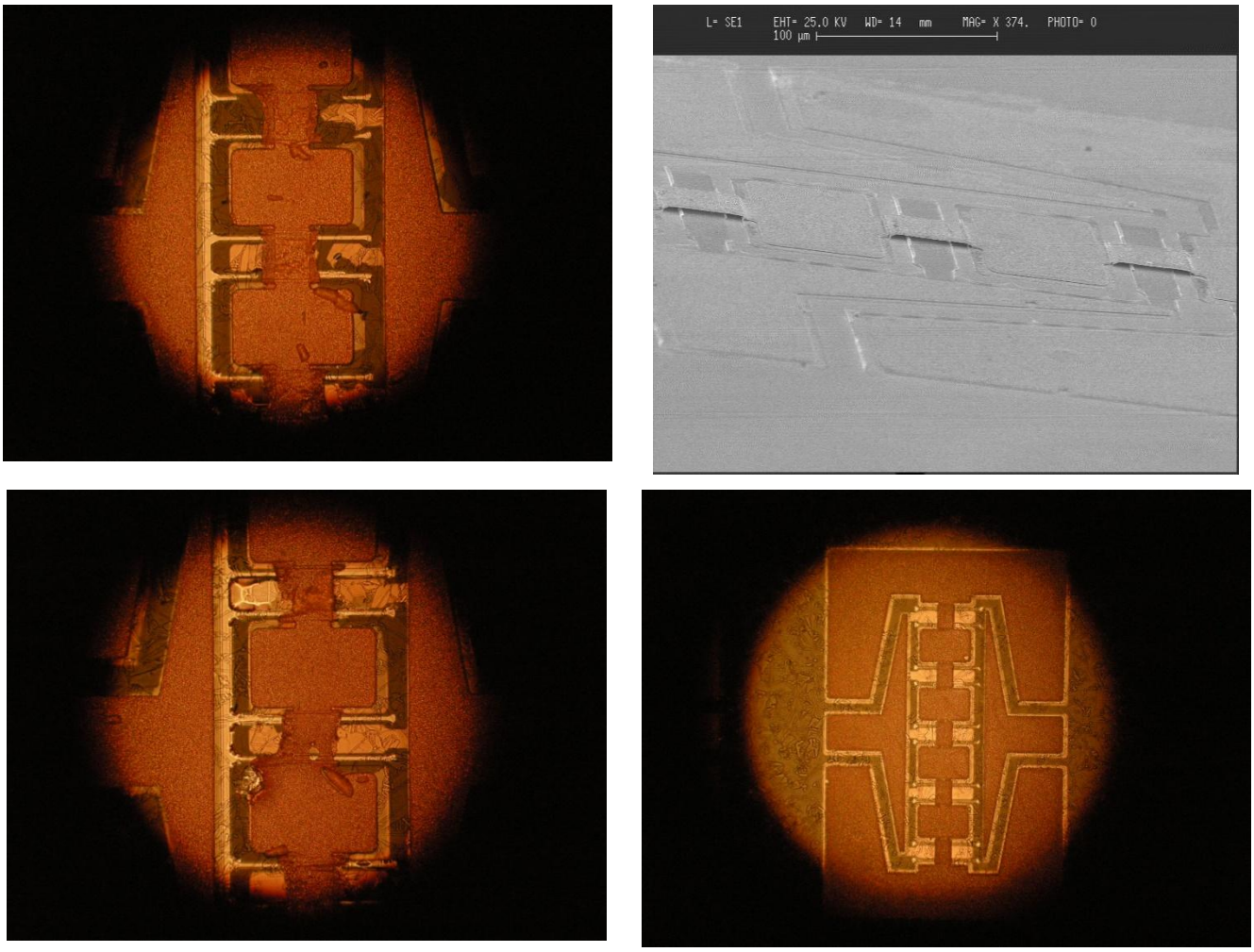


Figure A – Evolution of our technological process applied to bi/multi-fingers MESFETs, inductors and capacitors.

Future works plan the steps shown in Figure B as the continuation of what is shown in Figure 1.4. As we can see, we need to modify inductors and capacitors layout according to geometric considerations in order to improve their performances. After that we must simulate devices with these modifications and, if the EM answer is good enough, proceed to manufacture the optical mask. Moreover, after the construction of new devices, we must measure them and compare the actual and simulate behaviour. The total result will be a complete trend analysis with parameters variation.

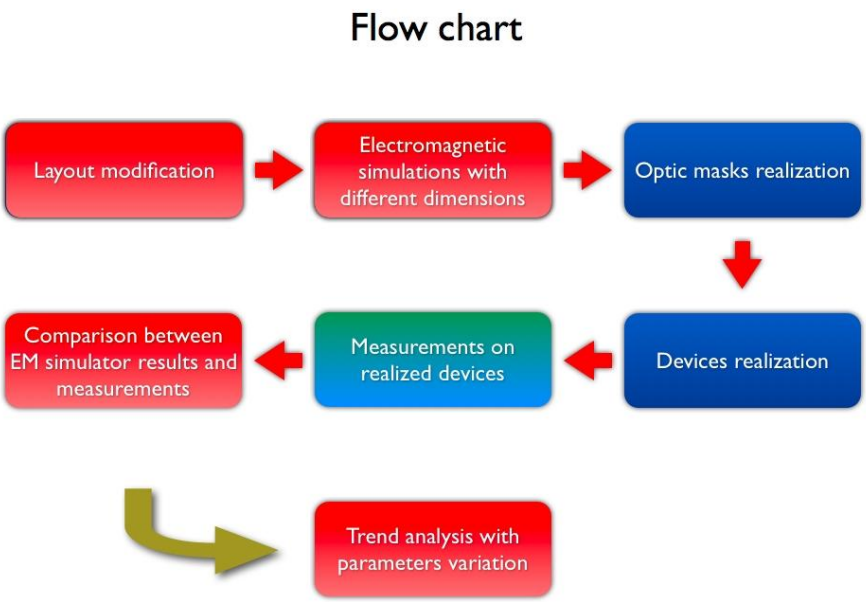


Figure B – Structure of the future works. It's shown the flow chart to obtain a complete trend analysis of devices.

Talking about multi-finger MESFETS we could improve device performances carrying out the following changes:

- Using high quality polycrystalline diamond substrates, with medium grain size of 100 μm;
- Placing gate fingers not in the middle between drain and source pads but closer to the last one to reduce source resistance R_s and to increase breakdown voltage;
- Reducing gate length to improve RF performances;
- Reducing gate-source and gate-drain distances to reduce channel resistance;
- Using a T-gate, or a Γ-gate to reduce gate resistance R_g and to increase breakdown voltage

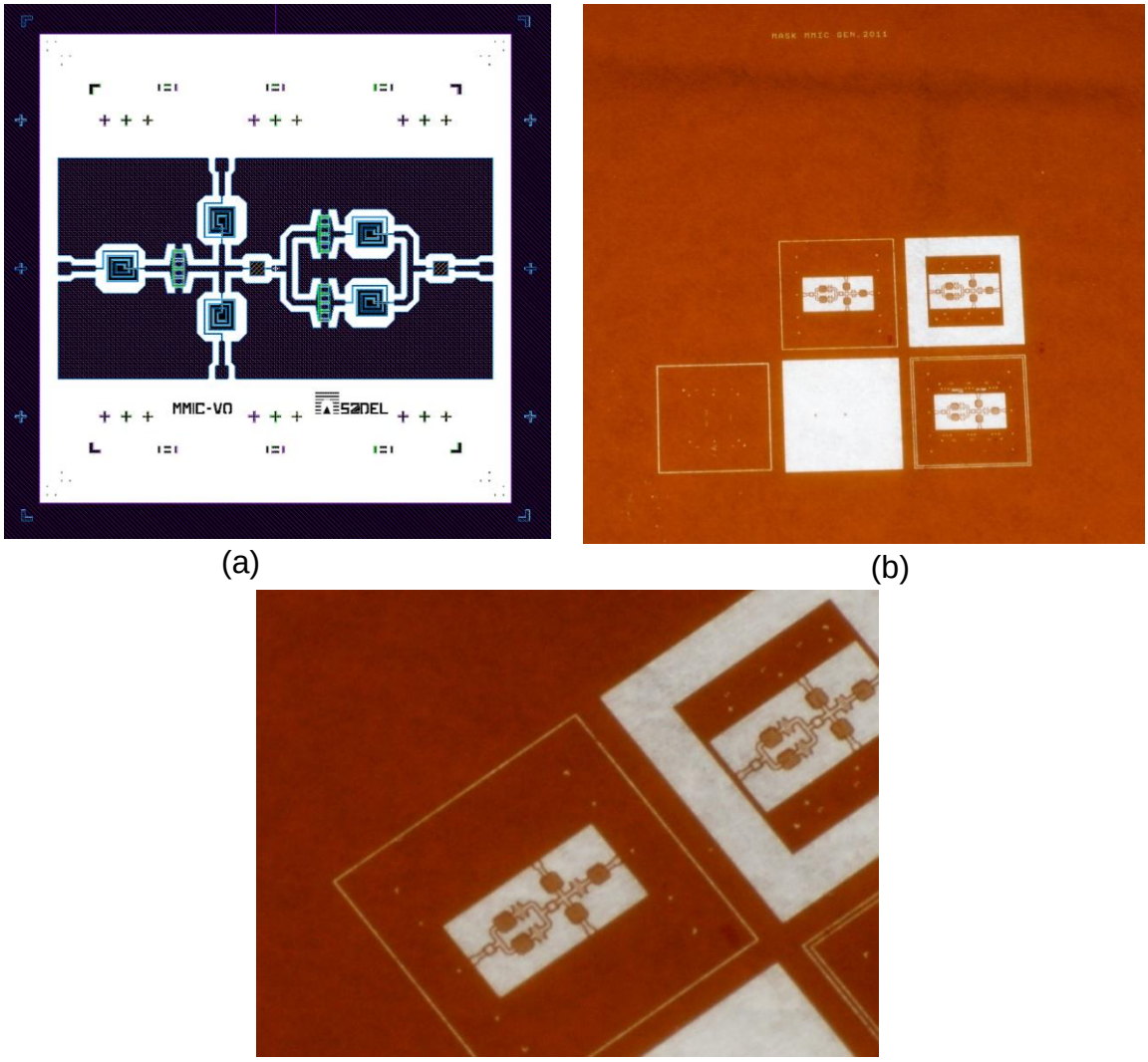
As far as bi-finger MESFET concern we could improve DC and RF performances using the electroplating technique to thicken contact metallization in order to reduce pad resistances.

A further step to improve all RF measurements on diamond devices is to develop a new calibration kit based on the final and fixed devices layout. In fact, what we have designed during our work is not applicable to our devices because we've changed the distances between conductors and their dimensions. Moreover, in this new calibration kit, we must use the electroplated gold to thicken and strengthen contacts: in fact, in the previous one,

we had only 200 nm of evaporated Au, that is very fragile when we put probes over it. Just after two/three times we had scratched all pads on it.

Last future work could be the construction of a diamond MMIC technological demonstrator, in order to demonstrate our capability to process at the same time all our devices. The mask set is just designed and fabricated and it's shown in Figure C. The entire process is divided in six steps that are listed below:

- *Ohmic contact*
- *Isolation*
- *Dielectric deposition*
- *Gate contact*
- *Seed layer*
- *Gold electroplating*



(a) (b)

(c)

Figure C – (a) designed and (b) (c) constructed mask set for MMIC technological demonstrator.

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- P. Calvani, F. Sinisi, A. Corsaro, M. Girolami, D.M. Trucchi, M.C. Rossi, G. Conte, S. Carta, E. Giovine, S. Lavanga , E. Limiti , V. Ralchenko ***"DC and RF Performance of surface channel MESFETs based on hydrogen terminated polycrystalline diamond"***, Diamond and Related Materials18, pp. 786-788,(2009)
- P. Calvani, F. Sinisi, A. Corsaro, M.C. Rossi, G. Conte, E. Giovine, E. Limiti ***"Microwave operation of sub-micrometer gate surface channel MESFETs in polycystalline diamond"***, GeMIC 2009 (ITG-FB 213). vol. 213, BERLIN: VDE Publishing House, ISBN/ISSN: 978-3-8007-3150-3 (2009)
- F. Sinisi, P. Calvani, L. Mariucci, M.C. Rossi, G. Conte, E. Limiti, S. Lavanga, C. Lanzieri, A. Cetronio, V. Ralchenko, ***"Sub-micron gate length MESFET on hydrogen terminated polycrystalline diamond",*** IJMOT, VOL. 3, NO.3, July 2008, pp. 235-242 ISSN: 1553-0396.
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- P. Calvani, A. Corsaro, F. Sinisi, M. C. Rossi, G. Conte, S. Carta, E. Giovine, W. Ciccognani, E. Limiti "***Diamond MESFET technology development for microwave integrated circuits***", IEEE 4th European Microwave Week Conference Proceedings (2009), pp. 148-151, ISBN 978-2-87487-010-1
- P. Calvani, A. Corsaro, F. Sinisi, M.C. Rossi, G. Conte, S. Carta, E. Limiti "***Microwave Performance of Surface Channel Diamond MESFETs***", IEEE Nanotechnology Materials and Devices Conference proceedings (2009), pp. 200-204, ISBN/ISSN: 978-1-4244-4696-4

Schools and courses

- Seminar title: ***"Diamond films for electronics: growth, treatment and characterization"***, Speaker: Prof. V. Ralchenko, General Physics Institute of Russian Academy of Science, Moscow, Russia.
- International School on advanced Microelectronics: MIGAS'08 - 11th session
- ***"Nanoscale CMOS and Si-based beyond CMOS nanodevices"***, Autrans, Grenoble, France.
- Course on: ***"RF IC design in nanometer CMOS"***,
- Speaker: Prof. Piero Andreani, Department of Electrical and Information Technology, Lund University, Sweden.

Conferences

- *18th Diamond European Conference, Berlin, Germany (2007)*
- *IV simposio sulle tecnologie avanzate, nuovi orizzonti teorici e applicativi, Roma, (2007)*
- *ISMOT 2007, 11th International Symposium on microwave and optical technology, Roma (2007)*
- *19th Diamond European Conference, Sitges, Spain (2008)*
- *15th MECSA National Symposium, Naples, Italy (2008)*
- *4th German Microwave Conference, Munich, Germany (2009)*
- *10th Ultimate Integration on Silicon Conference, Aachen, Germany (2009)*
- *IEEE Nanotechnology Materials and Devices Conference, Traverse City, Michigan (2009)*
- *20th Diamond European Conference, Athens, Greece (2009)*
- *4th European Microwave Integrated Circuits Conference (EuMIC), Rome, Italy (2009)*

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Luglio 2007. Ore 15.00. Un pomeriggio caldo e afoso, sole a picco e nessuno nel lungo vialone che porta gli studenti verso il Dipartimento. Solo io e la “vasca navale”, che sembra quasi conscia che a breve verrà abbattuta. In fondo a questo viottolo un bivio, una scelta, una decisione da prendere, un’idea che è maturata in primavera e che si sta per concretizzare.
Settembre-Ottobre 2007. Ore 16.00. Dopo una lunga attesa finalmente gli elenchi sono stati affissi. Il mio nome è lì, insieme a quello di alcuni miei compagni. Ce l’abbiamo fatta! Concorso superato! Tutti gli sforzi fatti durante l’estate, le ore passate sui libri a cercare di ripassare un po’ tutto, le rinunce a lunghe vacanze si sono rivelate fruttuose. E’ stata dura ma la soddisfazione è tanta.

Quel giorno è stato l’inizio di un percorso duro, un cammino faticoso ma davvero stimolante, ricco di sfide, talvolta perse talvolta vinte, che mi ha portato qui, seduto all’una di notte di fronte al mio fedele compagno di battaglia (eh si, sto parlando proprio del mio portatile...) a scrivere le ultime righe di un lavoro che, oltre a rappresentare quanto fatto in questi tre anni, racchiude tutta una serie di esperienze professionali ed umane che mi hanno formato e fatto crescere e che mi permetteranno sicuramente di affrontare al meglio il futuro.

Signori e signore, so che stavate aspettando questo momento e non vi faccio attendere oltre. Finalmente dopo tanto penare, è arrivato il momento dei ringraziamenti!!!
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Una sola parola...

...GRAZIE di cuore a tutti!!!

L'orologio segna le tre di notte...gli occhi si fanno sempre più pesanti e domattina mi aspetta un'altra giornata di duro lavoro. Credo sia il momento di spegnere tutto. Mission accomplished.

...“*E quindi uscimmo a riveder le stelle*” *

* Dante, “*La divina commedia*”, Inferno, XXXIV