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Charge Control Devices based on Wide Band Gap Semiconductors

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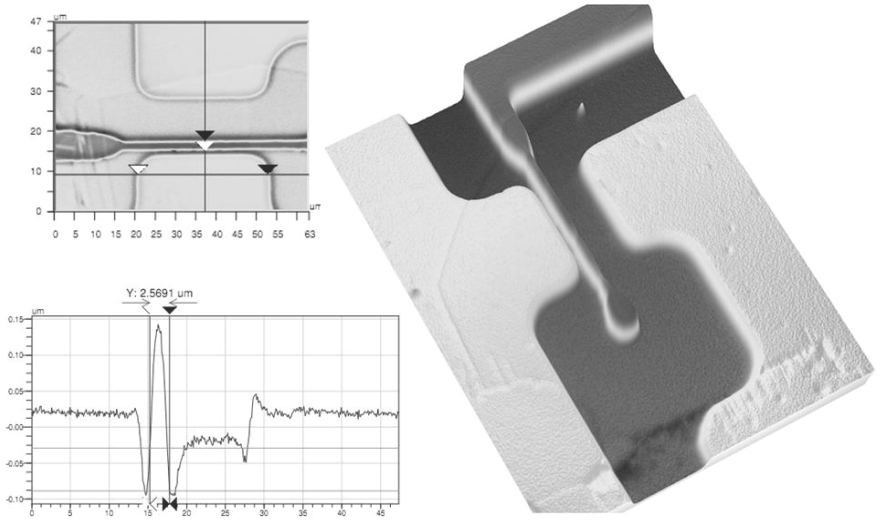

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Abstract

Metal-Semiconductor Field Effect Transistors (MESFETs) based on Hydrogen Terminated Diamond have been fabricated according to different layouts and technologies with different gate lengths. Aluminum self-aligned and fixed drain-source distance (in the following "*standard*") gates and gold ohmic contacts have been fabricated both on single crystal and polycrystalline diamonds supplied by Element Six and by Russian Academy of Sciences. Aluminum assures low ideality factor gate-source diodes, high rectification ratio and low leakage currents (basically higher for polycrystalline samples). Gold contacts, after a hard work of development and improvement, resulted in good mechanical adhesion and strength as well as contact resistivity, lower enough to allow an excellent device operation. The small L_T resulting from transfer length method (TLM) analysis, allows the supposition of a completely lateral charge transfer and hydrogen terminated area dimension reduction close to gate junction does not negatively affect device performances. Hydrogen terminated layer has been deeply investigated by means of Hall bars, TLMs and gate junctions characterization: hydrogen induced two dimensional hole gas (2DHG) results in sheet resistances essentially stable and repeatable depending on substrate quality.

Results achieved for self-aligned and standard FETs fabricated on nominally identical large-grain size, low quality, polycrystalline diamonds TM180 by Element Six are presented and investigated in order to obtain a better understanding of hydrogen terminated diamond transistors. DC characteristics clearly point out the presence of 2DHG as well as an operation typical of hetero-junction FETs. Anyway, achieved results seem to highlight the presence of an effective insulating layer at the aluminum-diamond interface. Self-aligned 200 nm gate length FETs show current density and transcondutance values of 100 mA/mm and 40 mS/mm, respectively. Higher values have been obtained on higher quality samples by Russian Academy of Sciences, with an I_{DSmax} of 120 mA/mm, stable up to a V_{DS} = -80 V (corresponding to an applied electric field E_A = 2 MV/cm) and a maximum transconductance exceeding 70 mS/mm. It is worth to notice as all devices fabricated in this thesis are not affected by self-heating effect.

RF small signal performances of fabricated FETs have been investigated for both self-aligned and standard devices fabricated on Element Six TM180 diamond plates. Established technology allows the fabrication of transistors with operation frequencies

always in the X and C band of the radio spectrum, even if based on low quality substrates.

Self-aligned 200 nm gate length FETs fabricated on TM180 achieved a maximum oscillation frequency f_{MAX} = 15 GHz and a current gain cut-off frequency f_T = 6 GHz resulting in a power output at 1 GHz of 800 mW/mm that is, up to now, the best result in literature for polycrystalline diamond based transistors. From S-parameters analysis, it has been possible to extract a FET small signal model.

Best results in terms of operation frequencies have been obtained, also in this case, for single crystal and polycrystalline diamond plates supplied by Russian Academy of Sciences. Single crystal plate achieved a f_{MAX} = 27 GHz and a f_T = 14 GHz when V_{DS} = -15 V and V_{GS} = -0.2 V and polycrystalline diamond exceed 30 GHz for maximum oscillation frequency while 9 GHz have been achieved for f_T. Completely satisfying reasons for better performances, in terms of f_{MAX}, obtained for polycrystalline diamond have not been found, probably such a trend is due to a sort of mobility increase owing to grain boundaries and bulk interface (bulk mobility in diamond is 1600 cm^2/Vs).

Results of this thesis have pointed out the supremacy of the self-aligned gate structure and the development of an RF optimized layout specifically for diamond results in a DC characteristics improvement and a f_{MAX}/f_T ratio reduction that will lead to better RF performances. Quality of substrate clearly influence the hydrogen termination and so, in terms of FETs operation.

Introduction

Wide band gap materials are semiconductors with band gaps greater than 1.7 eV. The magnitude of the coulomb potential, the size of atoms and electro-negativities determine the band gap. Materials with small atoms and strong, electro-negative atomic bonds are associated with wide band gaps. Smaller lattice spacing results in a higher perturbing potential of neighbors. Elements in the right top part of periodic table are more likely to be wide band gap materials. There are many III-V and II-VI compound semiconductors with high band gaps. The only high band gap materials in group IV are diamond and silicon carbide (SiC). The position of the conduction band minima respect the valence band maximum in the band diagram determine whether a band gap is direct or indirect. Most wide band gap materials are associated with a direct band gap, with SiC and diamond as exceptions.

Wide band gap semiconductors show incredible physical and electronics properties that allow the use of such materials as substrate for different applications: solid state lighting could reduce the amount of energy required to provide lighting as compared with incandescent lights and they can be also used to create light throughout the visible spectrum: the next generation of DVD players (Blu-ray and HD DVD formats) uses GaN based blue lasers. Wide bandgap semiconductors can also be used in RF signal processing. Gallium Arsenide (GaAs) and Gallium Nitride (GaN) based Heterojunction Bipolar Transistors (HBTs) and High Electron Mobility Transistors (HEMTs) have shown current gain to frequencies greater than 600 GHz and power gain to frequencies greater than 1 THz. Wide bandgap materials can be used in high-temperature and power switching applications.

Wide band gap semiconductors are the actual technological answer for the three fundamental requirements of emerging communication systems: high RF output-power density at more than 1 GHz; high energy efficiency in terms of power added efficiency (PAE); higher operation voltages with energy consumption as low as it is possible. Present days well-established technology of GaAs metal-semiconductor field electric transistors (MESFETs) largely used in base stations and radars offers about 1 W/mm for output-power density with a not negligible energy consumption. Groundbreaking technology development of GaN seems to be the real step beyond for devices working in extreme conditions in terms of communication satellites. However, the extreme substrate cost and frailty added to the pestering self-heating effects shown by GaN

based devices, foster the research of alternative materials for applications in the same areas.

Diamond is the widest band gap semiconductor (5.5 eV) and shows several physical properties that make it interesting for microwaves electronics. Very high breakdown electric field (10^7 V/cm), high carriers saturation velocity (10^7 cm/s) and mobility are advantages for high power applications.

Electrical conductivity of diamond as-grown is quite low. In 1980s, first diamond based active devices had been fabricated with heavy boron and phosphorous ion implantation in order to induce conductive channels, but it was very expensive and inaccurate because of diamond very tight crystal lattice. In 1989, the conductivity of hydrogen terminated diamond layers have been discovered; in this structure, diamond surface behaves as a hole conductive channel without the addiction of extrinsic doping impurities and such a channel can be used for fabrication of field effect transistors.

This PhD thesis has been focused on fabrication and characterization of metal-semiconductor field effect transistors (MESFETs) based on hydrogen terminated single crystal and polycrystalline diamond.

Chapter 1

In this chapter, author would like to introduce diamond as an electronic material. The great physical, optical and electronic properties of diamond will be reviewed in order to understand how the material quality is important for electronic device applications. A brief review of the growth techniques will be followed by a deep speculation on doping techniques, especially on surface conductivity induced by hydrogen termination.

Theory of ohmic and Schottky contacts will be explained with a specific attention to the age-old issues related to diamond contacts fabrication. A model of metal-semiconductor field effect transistor will be proposed for results that will be presented in this thesis and conclusively a review of active devices based on diamond will be provided. Greatest as well as disputed results will be discussed in order to supply a self-consistent state-of-art of diamond based transistors.

1. Synthetic Diamond History

Historically, earlier single crystals were probably mined in India and mainly used as cutting tools rather than as jewels. Today diamonds are mined in Africa, Russia, Brazil and Australia. The colors of natural diamond crystals can be quite different, from white-transparent to pink, yellow, green and blue depending on the impurities present in the crystal. They are polished to jewels and are used for cutting tool applications.

In the 18th century several scientists realized that diamond is a high-pressure, high-temperature modification of carbon. Probably the first successful diamond synthesis was performed by Scot J. B. Hannay in 1880 [1,2] and by the 1906 Nobel Prize F. F. H.

Moissan in 1893[3]. Hannay used a mixture of hydrocarbonates, lithium and oil which was heated up in iron pipes until it blasted. The reaction products were quite similar to diamond with a density of 3,5 g/cm consisting of 97% carbon. Moissan's method involved heating charcoal at up to 3500 °C with iron inside a carbon crucible in his newly developed electric arc furnace, in which an electric arc was struck between carbon rods inside blocks of lime: The molten iron was then rapidly cooled by immersion in water. The contraction generated by the cooling supposedly produced the high pressure required to transform graphite into diamond .

In 1941, an agreement was made between the General Electric (GE), Norton and Carborundum companies to further develop diamond synthesis: they achieved the first commercially successful synthesis of diamond on December 16, 1954, and this was announced on February 15, 1955[4]. The breakthrough was using a "belt" press, which was capable of producing pressures above 10 GPa and temperatures above 2000 °C. The "belt" press (see below) used a pyrophyllite container in which graphite was dissolved within molten nickel, cobalt or iron. Those metals acted as a "solvent-catalyst", which both dissolved carbon and accelerated its conversion into diamond. He was the first person to grow a synthetic diamond with a reproducible, verifiable and well-documented process[5,6].

However, an independent successfully diamond synthesis was achieved on February 16, 1953 in Stockholm by the ASEA (Allmänna Svenska Elektriska Aktiebolaget), one of Sweden's major electrical manufacturing companies. The results were, however, not published due to reasons of confidence.

The key process step for the production of synthetic diamond today requires the transformation of graphite into diamond at pressures of roughly 6 GPa, temperatures up to 1600°C and the use of catalysts. Up to now there exists a great industrial need for synthetic diamond. Roughly 80000 kg synthetic diamond is used every year worldwide. Greater industrial use of diamond was always limited by the small size, normally not more than a few millimetres in diameter, of natural or synthetic diamond crystals.

With the invention of the chemical vapour deposition (CVD) of diamond on various substrates this problem was solved. In the 1950s, research started in the Soviet Union and the US on the growth of diamond by pirolysis of hydrocarbon gases at the relatively low temperature of 800 °C with the CVD low-pressure process. William G. Eversole reportedly achieved vapor deposition of diamond over diamond substrate in 1953, but it was not reported until 1962[7]. Diamond film deposition was independently reproduced by Angus and coworkers in 1968[8] and by Deryagin and Fedoseev in 1968[9], 1970[10] and 1973[11]. Whereas Angus used large, expensive, single-crystal diamonds as substrates, Deryagin and Fedoseev succeeded in making diamond films on non-diamond materials (silicon and metals), which led to massive research on

inexpensive diamond coatings in the 1980s. Hydrogen is the key to growing diamond and not graphite under these conditions, Angus' early work showed. At the surface, the carbon lattice of diamond is decorated with "dangling bonds" that can potentially cross-link to reorganize the surface into more stable graphite. Capping these bonds with hydrogen prevents graphite formation and generates reactive surface sites for attachment of carbon radicals.

In 1992 the first heteroepitaxial growth of diamond films on (001) silicon was reported[12]. However, these heteroepitaxial films are essentially polycrystalline with pronounced grain boundaries. The stunning achievements of the Japanese researchers rekindled commercial interest in CVD diamond, particularly in the USA, where, by the end of the 1980s more than 30 companies were investigating the possibilities of this new diamond material and how it could be applied to their businesses. Up to now several research groups worldwide are investigating the improvement of growth methods and the improvement of the thermal, electronic and mechanical properties of these films, with a special focus on industrial applications. The magnitude of research on the properties and growth of CVD diamond is large and author would like to cite the works of V. G. Ralchenko at the Russian Academy of Science[13,14,15].

In 2002 a key publication by Element Six Ltd., formerly known as De Beers Industrial Diamonds, on CVD diamond's electronics properties was published in Science[16]. This work, combined with increased commercial availability of the material, has rekindled major interest in CVD diamond.

2. Diamond properties

Table 1 is a synthesis of diamond mechanical, optical, thermal and electronic properties:

Table 1 - Properties of CVD Diamond

Property	*Value*	*Units*
Hardness	1×10^4	kg/mm^2
Strength, tensile	>1.2	Gpa
Strength, compressive	>110	Gpa
Fracture Strength	400-800	MPa at <1 mm thickness
Sound Velocity	1.8×10^4	m/sec
Density	3.52	g/cm^3
Young's modulus	1200	Gpa
Poisson's ratio	0.2	dimensionless
Atomic density	1.77×10^{23}	$atoms/cm^3$
Lattice Constant	3.567	Å
Thermal Expansion coefficient	1.1-5.0 (300-1300K)	ppm/K

Thermal Conductivity	10-20	W/cmK
Thermal shock parameter	3×10^7	W/m
Coefficient of friction	0.05 (dry)	dimensionless
Derbye temperature	2200	K
Melting point	4100	K
Optical index of refraction	2.41 (591 nm)	dimensionless
Optical Transmissivity range	225 to far IR	nm
Emissivity	0.02-0.03	At 10 μm
Optical absorption coefficient	0.05-0.3	At 10 μm
Absorption edge	0.20	μm
Loss tangent at 40 Hz	0.0006	dimensionless
Loss tangent at 140 GHz	$<10^{-5}$	dimensionless
Dielectric constant	5.7	dimensionless
Dielectric strength	1×10^7	V/cm
Electron mobility	2200	cm^2/Vs
Hole mobility	1600	cm^2/Vs
Electron saturation velocity	2.7×10^7	cm/s
Hole saturation velocity	1×10^7	cm/s
Work function	small and negative	on [111] surface
Bandgap	5.45-5.7	eV
Resistivity	10^{13}-10^{16}	Ωcm

Definitions:

- ✓ **Hardness** is the measure of how resistant solid matter is to various kinds of permanent shape change when a force is applied.
- ✓ **Tensile strength** is the maximum stress that a material can withstand before necking, which is when the specimen's cross-section starts to significantly contract.
- ✓ **Compressive strength** is the capacity of a material to withstand axially directed pushing forces. When the limit of compressive strength is reached, materials are crushed.
- ✓ **Fracture strength** is a mechanical parameter for brittle material, is defined as a material's ability to resist deformation under load.
- ✓ **Sound velocity** is the distance traveled during a unit of time by a sound wave propagating through material.
- ✓ **Density** of a material is defined as its mass per unit volume.
- ✓ **Young's modulus**, also known as the tensile modulus, is a measure of the stiffness of an isotropic elastic material. It is defined as the ratio of the

uniaxial stress over the uniaxial strain in the range of stress in which Hooke's Law holds.

- ✓ **Poisson's ratio** is the ratio, when a sample object is stretched, of the contraction or transverse strain (perpendicular to the applied load), to the extension or axial strain (in the direction of the applied load).
- ✓ **Atomic density** refers to the number of atoms per unit volume.
- ✓ **Lattice constant** refers to the constant distance between unit cells in a crystal lattice.
- ✓ **Coefficient of thermal expansion** refers to the degree of expansion divided by the change in temperature.
- ✓ **Thermal conductivity** is the property of a material reflecting its ability to conduct heat.
- ✓ **Thermal shock** is the name given to cracking as a result of rapid temperature change.
- ✓ **Coefficient of friction** is a dimensionless scalar value which describes the ratio of the force of friction between two bodies and the force pressing them together.
- ✓ **Debye temperature** is, in Debye theory, the temperature of a crystal's highest normal mode of vibration, i.e., the highest temperature that can be achieved due to a single normal vibration.
- ✓ **Melting point** of a solid is the temperature at which the vapor pressure of the solid and the liquid are equal. At the melting point the solid and liquid phase exist in equilibrium.
- ✓ **Index of refraction** of a substance is a measure of the speed of light in that substance. It is expressed as a ratio of the speed of light in vacuum relative to that in the considered medium. The velocity at which light travels in vacuum is a physical constant, and the fastest speed at which energy or information can be transferred.
- ✓ **Transmittivity** is the fraction of incident light at a specified wavelength that passes through a sample.
- ✓ **Emissivity** of a material is the relative ability of its surface to emit energy by radiation. It is the ratio of energy radiated by a particular material to energy radiated by a black body at the same temperature. It is a measure of a material's ability to radiate absorbed energy.
- ✓ **Absorption coefficient** is a quantity that characterizes how easily a material or medium can be penetrated by a beam of light, sound, particles, or other energy or matter.
- ✓ **Absorption edge** is a sharp discontinuity in the absorption spectrum of X-rays by an element that occurs when the energy of the photon corresponds to the energy of a shell of the atom.

- ✓ **Loss tangent** is a parameter of a dielectric material that quantifies its inherent dissipation of electromagnetic energy. The term refers to the tangent of the angle in a complex plane between the resistive (lossy) component of an electromagnetic field and its reactive (lossless) component.
- ✓ **Dielectric Constant** of a material under given conditions reflects the extent to which it concentrates electrostatic lines of flux. It is the ratio of the amount of electrical energy stored in a material by an applied voltage, relative to that stored in a vacuum; similarly, it is the ratio of the capacitance of a capacitor using that material as a dielectric, compared to a similar capacitor which has a vacuum as its dielectric.
- ✓ **Dielectric strength** is the maximum electric stress the dielectric material can withstand without *breakdown (breakdown electric field).*
- ✓ **Mobility** relates the drift velocity of electrons in relation to an applied electric field across a material.
- ✓ **Saturation velocity** is the maximum velocity a charge carrier in a semiconductor, generally an electron, attains in the presence of very high electric fields.
- ✓ **Work function** is the minimum energy (usually measured in electron volts) needed to remove an electron from a solid to a point immediately outside the solid surface (or energy needed to move an electron from the Fermi level into vacuum).
- ✓ **Bandgap** is an energy range in a solid where no electron states can exist.
- ✓ **Resistivity** is a measure of how strongly a material opposes the flow of electric current.

2.1. Mechanical and wear properties

Diamond is the hardest natural material known and its strength is obviously related to its high density of very strong bonds. An analysis based on elastic modulus, fracture surface energy and nearest neighbor distance gives a theoretical strength of about 100-200 GPa[17]. Diamond hardness depends on its purity, crystalline perfection and orientation: hardness is higher for flawless, pure crystals oriented to the (111) direction [18]. Combining its wear properties with low friction and high thermal conductivity makes diamond a suitable material for cutting tool applications. A lot of studies have been reported in literature [19,20,21].

2.2. Thermal Properties

The thermal conductivity of diamond is higher than any other material at room temperature, and contributes significantly to its performance in a number of applications including windows for multi-kilowatt CO_2 lasers[22], megawatt gyrotrons[23] and even cutting tools. The main heat conduction mechanism for many

materials is by electrons; high thermal conductivity is associated with high electrical conductivity. In diamond, vibrations of lattice phonons provide the main mechanism. Therefore any lattice defect acts to reduce its thermal conductivity by scattering phonons. With a sound velocity of 18 km/s[24], diamond is the material with the highest Debye temperature (2200 K), exceeding that of most other insulators by an order of magnitude. With a thermal conductivity of 20–25 W/cmK at room temperature[24], natural diamond is the material with the highest thermal conductivity, exceeding that of copper by a factor of 5. Even lower grades with thermal conductivities of 10 W/cmK exceed other competitor ceramics such as aluminium nitride by a factor of four to six.

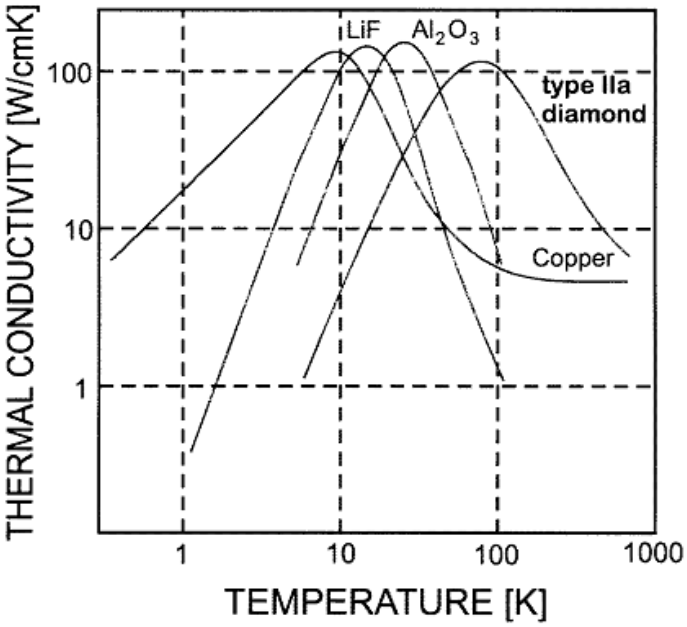


Figure 1 - Thermal conductivity of LiF, Al_2O_3, copper and type IIa natural diamond[27]

In recent years, progress in the CVD deposition techniques allowed the thermal properties of CVD diamond to become comparable to that of the best natural diamonds. Large-area CVD diamond plates with thermal conductivities around 20 W/cmK became available[25,26], increasing the demand for CVD diamond for various thermal management applications. The thermal conductivity of non-metallic crystals and copper is compared with that of diamond in figure1. For all insulators, the temperature dependence of the thermal conductivity is qualitatively similar. At low temperatures, the thermal conductivity is proportional to T^3 . It reaches its maximum at temperatures of about 1/20 of the Debye temperature and it decreases again for higher temperatures. The only difference between diamond and the other insulating materials is a shift of the maximum for the thermal conductivity to higher temperatures, thereby

leading to the highest thermal conductivity of any material at room temperature. Due to the wide bandgap of diamond (5.47 eV), even at temperatures as high as the Debye temperature, virtually all the heat is conducted by phonons[28]. The theory of heat conduction due to lattice vibrations is known as the Klemens–Callaway theory[29,30].

The phonons scattering mechanisms involved are scattering at grain boundaries, extended-defect and point-defect scattering and the intrinsic umklapp scattering (an anharmonic phonon-phonon scattering process, creating a phonon with a momentum outside the first Brillouin zone, a uniquely defined primitive cell in reciprocal space). Each of these scattering mechanisms influences the thermal conductivity in a certain temperature range. At low temperatures the thermal conductivity of CVD diamond is proportional to T^3 and the sample size.

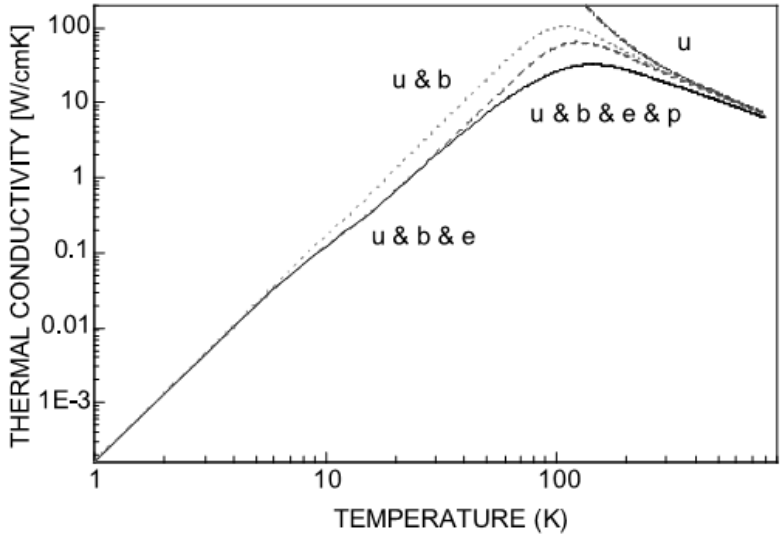


Figure 2 - Thermal conductivity of diamond according to the Klemens–Callaway theory if only umklapp scattering is present (u). The other curves are calculated with successive addition of boundary scattering (b), scattering at extended defects (e) and point defects (p), respectively[31].

The thermal resistance is dominated by grain boundary scattering. At medium temperatures, extended-defect and point-defect scattering contribute to the thermal resistance and affect the maximum of the thermal conductivity. At high temperatures, intrinsic umklapp scattering is the main source of thermal resistance. The characterization of CVD diamond films and plates with respect to their thermal conductivity has been the subject of extended scientific investigation in the past few years. A multitude of characterization techniques were developed, each one having certain advantages and drawbacks. Figure 3 reports a comparison of different diamond quality grades (by Element Six Ltd.) in the room temperature range.

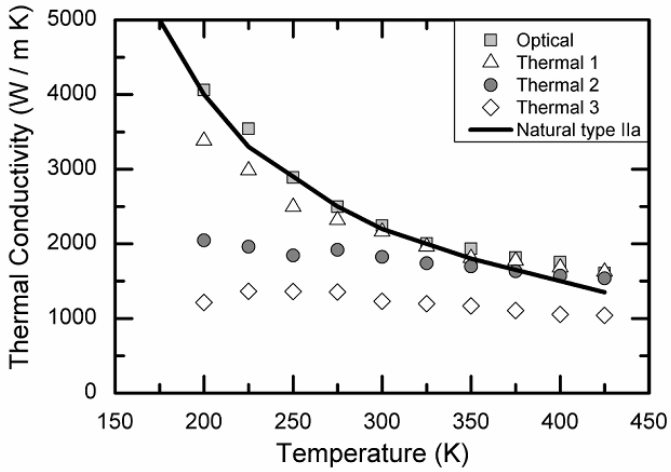


Figure 3 - Thermal conductivity versus temperature for natural type IIa and CVD polycrystalline diamond. Thermal 1, 2 and 3 are representative of grades with nominal room temperature conductivities of 18, 15 and 10 W/cmK respectively.

2.3. Optical Properties

Diamond is unique among all materials in its optical properties. Its transparency ranges from the UV just beyond the bandgap edge at 220 nm (5.5 eV) all the way to the far IR and even to microwave and radio frequencies. Such transmission properties make diamond ideally suitable for various optical applications. The progress made in producing CVD diamond with an optical quality comparable to the best natural diamonds has stimulated efforts to exploit CVD diamond as well for solar blind UV detection[32,33] as for IR optics, especially in the region around 10 µm. The absorption coefficient for intrinsic diamond from the UV to long-wavelength IR is illustrated in figure 4.

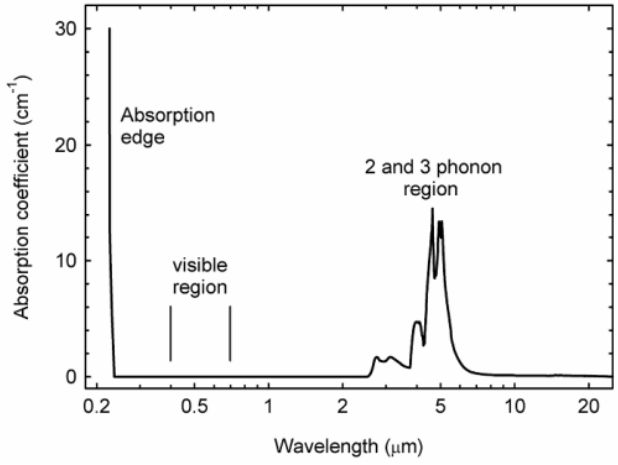


Figure 4 – Absorption[34] spectrum (b, right) of CVD diamond from the UV to IR

The maximum absorption coefficient in this spectral range amounts to 14 cm^{-1} at 2158 cm^{-1}[36]. Wide spectral transparency can be seen (Fig. 5), even extending to 500 µm[37] except for regions of absorption in the infra-red between around 2.5 to 6.5 µm (4000 to 1500 cm^{-1}), and below the bandgap at around 226 nm[38]. The spectra of both natural and CVD diamond exhibit a multitude of absorption lines and bands which can be attributed to impurities and defects.

The most important impurity is nitrogen which forms various optical centres as single substitutional nitrogen and multi-atom aggregates which are responsible for the yellow or green colour of many natural diamonds. Substitutional boron leads to a blue coloration. Further optical centres can be produced by irradiation. The absorption in the infra-red is due to two-phonon and three-phonon processes. Two-phonon (1332–2664 cm^{-1}) and three-phonon (2665–3994 cm^{-1}) transitions are responsible for the only intrinsic absorption. These are temperature dependent and the absorption is successfully described by the model developed by Piccirillo *et al*[39]. Apart from the intrinsic absorption, the most frequently observed extrinsic absorption bands of CVD diamond are the CH-stretch vibrations between 2700 and 3000 cm^{-1} [35,40]. Its strength can be used to estimate the hydrogen content[41]. However, these absorption bands are negligible in high-quality CVD diamond films.

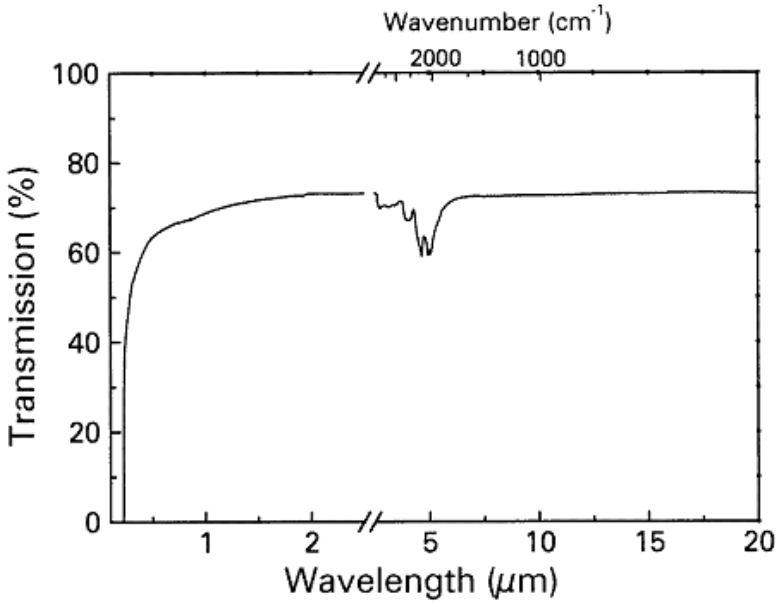


Figure 5 – Transmission[35] spectrum (b, right) of CVD diamond from the UV to IR

Other IR transmitting materials, such as ZnS and ZnSe owe their transparency to heavy atoms and weak bonds, resulting in low phonon energies and thus a cut-off frequency in the far IR. Diamond with its low mass and rigid lattice possesses the

highest fundamental phonon (absorption) frequency of any material, with the single phonon mode centred at 7.5 µm (1332.5 cm^{-1}). While the lattice remains defect free, and thus symmetric, absorption at this frequency is forbidden. Recent measurements of absorption by calorimetry at 1064 nm[42] yield values of 0.003 to 0.07 cm^{-1} for single crystal CVD diamond, while the absorption coefficient at 10.6 µm has been found to be between 0.02 and 0.05 cm-1 on both single and polycrystalline samples[43]. Polycrystalline diamond causes significant Rayleigh scattering losses at wavelengths below approximately 1 µm[44].

2.4. Electronic Properties

Diamond is a wide bandgap semiconductor with an indirect gap of about 5.47 eV. One of the benefits of this is that diamond can support high electric fields before breakdown. Experiments on high purity CVD diamond have reported high mobility values and long lifetimes for electrons and holes. Combined with the high thermal conductivity, diamond can be the preferred material for a number of demanding electronic applications. The concentration of electrons in the conduction band (n) of an intrinsic semiconductor, assuming a mid-bandgap Fermi level, is approximately $n=N_C \times exp[E_g/(2k_BT)]$ where N_c is the effective density of states in the conduction band, E_g is the energy gap, k_B is Boltzmann's constant and T is temperature. At room temperature $N_c \sim 2 \times 10^{19}$ cm^{-3}[45] and n is very much less than one electron per km^3.

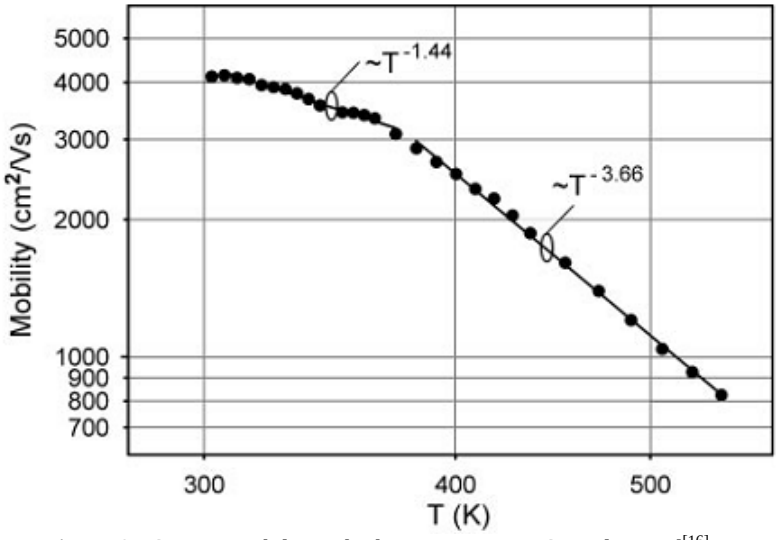


Figure 6 - Carriers mobility in high purity intrinsic CVD diamond[16].

High carrier mobility in high purity intrinsic CVD diamond (Fig. 5) was first reported in 2002[16]. In the high carrier injection regime (when Q>CV, where Q is the

charge, C is the capacitance and V is the voltage), the mobility decreases with a $T^{-3/2}$ dependence, indicative of acoustic phonon scattering as limiting mechanism up to temperatures ~400 K. At higher temperatures, it shows a $\sim T^{-3.7}$ dependence consistent with measurements on natural diamond. At room temperature a hole mobility of 3800 (±400) cm^2/Vs was reported.

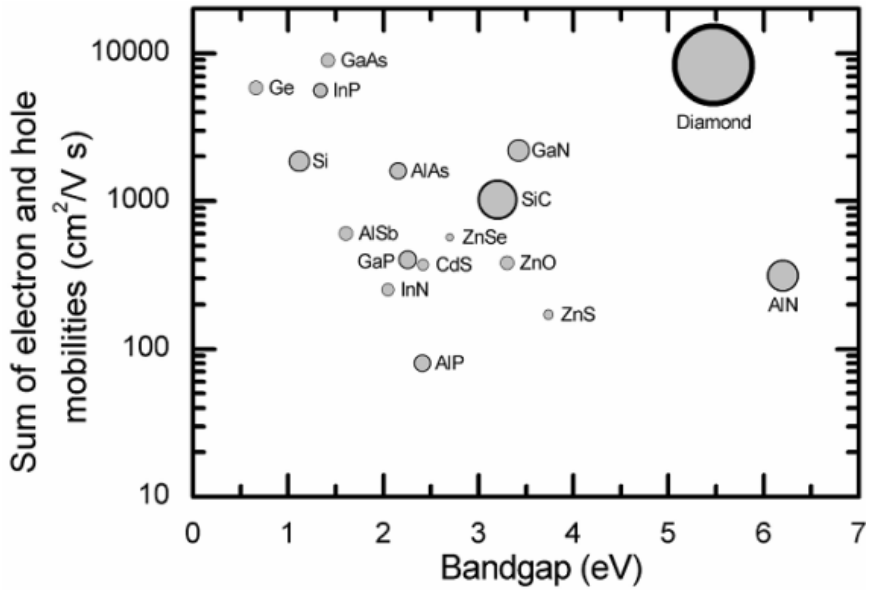


Figure 7 - Combined electron and hole mobility (room temperature) for electronics materials. Mobility circles have an area proportional to the thermal conductivity

Even at 400 K the mobility still exceeds 2000 cm^2/Vs. Scientific community accepts undoped diamond hole and electron mobility as 1900 and 2200 cm^2/Vs respectively, in agreement with theoretical results[46,47]. The combined electron and hole room temperature mobility for a number of electronic materials is plotted against bandgap in Figure 6.

Diamond's unique position is evident, especially when thermal conductivity is considered (the circle in the plot). Diamond's relative low dielectric constant and large bandgap combine to predict a widely quoted breakdown field of 10^7 V/cm[48]. Breakdown voltage measurements have been performed for diamond based Schottky diodes. For planar diode structures, a breakdown voltage of 6 kV has been attained using a wide contact spacingresulting in a 50V/µm for breakdown electric field[49], a 146 V/µm breakdown field for micron-scale separation devices[50] and up to 2kV/µm for a microstrips diode structure[51]. In vertical device structures, 2.5 kV breakdown has been reported for 18 µm thickness of intrinsic diamond (140 V/µm) [52]. Others have also achieved breakdown fields of this magnitude[53,54].

3. Diamond Growth

The development of diamond growth using CVD techniques started in the 1950s, when Union Carbide laboratories achieved the first overgrowth of diamond from the gas phase on the surface of diamond powder particles[7], probably before the first successful high-pressure, high-temperature synthesis (HPHT) of diamond obtained at the General Electric Company[5]. The results were only of scientific interest and the field was abandoned for more than a decade until Russian scientists found that the growth of diamond by CVD methods could be widely enhanced in the presence of a superequilibrium concentration of atomic hydrogen[8,9,10,11]. Although this achievement can probably be dated back between the late 1960s and the early 1970s, the first two techniques described in detail were the hot-filament CVD[55] and the microwave-plasma CVD method (MWCVD)[56]. Although strong efforts were made to develop a multitude of diamond CVD processes, the HFCVD and the MWCVD processes continued to be the techniques most used: the HFCVD based on its simplicity and up-scaling potential and the MWCVD as a result of the outstanding quality of the CVD wafers prepared with this technique and also its up-scaling potential because of the increasing availability of high-power microwave generators.

3.1. HTHP: thermodynamically stable synthesis

At room temperature and pressure, graphite is the stable allotrope of carbon while diamond is a metastable allotrope. The genesis of natural diamond is believed to occur at depths of around 200 km, corresponding to pressures and temperatures of 7-8 GPa and 1400-1600°C [57,58]. This is in the region of the carbon phase diagram where diamond is thermodynamically stable (Fig. 8).

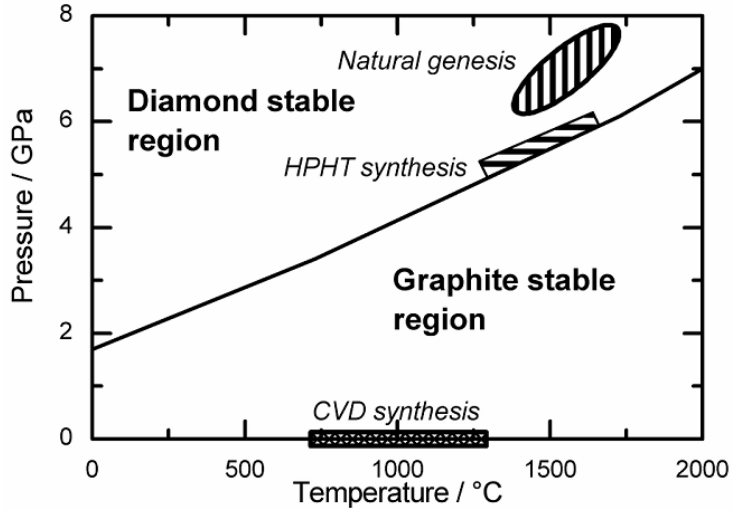


Figure 8 – Carbon Phase Diagram indicating main regions of pressure-temperature space

Natural diamonds have grown in a variety of uncontrolled environments and their composition and growth habits vary significantly: types I and II are the main divisions on the basis of optical absorption[59]:

Table 2

Property	**Type IIa SC CVD**	**Type Ib HPHT**	**Type Ia** *natural*	**Type IIa** *natural*
Nitrogen (ppm)	<1	150-200	200-3000	<10
Dominant Nitrogen form	Single substitutional	Single substitutional	Aggregates	Aggregates or substitutional
Colour	Colourless	Yellow	Colourless – yellow to brown	Brown – colourless
Thermal Cond. (W/cmK) @300K	18-22	8-12	4-12	18-22
Dislocations	$<10^4$ cm^{-2}	10^4-10^6 cm^{-2}	$<10^6$ cm^{-2}	10^8-10^9 cm^{-2}

The first industrialized method of synthesising diamond was the HPHT[5]. In the HPHT method, there are three main press designs used to supply the pressure and temperature necessary to produce synthetic diamond: the belt press, the cubic press and the split-sphere (BARS) press:

- ✓ In the *belt press* the upper and lower anvils supply the pressure load to a cylindrical inner cell. This internal pressure is confined radially by a belt of pre-stressed steel bands.
- ✓ The *cubic press* has six anvils which provide pressure simultaneously onto all faces of a cube-shaped volume. A cubic press is typically smaller than a belt press and can more rapidly achieve the pressure and temperature necessary to create synthetic diamond.
- ✓ The *BARS* apparatus is the most compact, efficient, and economical of all the diamond-producing presses. In the centre of device, there is a ceramic cylindrical "synthesis capsule". The cell is placed into a cube of pressure-transmitting material which is pressed by inner anvils made from cemented carbide. The outer octahedral cavity is pressed by 8 steel outer anvils. After mounting, the whole assembly is locked in a disc-type barrel with a diameter about 1 meter. The barrel is filled with oil, which pressurizes upon heating, and the oil pressure is transferred to the central cell. The synthesis capsule is heated up by a coaxial graphite heater and the temperature is measured with a thermocouple.

All methods use a core reaction cell in which the diamonds are grown. This reaction cell is submitted to the extreme temperatures and pressures needed. Inside the reaction

cell a carbon source is placed, as well as some seed crystals. One of the most important elements in the process is the presence of a metal solvent or 'flux', which acts as a solvent and transport material of the carbon source to the seed. This solvent can be Fe, Co, Ni or mixture of the three. This flux makes it possible to synthesize a diamond at much lower temperatures and pressures than necessary for direct conversion of graphite into diamond. The exact composition of the flux strongly influences the properties of the synthetic diamond. A slow, well-controlled growth is essential for growing high quality diamonds. Only a few minutes are needed to convert graphite into powder sized diamond, but it takes about three days to crystallize rough gem-quality stone. The HPHT growth process offers a significant degree of control over the quality and geometry of diamond obtained[60,61]. Most HPHT diamond is small grains of type Ib for use in grinding and other abrasive applications. Longer, controlled growth periods enable production of single crystal Ib stones with dimensions routinely up to 8 mm. Addition of selected getter mixtures to the capsule (for example Ti, Al, Zr) removes nitrogen atoms and enables growth of type IIa diamond[62,63]: nitrogen present is preferentially bound to the getter, rather than being incorporated in the diamond lattice. Extraordinary degrees of lattice perfection have been achieved in processes similar to this, where the slow, well-controlled growth has generated areas of over 4×4 mm^2 with no detectable extended defects[64].

3.2. CVD: metastable synthesis

Diamond can also be synthesized in its metastable regime. Growth by Chemical Vapour Deposition (CVD) was first performed in 1953[7] and work leading to industrialized processes was reported in the 1980s[55,56,65]. Being in the region where diamond is metastable compared to graphite, synthesis of diamond under CVD conditions is driven by kinetics and not by thermodynamics. Diamond synthesis by CVD is normally performed using a small fraction of carbon (typically <5%) in an excess of hydrogen[14]. If molecular hydrogen is heated to temperatures in excess of 2000K, there is a significant dissociation to atomic hydrogen. The heating techniques can be various (arc-jet[66,67], hot filament, microwave plasma or DC arc[68,69] or even by using an oxy-acetylene flame[70]). In the presence of a suitable substrate material (Si, Mo, W, Ti, diamond), diamond can be deposited. The majority of the impurities in the gas mixture come from the source gases. The low concentrations of impurities in nowadays available source gases, have contributed to the growth of diamond with exceptionally high purity[52,71,72]. Another significant aspect of CVD diamond growth is that large areas of diamond can be obtained. While very few natural, single crystal gem diamonds have dimensions exceeding 15 mm, freestanding polycrystalline diamond wafers are routinely manufactured in discs exceeding 100 mm[69,73]: four inches polycrystalline diamond is currently commercially available.

3.2.1. Forms of CVD Diamond

Solid materials can be divided into three broad classes - amorphous, polycrystalline and single crystal. Amorphous materials are characterized by a lack of long range order (glasses, plastics and diamond-like carbons DLCs). Polycrystalline materials are also common, including most metals, metal alloys, and igneous rocks: these are composed of small single crystals (grains) bound tightly together by a thin disordered interface. Macroscopic single crystals do exist, but are much less common: the most widely used macroscopic single crystal of our era is silicon.

Diamond grown by CVD can fall into two of these categories: polycrystalline and single crystal. Single crystal diamond is formed by homoepitaxial growth, where the seed, or substrate, is a single crystal diamond (natural, HPHT, or CVD). Polycrystalline diamond is typically formed whenever growth occurs on a non-diamond substrate. Unlike many other polycrystalline materials, the grain structure of polycrystalline diamond has a non-uniform composition. The grains show a preferred direction, and vary dramatically in size from one side of a polycrystalline diamond wafer to the other. This is due to the growth process. A high density of nucleation sites is initially formed on the substrate. Each of these sites grows, but grains with favoured facets and orientations grow preferentially with respect to their less favoured neighbours. This growth competition increases the size of grains to around 10% of the layer thickness; each surviving grain can be traced back to a single nucleation point at the substrate surface. In addition to homoepitaxial growth, significant efforts have gone into single crystal diamond growth by heteroepitaxy. The non-diamond substrate is chosen so that nucleating grains are crystallographically aligned, and strain and lattice mismatch are minimized. Careful control of the growth conditions is required to ensure that the grains remain aligned in both the growth plane and growth direction and can coalesce. As with heteroepitaxial growth of other materials, extended defects propagate from the original grain boundaries but, unlike them, diamond cannot be readily annealed to create a low defect single crystal.

3.2.2. Hot Filament CVD

In the case of the Hot Filament CVD (HFCVD) technique, atomic hydrogen is produced by a heated refractory metal wire (for example, W) in the immediate vicinity of the substrate. The elementary principle was first published by Matsumoto in 1982[55] and is depicted in figure 9: practically, all contemporary HFCVD processes for diamond deposition are derived from this publication. The Japanese scientists used a coiled tungsten filament mounted near the substrate and electrically heated to about 2000°C.

The temperature in the deposition chamber was measured by a thermocouple in contact with the silica substrate holder and amounted to between 700 and 1000° C. The process gas was composed of about 1% methane diluted in hydrogen with a total flow rate of 10–100 cm^3/min.

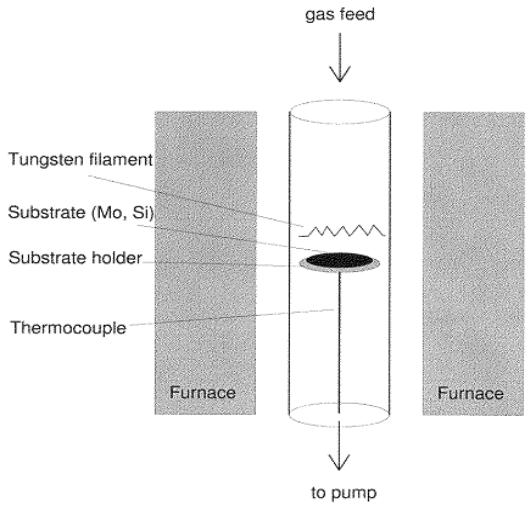


Figure 9 - Schematic sketch of the hot-filament deposition chamber as used by Matsumoto[55]

Diamond was formed at chamber pressures between 1 and 10 kPa. The samples were characterized in order to provide evidence that diamond particles or films had been formed and Scanning Electron Micrographs (SEMs) showed the cubo-octahedral morphology typical for CVD diamond while the Raman peak at 1334.5 cm^{-1} was very close to the position reported for single-crystal diamonds. Under the conditions quoted above, linear growth rates of roughly 1 µm/h were achieved, a growth velocity which can still be considered as typical for HFCVD processes. Since the fundamental Japanese work, numerous investigations have been performed in order to clarify which and how parameters influence diamond growth rates and film qualities. The most important factors[74,75] can be summarized in:

a) In order to form a closed film as fast as possible, a high nucleation density has to be achieved. It can be realized by a proper substrate pre-treatment (e.g. ultrasonic irradiation in a diamond powder suspension)
b) Maximum growth rates are achieved for temperatures of about 850° C
c) The growth rate increases with the filament temperature: higher growth rates are achieved at lower filament–substrate distances
d) The growth rate increases with increasing methane concentration: the non-diamond carbon components will also increase
e) As a function of gas pressure, the growth rate has a maximum at about 10 kPa.

One inevitable effect of applying the HFCVD technique is the incorporation of filament impurities in the diamond film. A lot of studies were performed on the three most typical filament materials: tungsten, tantalum and rhenium[76,77]. In contrast to tungsten and tantalum, rhenium does not form a carbide, but carbon diffuses rhenium rapidly. Nevertheless, rhenium remains ductile and, therefore, has a longer lifetime than the brittle tungsten and tantalum carbides. Although rhenium is more expensive, it might be the appropriate filament material if lifetime aspects are important and the impurity incorporation originating from the filaments can be ignored. On the other hand, if impurity incorporation has to be minimized, tantalum and tungsten filaments are more appropriate because the pre-carburization of the filaments reduces the impurity concentration in the chamber. The impurity concentration can be further reduced by applying low filament temperatures and/or increased methane concentrations. However, the first has a negative effect on the growth rate and the second deteriorates the phase purity of the deposited diamond. Since the Japanese work, many scientific groups have investigated and optimized the HFCVD process in order to increase the depostion rate and to deposit diamond on larger areas[78]. HFCVD diamond films generally have a lower purity than high-quality plasma CVD films so that the potential of HFCVD diamond films is limited with regard to optical and electronic applications. However, the HFCVD technique is superior to the MWCVD technique concerning the deposition on complex-shaped surfaces. Because of its higher flexibility and its up-scaling potential it is the technique of choice for the deposition on cutting tools and wear parts.

3.2.3. Microwave CVD

Along with HFCVD, it was microwave-plasma enhanced CVD (MPECVD) which moved diamond deposition from its niche of scientific curiosity into the area of industrially applicable technologies. It was first demonstrated in 1982 at NIRIM (National Institute for Research in Inorganic Materials) in Japan[56]. Since then this technique has found a lot of success because of its simplicity, flexibility, and the early commercial availability of reactors from New Japan Radio Corporation based on the NIRIM work. Also, great progress was made in the up-scaling of microwave reactors in order to enlarge the deposition area and to increase growth rates. Generally, in a microwave-plasma diamond deposition reactor, process gases are introduced into a reactor chamber which contains the substrate to be coated. Microwave power is then coupled into the chamber in order to create a discharge. The chamber is an integral part of an electromagnetic cavity and consequently its geometry has a strong influence on the location and the extent of the microwave discharge. It is of great importance to create a stable plasma which can be reproducibly controlled. Typically, the substrate to be coated with diamond is immersed into the plasma within this cavity. The

microwaves couple energy into the electrons which in turn transfer their energy to the gas through collisions[79,80]. As a result of these collisions the process gas is heated and chemical reactions in the gas phase lead to the formation of diamond precursors which impinge on the substrate surface. If the surface conditions are carefully adjusted, diamond starts growing on the substrate. The microwave plasmas are excited by 915 MHz (32.8 cm) and 2.45 GHz (12.2 cm). The choice of these very specific frequencies is mainly due to the availability of components that comply with national regulations. Undoubtedly, Microwave Plasma Enhanced CVD (MPECVD) is a very flexible technique in terms of the variety of gas precursors which can be used for diamond growth. In contrast to the HFCVD, where the admixture of aggressive reactant gases like oxygen or halogens would destroy the filaments, almost every conceivable gas mixture can be used. The use of liquid precursors is also common[70]. Obviously, not every possible gas combination will lead to successful diamond growth. Since the start of CVD diamond growth in the early 1980s, a lot of topics were dicussed: it should be mentioned that besides the great importance of the correct gas composition, it is also necessary to choose the correct surface temperature and chamber pressure. Other aspects such as surface material and surface pretreatment are also required for a successful growth. The efforts to commercialize CVD diamond products have also triggered the development of microwave CVD reactors which distinguish themselves by increasing power, increasing size and increasing diamond deposition rate. This evolution will likely continue as new commercial applications of diamond appear in the marketplace. Historically, the evolution started with the NIRIM reactor in 1982[56] and went on with the development of the bell jar reactor by Bachmann[70] at ASTeX (Applied Science and Technology) in 1987.

✓ *The NIRIM tubular reactor*

The microwave-plasma reactor developed at NIRIM was very popular in the early 1980s because of its simplicity. A quartz discharge tube is inserted through the broad side of a fundamental mode rectangular waveguide appropriate for the propagation of microwaves at 2.45 GHz. The TE_{10} mode (the dominant mode of a rectangular waveguide with inside width larger than inside height: it has the lowest attenuation of all modes) which propagates in this waveguide is parallel to the short dimension of the guide (y-direction) and varies sinusoidally along the broad length of the guide (x-direction). Along the propagation direction and beyond the discharge tube location, the waveguide is normally terminated by a sliding short which can be adjusted to maintain the plasma location in the middle of the discharge tube. The choice of the position of the short is such that a maximum of the microwave electric field is obtained at the plasma location. Furthermore, a tuner is placed between the microwave source and the discharge tube to ensure that all the power is absorbed in the plasma load. The

substrate to be coated is introduced from the bottom of the discharge tube using a dielectric rod to prevent microwave leakage to the outside. Although this reactor design has become very popular among scientists, it has several disadvantages which prevented the use of this reactor type for commercial applications:

a) The deposition area is only 1–2 cm since the plasma size is limited by the presence of the nearby walls and the microwave wavelength
b) The power that can be coupled into this configuration and the plasma operating pressure is limited by the possible destruction of the discharge tube. As a consequence, both the linear and mass deposition rates possible with this reactor are small and of the order of 0.5 mg/h
c) Plasma etching of the quartz tube often leads to contamination of the diamond deposited
d) The substrate is heated by the microwave plasma. Therefore, the substrate temperature cannot be adjusted independently of the microwave power coupled into the system.

✓ *2.45 GHz microwave reactors*

In the late 1980s, ASTeX developed a different set-up for 2.45 GHz microwave plasma CVD of diamond which would soon overcome many of the limitations of the NIRIM design. With the this ‘bell jar’ reactor, it was possible to produce diamond films of up to 7.5 cm diameter. In that set-up a silica bell jar replaces the silica tube of a NIRIM-type reactor.

Figure 10 - The silica microwave window CVD reactor developed by ASTeX

A microwave coupler picks up the 2.45 GHz radiation inside the rectangular waveguide and, via an antenna, emits it centro-symmetrically into an air-cooled

circular waveguide that contains the evacuated bell jar. The plasma is generated at the point of highest electrical field strength inside the bell jar. Its shape, size and also its stability is dependent on the deposition conditions, the plasma power, the pressure and the gas composition. If correct conditions are chosen, a ball-shaped, stable plasma is formed in the centre of the bell jar, far away from the reactor walls. Between 1988 and 1992, ASTeX improved and commercialized this reactor type, thereby replacing the bell jar by a flat silica microwave window (Fig. 10). Again, the inner chamber diameter is chosen so that only one microwave radial mode can be sustained inside the cavity at 2.45 GHz. The substrate is located on top of an inductively heated substrate stage which allows substrate temperature control independently of plasma conditions. The microwave power which could be coupled into the plasma increased up to 8 kW in 1997[14]. The ASTeX reactors overcame a lot of the limitations of the NIRIM-type reactors. Because the plasma has no contact to the reactor walls, the incorporation of impurities is greatly reduced. If operated under well-defined deposition conditions, it is possible to deposit diamond continuously and unattended for several days or even weeks and to produce diamond wafers up to 30 cm^2 areas and 1 mm thickness[14].

4. Doping Diamond

Because of its large bandgap, undoped diamond is normally electrically insulating and cannot be used as an semiconductor material. But, as other large band-gap materials, diamond can be made conductive by doping it with certain elements. Currently, boron and so-colled surface transfer doping are used to obtain a p-type conduction and phosphorus or nitrogen are typically used for n-type behavior.

4.1. In situ doping

The effects caused by incorporation of dopants or impurities in CVD diamond films during the deposition have been studied extensively in the 1990s. This was motivated by the wish to make CVD diamond conducting in order to realize electronic applications and by the more fundamental objective to study the structural effects of dopants or impurities on the growth on CVD diamond films. The most prominent impurities in diamond are boron and nitrogen. To date, only boron has been demonstrated conclusively to be an electrically active dopant in diamond. It makes diamond p-type with an activation energy of 0.37-0.38 eV above the top of the valence band. Nitrogen forms a deep donor with a level at 1.7 eV below the conduction band and is electrically inactive at room temperature. Its importance results from its strong influence on the structural properties and the growth velocity of the CVD diamond films[81]. In order to realize n-type conductivity, several other dopants such as lithium and sodium have been proposed[82], particularly CVD diamond films doped with

phosphorous which exhibit n-type conductivity with an activation energy of 0.43 eV[83].

Boron has to be admixed to the reactant gas in solid, liquid or gaseous form. The only gaseous form of boron at room temperature is B_2H_6. It has been used widely to dope CVD diamond films in the 90s[84,85,86] but because of its high toxicity, more easily handled sources in solid or liquid form have been investigated. Solid sources used for boron doping include boron powder[87] and boron trioxide (B_2O_3)[88]. Boric acid (H_3BO_3)[89], cyclic organic borinate ester (R_2BOR)[90] and trimethylborate ($B(OCH_3)_3$)[91] are successfully applied liquid sources. Such non-gaseous boron sources must be heated or dissolved in a high-pressure liquid to enhance their vapour pressure; otherwise they have also often been placed near the substrate and heated in order to diffuse them into the growth surface. The boron incorporation is dependent on the texture of the diamond film or the orientation of the single-crystal diamond. An enhanced boron incorporation one order of magnitude higher than in the <100> oriented films has been observed in <111> diamond crystals[92]. The total amount of boron incorporated into CVD diamond films can be varied over several orders of magnitude up to concentrations of about 10^{21} cm^{-3} without significant deterioration of the structural quality under appropriate deposition conditions. Normally, nitrogen and phosphorous can be simply introduced to the gaseous enviroment as N_2 or NH_3 and PH_3 respectively. However, whereas the probability for boron and phosphorus[83] incorporation can be higher than 0.1, nitrogen incorporation probability was found to be only about 5×10^{-4}, also dependent on growth direction[92].

4.2. Ex situ doping (diffusion and ion-implantation)

Ex situ doping of diamond can be performed by diffusion or ion-implantation. Diffusion of impurities in diamond requires extremely high temperatures due to the low diffusion coefficient at moderate temperatures. Successful boron doping by diffusion was first reported for the fabrication of a diamond MEtal Semiconductor Field Effect Transistor (MESFET)[93]. Other groups[94,95,96] performed experiments for boron diffusion with different techniques obtaining a diffusion coefficient of about 4×10^{-13} cm^2/s at 1000°C, resulting in a dopant concentration around $2\text{-}5\times10^{-19}$ cm^{-3}.

Ion implantation studies on diamond have been reported since 1960s[97,98]. Since then, a better understanding of defect creation and accumulation during ion implantation has emerged. This has made it possible to devise successful routes that enabled diamond to be doped p-type by boron-ion implantation whereas limited success has also been achieved for phosphorus, lithium, nitrogen and oxygen doping to generate n-type layers. Ion-implantation is the method of choice for modern microelectronics in silicon technology. However, implantation requires annealing to remove the damage and to electrically activate the implants: in this case diamond

behaves quite differently than silicon. Misleading results for diamond can be obtained due to the electrical activity of damage in diamond caused by graphitization, amorphization or point-defect agglomerates. For implantation energies from tens to hundreds of keV, the penetration of energetic ions in the diamond lattice creates mainly vacancies and interstitial carbon atoms. B-implanted CVD diamond was characterized by electron spin resonance and defect formation rate was estimated to be 36 defects per implanted ion. For doses above the spin number increasing saturation threshold, the defects concentration was estimated to be in the order of 10^{21} cm^{-3}. Once the *sp3* bonds of diamond have been broken they revert to the more stable *sp2* bonds, thus giving rise to a crystalline graphite phase. For doses below the amorphization threshold it is important to remove the implantation damage and to electrically activate the dopant. This is normally achieved by annealing. Due to the fact that the diffusion coefficients of most impurities in diamond are very low, high-temperature annealing steps are necessary. Over the years several implantation/annealing schemes have been proposed. One way is high-dose implantation above the amorphization threshold and a subsequent high-temperature anneal. The purpose is to electrically activate the 'implantation tail' and create a graphite layer at the damaged surface which can be removed by wet chemical etching. When the temperature during implantation is significantly increased the amorphozation threshold is also shifted towards higher implantation doses[99]. Furthermore, this procedure should allow an in situ anneal of the implanted area, thus reducing implantation damage. Another method is based on the assumption that the vacancies and interstitials are mobile at different temperatures[100]. The implantation scheme (Cold Implantation and Rapid thermal Annealing - CIRA) consists of two steps, a cold implantation typically at liquid nitrogen temperature and rapid anneal typically above 1000°C. Cold implantation 'freezes in' the implant and damage so that the interstials and vacancies are kept in close proximity. The high-temperature anneal is assumed to take advantage from the close proximity of the interstial and vacancies and enhances the probability of interstial–vacancy recombination.

A homogeneously boron doped layer of about 750 nm was obtained and characterized by Fontaine *et al.*[101] applying CIRA method using energies up to 0.7 MeV: such implantation leads to a dopant concentration of 4×10^{18} cm^{-3} and a p-type mobility up to 385 cm^2/Vs. During the same experiment, also phosphorus, lithium and nitrogen were successfully implanted on diamond. Even oxygen has been proposed as a n-type dopant to be implanted into diamond[102]. However, implantation techniques to introduce dopants in diamond have had limited success: diamond's metastable properties at room temperature and pressure mean that implantation creates damaged or graphitic regions; even if post-implantation annealing can remove the majority of damage, it cannot restore the diamond to a perfect lattice.

4.3. Delta doping

Recently, another technique of doping diamond has been introduced. The so-colled "δ doping" has been firstly demonstrated as a boron pulse doped buried layer to be used as a channel for diamond based transistors[103]. The idea was inspired by the δ-MESFET theory proposed by Board *et al.* in 1981[104] in order to reach the ultimate physical limit of miniaturization normal to the crystal surface by confining a high carrier density to a very thin layer.

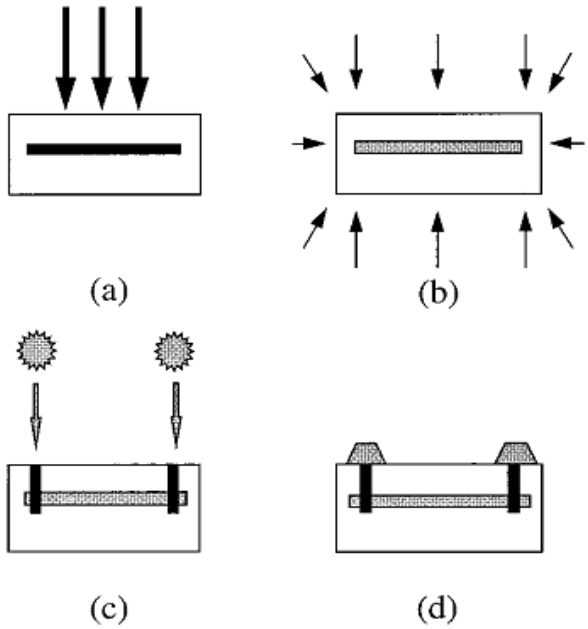


Figure 11 - Schematic of the steps required to fabricate ohmic contacts to buried doped layers. (a) MeV ion implantation; (b) thermal annealing to 950°C; (c) laser irradiation to fabricate vertical graphitic contacts; (d) silver paint baked onto the top of the contacts; between steps (c) and (d) a further high temperature anneal at 1450°C is carried out.

Figure 11 shows the technique proposed by Walker *et al.*[105] for the realization of the δ-doped layer: deeply buried boron doped layers are realized using MeV ion implantation, contact to the buried layers is accomplished using pulsed focused laser irradiation which is selectively absorbed in the implanted layer to form a graphite column up to the surface, the contacts are ohmic over a wide range of applied voltage. Implantation induced defects that are responsible for compensation of the acceptors are identified. It is found that removal of these defects requires annealing temperatures of about 1450°C, but once these defects are removed the buried B doped layer displays excellent activation of the acceptors with an activation energy of 0.372 eV. High holes mobility of 600 cm^2/Vs has been achieved with a boron concentration of about 1.3×10^{20} cm^{-3}.

Figure 12 shows a Secondary Ion Mass Spectrometry (SIMS) depth profile of the B concentration. The peak vacancy concentration produced by a dose of 1×10^{15} B/cm^2 at 77 K is 8×10^{21} vacancies/cm^3, which is just below the critical vacancy concentration for graphitization upon annealing of 1×10^{22} vacancies/cm^3. The density of defects in the cap layer is much lower than the peak value, thus allowing for very good recovery of the cap layer following annealing. It should also be noted that no diffusion of B can be observed[106]. Recently, Element Six Ltd.[52,107] developed a δ-doping process during diamond deposition, interrupting CVD with the creation of the boron doped layer by using a boron rod source in the chamber and then completing the deposition with a diamond cap layer at high temperature in order to minimize memory effects from the residual boron[108].

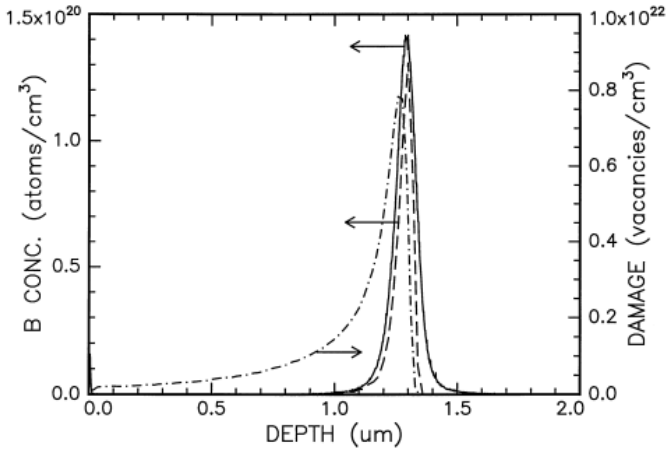


Figure 12 - Secondary ion mass spectrometry (SIMS) depth profile of the B concentration in type IIa diamond implanted with 1×1015 B/cm2 at 2 MeV (solid line). The broken lines show the calculated B and vacancy concentration produced by the implantation[105].

4.4. Surface transfer doping

Although intrinsic diamond is highly insulating, a striking surface conductivity (SC) of hydrogenated diamond was firstly discovered by Ravi and Landstrass on both natural diamond surfaces[109] and on CVD diamond films[110] after exposure to hydrogen plasma. The measured areal hole density responsible for the p-type surface conductivity (10^{-4}–10^{-5} Ω^{-1}) lies in the range of 10^{12}–10^{13} cm^{-2} with Hall mobility between 10 and 100 cm^2/Vs.

the outstanding traits of diamond ranks a property that it shares with no other semiconductor: a highly stable intrinsic Negative Electron Affinity (NEA). The electron affinity of a semiconductor is defined as the energy difference between the vacuum level and the Conduction Band Minimum (CBM): when in a semiconductor an electron is raised from the valence band to the CBM, for example by light, such an

electron is not free to leave the sample because at the surface it encounters an energetic barrier of a few eV, the electron affinity χ and in this case the crystal has a positive electron affinity (PEA)[111,112]. The negative electron affinity of diamond is stable in air up to several hundred °C and its most conspicuous consequence is a yield of photoelectrons that exceeds that of a surface with PEA by several orders of magnitude[113,114]. From a diamond surface coming from the polisher's wheel or synthesized by CVD, an electron at the CBM is free to leave the crystal because such a barrier does not exist; χ is negative and consequently the surface has Negative Electron Affinity. The NEA of diamond has been discussed qualitatively using secondary electron microscopy (SEM), X-ray induced photoelectron spectroscopy (XPS) and ultraviolet light induced photoelectron spectroscopy (UPS): the formation of C–H dipoles is considered to be the origin of the negative electron affinity of hydrogen-terminated diamond. In case of oxidized diamond, the dipole is reversed which gives rise to a positive electron affinity (PEA) and to an insulating surface[111,112,115].

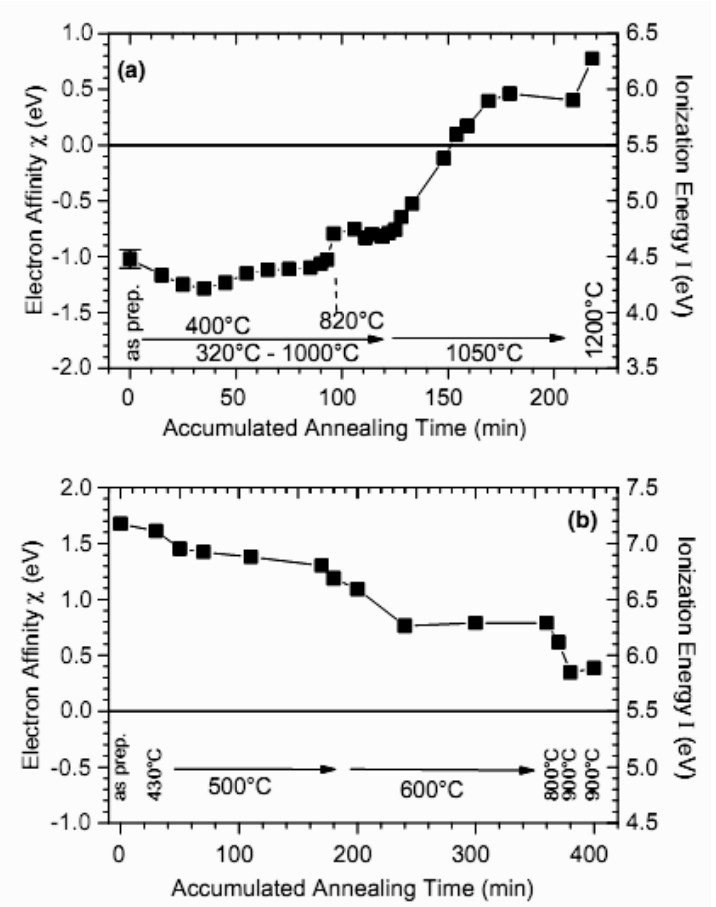


Figure 13 - Electron affinity and ionization potential of a hydrogen (a) and an oxygen (b) terminated diamond (100) surface during thermal desorption of the terminating species.

Among The surface conductivity is only observed on hydrogenated diamond, and disappears when the surface undergoes dehydrogenation or oxidation[116].

Therefore several mechanisms have been proposed to explain how hydrogen causes surface hole accumulation layer leading to the surface conductivity:

a) the passivation of deep levels (e.g. trap states, gap states) and grain boundaries by subsurface hydrogen[117]; this theory was basically hazarded during a study of hydrogenation as an alternative to Deep Level Transient Spectroscopy (DLTS), suitable for characterization of traps in a wide-band-gap material like diamond;

b) the formation of shallow acceptor states by hydrogen incorporated to a depth of around 0.6 µm in diamond subsurface[118];

c) the existence of hydrogen-induced shallow acceptors in the surface region of as-deposited hydrogenated diamond films within a region of 200Å below the surface[119,120];

d) the possible existence of acceptor-type energy states includes surface C–H bonds with energy levels around diamond VBM [121] that would explain the surface conductivity[122];

e) the ionization of acid in water produced oxonium ion (H_3O^+) which reacts with hydrogen on diamond film and causes the creation of holes in diamond film[123].

However, none of these mechanisms satisfactorily explains this intriguing phenomenon of surface conductivity due to conflicts with experimental results as well as theoretical calculations [124,125].

In 2000, inspired by the electrochemical model by Japanese researchers (c) [119,120], Maier *et al.* proposed the so-called *surface transfer doping model*[126]. Under the framework of the electrochemical surface transfer doping model [127], red/ox couples in the adsorbed water layer provide the surface acceptor levels necessary for initiating electron transfer across the diamond/air interface, thereby resulting in an accumulation of subsurface holes in diamond. The charge transfer proceeds until thermodynamic equilibrium between the electrochemical potential of the electrons involved in the red/ox reaction and the Fermi level of diamond is reached. Such red/ox couple was initially to be H_3O^+/H_2[126]. More recently, alternative O_2 red/ox couple (i.e. O_2/H_2O for acid condition, O_2/OH for basic condition) has been proposed[128] and experimentally verified as more realistic surface acceptors to electrochemically facilitate interfacial electron transfer[129,130], owing to their lower electrochemical windows than that of H_3O^+/H_2 red/ox couple[2] and higher O_2 concentration dissolved in the adsorbed water layer. Although it is still not clear which red/ox couple is mainly responsible for inducing surface conductivity in diamond, the electrochemical surface transfer doping model is well-accepted over other competing models. It can not only explain the p-type surface conductivity of diamond, but also can be potentially implemented as an alternative way to dope diamond with unprecedented advantages. For example, the

ultrashallow junction formation crucial to nanoscale devices is readily achieved by surface transfer doping because the resulting hole accumulation layer in diamond is confined to the top few nanometers[131].

Substantial p-type surface conductivity of diamond can be readily achieved via surface transfer doping using atmospheric surface acceptors. However, problems are encountered in applying this method as a practical doping scheme for diamond electronic device applications include the lack of controllability of the induced hole concentration, and the volatile device performance due to the poor thermal-stability of the physisorbed wetting layer.

Therefore, organic molecules have been proposed as alternative ‘‘solid-state” surface transfer dopants due to their good thermal stability, non-volatility after adsorption, compatibility with low-temperature or solution processing, the ability to selectively dope and hence pattern the diamond surface via thermal evaporation, tunability of electronic properties by chemical structure modifications, and the wide selection of molecules with suitable electron affinities (EA). A number of organic molecules have already been demonstrated by principles calculations to be effective surface acceptors on diamond, including fullerene and fluorinated fullerene (C_{60}, $C_{60}F_{36}$)[132,133] and 2,3-dichloro-5,6-dicyano-1,4-benzoquinone (DDQ)[134]. High surface conductivity in diamond induced by deposition of fullerenes and fluorinated fullerenes has been observed experimentally[135].

4.4.1 General Concepts

For classical doping of semiconductors, the dopant, incorporated atoms into the host lattice, releases an eccess of electron as a free negative charge carrier to the semiconductor (n-type) or consumes one more electron for chemical bounding than it brought whit them (p-type). The electrons or holes remain weakly bound to the dopants that carry their respective counter charge, and it takes a characteristic activation energy to release them as free charge carriers (Figure 14, left).

However doping can also be achieved by an electron exchange between a semiconductor and dopants situated at its surface. In general terms, surface transfer doping relies on exchange of electrons between an intrinsic semiconductor on the one side and an electron accepting reservoir at the surface on the other side. This electron accepting reservoir can be less or more complex, from isolated molecules to thin solid layers up to electrochemical phases with various sorts of solvated ionic species. This electronic reservoir can be called “surface acceptors”.

The surface dopants (e.g. acceptors) possess Unoccupied Molecular Orbitals (UMOs). If the energetically Lowest Unoccupied Molecular Orbital (LUMO) is close to the Valence Band Maximum (VBM) of the semiconductor, it will steal an electron from the semiconductor, just like classical acceptors do. As a result, holes will form in

the semiconductor, and negative charge will be localized on the surface acceptors: this charge separation will automatically established an electrostatical potential that confines the holes in a perpendicular direction but leaves them free to move parallel to the surface.

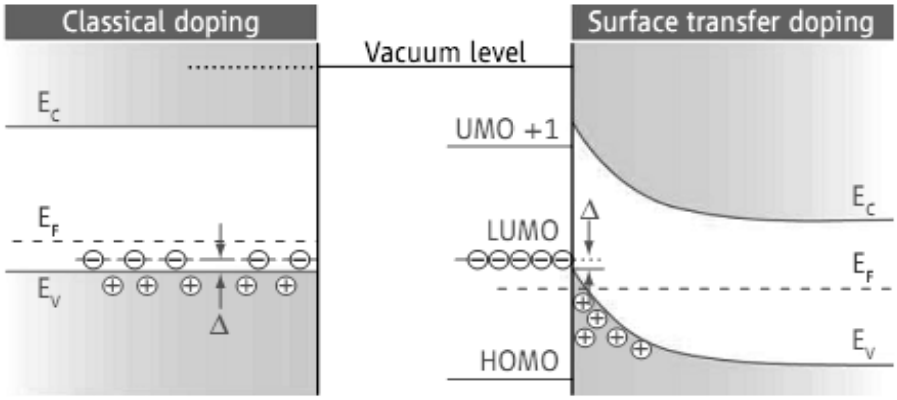


Figure 14 - Beyond conventional doping. This band diagram illustrates classical p-type doping (left) and p-type surface transfer doping (right), using the energy of an electron in free space as a reference (vacuum level). E_c and E_v are the energies of the conduction band minimum (CBM) and the valence band maximum VBM), respectively. The balance between electrons localized in acceptor states and free holes in the valence band is expressed by the constant Fermi energy E_F. The closer E_F is to E_v, the higher the local density of holes. LUMO and HOMO are the lowest unoccupied and highest occupied molecular orbitals of the surface acceptors, respectively.

More specifically, when diamond is brought together with surface acceptors, which in principle can be solvated electrochemical species (O_2 red/ox couples), isolated molecules or solid adsorbates, the Fermi energy difference between diamond and the surface adsorbates (electrochemical potential equivalent for aqueous solution) will drive electrons from diamond valence band to the electronic empty acceptor level of the surface adsorbates (e.g. LUMOs). As a result of the interfacial charge transfer, the surface adsorbates became negatively charged, and equal numbers of compensating holes accumulate in diamond valence band. Together they build up a space-charge layer with associated upward band bending toward diamond surface. This in turn raises the Fermi level of the surface adsorbates so that it aligns with the Fermi energy of diamond at thermodynamic equilibrium (Fig...). The upward band bending can be so strong that the Fermi level of diamond is forced below the VBM at the surface for the highly doped case, resulting in a degenerate situation.

Two prerequisites must be satisfied for effective surcafe transfer doping of diamond (or other semiconductors):

a) To induce significant interfacial charge separation between the surface adsorbates and diamond, the LUMO of the surface adsorbates must be close to or below the VBM of diamond for surface transfer p-type doping, or highest

occupied molecular orbital (HOMO) of the surface adsorbates must lie close to or above the CBM of semiconductor for surface transfer n-type doping.

b) The excessive holes or electrons resulting from interfacial charge transfer must be delocalized in the near interface region yet mobile parallel to surface to serve as effective charge carriers. The accumulated holes or electrons tend to be confined (squeezed) normal to the surface by the electric field created by interfacial charge separation, thereby resulting in a narrow space-charge layer of the order of several nm.

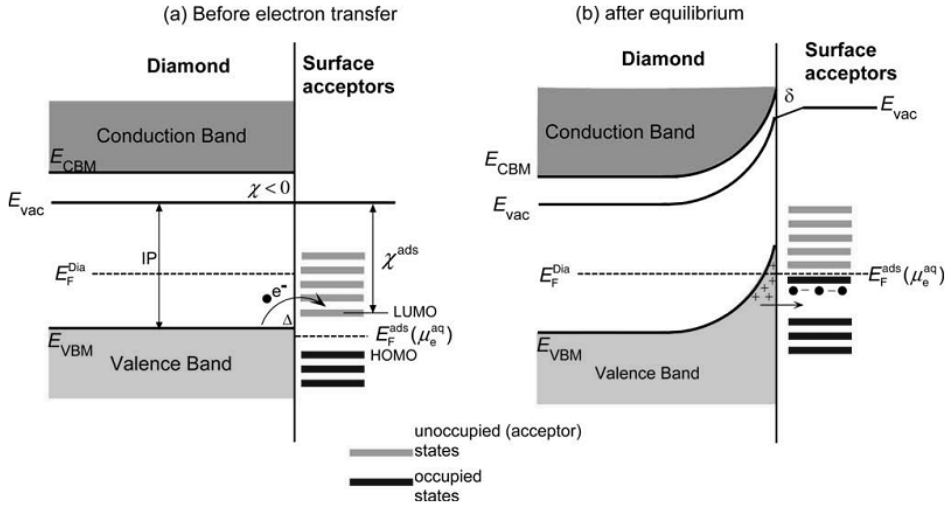


Figure 15 - Schematic energy levels for p-type surface transfer doping process. (a) Before electron transfer, the Fermi level (E_F^{ads})or electrochemical potential (μ_e^{aq}) of the adsorbates is lower than that of the diamond. Electron transfer from diamond valence band to adsorbates' unoccupied acceptor states (LUMO) is energetically favored. (b) In thermal equilibrium after electron transfer, Fermi levels on both sides are aligned and the diamond has a layer of accumulated holes at its surface, with equal amount of compensating electrons in adsorbates.

In 2004, Nebel *et al.*[136,137] summarized the results of several experiments on hydrogen terminated diamond and presented theoretical calculations of the density-of-states (DOS) in diamond at the interface to an adsorbate layer, starting from Maier's explication[126] of the origin of surface conductivity.

Maier proposed that pH value of water is about 6 due to CO_2 content or other ionic contamination, so they calculated the chemical potential for such an aqueous wetting layer to be about -4.26 eV. Considering hydrogen terminated diamond negative electron affinity to be -1.3eV, the pinning position of the Fermi level E_F at the water/diamond interface would be about 50 meV below the VBM: this is enough to generate a hole accumulation layer at the surface of diamond. Figure 16 shows the schematic energy band diagram of the density of states at the interface diamond/H-terminated diamond surface (C-H)/adsorbate layer, as measured by Contact Potential Difference (CPD) experiments applied to characterize the surface Fermi-level with

respect to an Au and Al structure (Au work-function has been used for calibration of the Kelvin probe experiment) where the NEA of -1.3 eV has been taken into account. The C-H dipole energy has been calculated to be 1.68 eV[138].

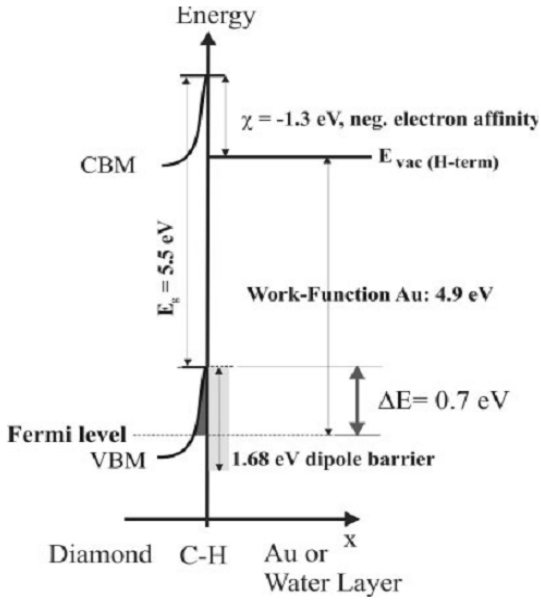


Figure 16 - Schematic energy band diagram of the density of states at the interface diamond/H-terminated diamond surface (C–H)/adsorbate layer.

Figure 17 shows a schematic view of the electronic properties at the surface of H-terminated diamond, where valence-band electrons can diffuse into empty electronic states of an adsorbate layer. Such diffusion gives rise to a band-bending which decrease in diamond with increasing distance to the surface. To calculate the width of band-bending in proximity of the surface of diamond a numerical approach has been developed to solve the schrodinger and Poisson equations simultaneously based on the narrow GaAs/$Ga_{1-x}Al_xAs$ hetero-junctions models[139]. It has to be taken into account that in case of band-bending over a distance which is shorter than the De Broglie wavelength of about 100 Å for holes (in diamond), the three dimensional (3D) DOS is changing to a two dimensional (2D) DOS as shown in figure 17b. Calculations have been performed for hole sheet density of 5×1012 cm-2 and 5×1013 cm-2. In the first case ($N=5\times10^{12}$ cm^{-2}), the Fermi energy is 237 meV below VBM at the interface (VBM_{INT}), in the second case Fermi energy is close to 90 meV: in both situations three different discrete energy levels below VBM_{INT} are present. In 2010 a detailed study of the 2D Hole Gas (2DHG) underlying the C(001):H surface has been presented based on a 1D self-consistent Poisson-Schrödinger model[140]. Surface transfer doping gives rise to a potential which confines a sheet of holes within a depth of 0.2 nm of the C:H interface. The occupation of these states has been computed to allow a determination of

the Fermi level as a function of temperature and hole sheet density: the Fermi level resides below the VBM in the valence band and previously discussed results are substantially confirmed.

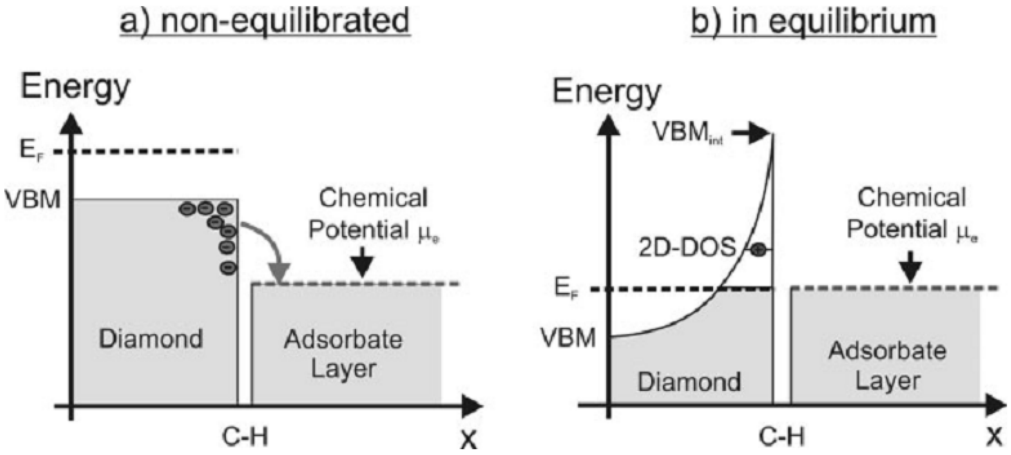


Figure 17 - Schematic drawing of the diamond/adsorbate hetero-junction for the non-equilibrated (a) and for the equilibrated (b) case. Electrons from the valence-band diffuse into empty electronic states of the adsorbate layer as long as the chemical potential μ_e is lower than the Fermi energy.

Experiments in combination with numerical calculation indicate that the Fermi energy in diamond at the interface of H-terminated diamond/adsorbate layer is deep below the VBM_{INT}. Due to the high density of states in the valence band, a Two Dimensional Density of States (2D-DOS) for holes is generated.

Other groups experimentally showed the formation of well-defined quantum states of holes in the 2D surface layer present on hydrogenated air-exposed diamond surface by means of Field Emission Measurements[141]. This quantization is evident from the appearance of discrete jumps in the electron emission current, at well-defined values of the extracting electric field. The fact that quantum effects are found[142], at RT, in the field emission from a front contacted surface conducting diamond and that they can be theoretically reproduced, supports the hypothesis that it is the “surface transfer doping” model that gives rise to surface conduction of H-terminated diamond, also showing that such field emission properties of H-terminated intrinsic diamond covered with an adsorbate layer can be attributed to the 2D-DOS at the diamond surfaces[143].

5. Electronic Contacts on Diamond

5.1. Contact theory

Metal and semiconductor have to be considered as two different energy levels. They can be seen as completely full for energies lower than Fermi level (electrons) and completely empty for higher energies (holes). In figure 18, E_0 represents the energy of

free electron in vacuum, φ the work function (energy needed for electrons transition from Fermi level to vacuum level) and χ is the semiconductor electron affinity. Besides, E_C and E_V are obviously conduction and valence band energy respectively while E_g is the gap between them ($E_g=E_C-E_V$)

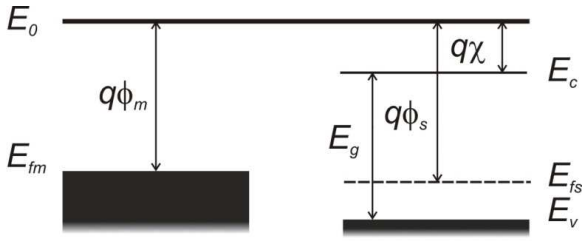


Figure 18 – Energy levels for a metal and a semiconductor

Different situations can be found in dependence of the positions of the different energy levels: in a *p*-type semiconductor the Fermi level will be close to the valence band E_V while for a *n*-type semiconductor it will be close to conduction band E_C. Considering the contact between a metal and p-type semiconductors where $\varphi_M<\varphi_S$ (Schottky contact), holes will be the carriers for the conduction phenomena in the material and the semiconductor Fermi level will be lower than the metal Fermi level.

At thermodynamic equilibrium, Fermi levels must be equal so the semiconductor needs a holes depletion at the interface, an electrons flow from metal to semiconductor: this process will result in a electric field that will saturate creating a rectifying junction, the Schottky junction.

5.1.1. Schottky Junction

The built in voltage φ_i is defined as $\varphi_{i=}\ \varphi_m-\varphi_s$ and $q\varphi_i$ is the barrier height bring by holes from semiconductor to metal. Schottky barrier is defined as: $q\varphi_{B0=}E_g+q\chi-q\varphi_m$, basically the barrier height bring by holes from metal to semiconductor.

Electric field is completely localized in the semiconductor depleted layer and, in the ideal hypothesis of full depletion, charge distribution and electric field for a p-type metal-semiconductor junction are shown in figures 18b and 18c. If metal can be considered a perfect conductor, charge distribution would be parallel to its surface. By the way in an ideal *p*-type semiconductor, negative charge would be due either to ionized acceptors and free electrons, while holes would be responsible of positive charge. In depletion approximation, x_d is the spatial charge extension and the maximum for electric field is at the interface. From the Maxwell equations ($dE/dx=\rho/\varepsilon$) result, with $\rho=qN_A$:

$$E(x)=\frac{qN_A}{\varepsilon_s}(x_d-x)$$

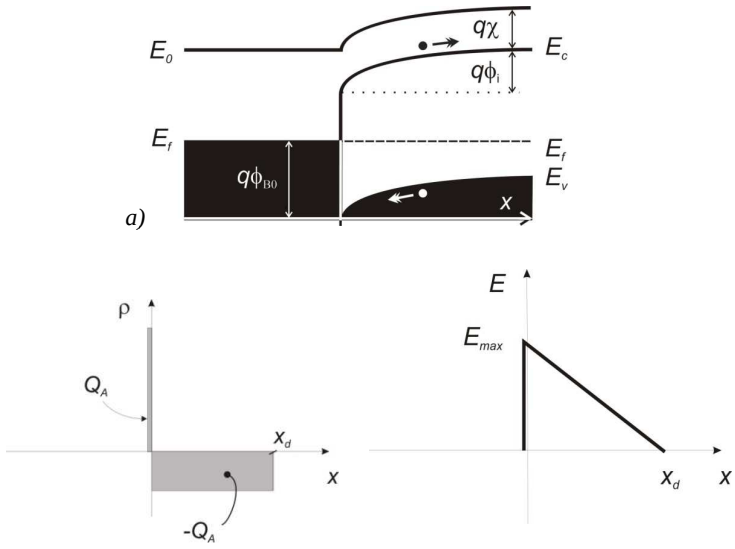


Figure 19 – a) band diagram of a p-type semiconductor Schottky junction, b) charge distribution in the full depletion hypothesis, c) electric field behavior for full depletion

And so $E_{max}=(qN_Ax_d)/\varepsilon_s$. Considering $E(x)=-grad[\varphi(x)]$, *built-in* is:

$$\varphi_i = \varphi(x = x_d) = -\frac{1}{2}E_{max}x_d = -\frac{1}{2}\frac{qN_Ax_d^2}{\varepsilon_s}$$

From φ_i equation, it is possible to find the extension of the depletion region. So, the surface space charge density in the semiconductor is $Q_A=qN_Ax_d=(-2q\ \varepsilon_s N_A\ \varphi_i)^{1/2}$.

The entire voltage drop is extended only in the semiconductor. If an external voltage would be applied, it would be supported by semiconductor and it would result in a modification of the band diagram, changing voltage bending and φ_i value. When the metal is negative biased as for the semiconductor, there is a reduction of such a barrier and, the other way round, it increases in the opposite conditions (see Fig 20a and 20b).

In inverse biasing conditions a positive voltage is applied on the metal and the built-in voltage drops down to a negative value (φ_i-V_a). The space charge in the depleted region increase to $Q_A=[-2q\ \varepsilon_s\ N_A(\varphi_i-V_a)]^{1/2}$. Applying a small alternate signal, the junction points out a capacitive behavior, characterized by a specific capacitance:

$$C_S = \left|\frac{\partial Q_S}{\partial V_a}\right| = \sqrt{-\frac{q\varepsilon_s N_A}{2(\varphi_i - V_a)}} = \frac{\varepsilon_s}{x_d}$$

that could be explicited for V_a as:

$$V_a = \varphi_i + \frac{q\varepsilon_s N_A}{2}\frac{1}{C_s^2}$$

It is worth to notice that the slope of such a curve points out the acceptors concentration and the interception with the voltage axis provide an approximation of the built-in value.

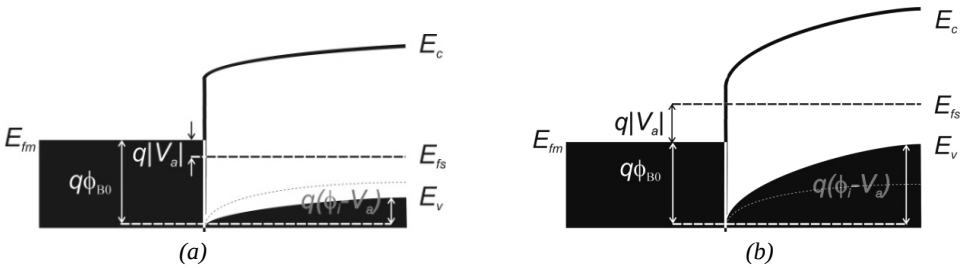


Figure 20 – Band bending for a *p*-type semiconductor: a) direct biasing for $V_a<0$ results in a barrier lowering, b) inverse biasing for $V_a>0$ results in a barrier incresing

$$N(x_d) = \frac{2}{q\,\varepsilon_s\;\partial C^{-2}/\partial V} = -\frac{C^3}{q\,\varepsilon_s}\left(\partial C/\partial V\right)^{-1}$$

The current across a metal-semiconductor junction is mainly due to majority carriers. Three distinctly different mechanisms exist: diffusion of carriers from the semiconductor into the metal, thermionic emission of carriers across the Schottky barrier and quantum-mechanical tunneling through the barrier. The diffusion theory assumes that the driving force is distributed over the length of the depletion layer. The thermionic emission theory on the other hand postulates that only energetic carriers, those, which have an energy equal to or larger than the conduction band energy at the metal-semiconductor interface, contribute to the current flow. Quantum-mechanical tunneling through the barrier takes into account the wave-nature of the electrons, allowing them to penetrate through thin barriers. In a given junction, a combination of all three mechanisms could exist. However, typically one finds that only one current mechanism dominates.

The analysis reveals that the diffusion and thermionic emission currents can be written in the following form:

$$J_p = qvN_c e^{-\varphi_B/V_t}\left(e^{V_a/V_t} - 1\right)$$

This expression states that the current is the product of the electronic charge, q, a velocity, v, and the density of available carriers in the semiconductor located next to the interface. The velocity equals the mobility multiplied with the field at the interface for the diffusion current and the Richardson velocity for the thermionic emission current. The minus one term ensures that the current is zero if no voltage is applied as in thermal equilibrium any motion of carriers is balanced by a motion of carriers in the opposite direction.

The tunneling current is of a similar form, namely: $J_p = q\ v_R\ n\ \Theta$, where v_R is the Richardson velocity and n is the density of carriers in the semiconductor. The tunneling probability term, Θ, is added since the total current depends on the carrier flux arriving at the tunnel barrier multiplied with the probability, Θ, that they tunnel through the barrier.

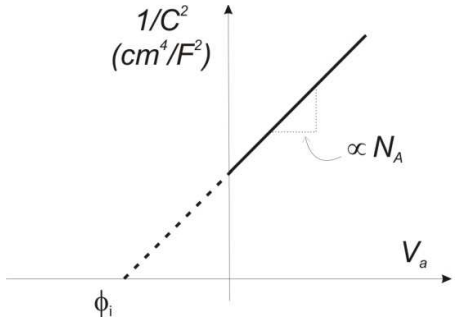


Figure 21 – Capacitance dependence on applied voltage expected behaviour

✓ *Diffusion current*

This analysis assumes that the depletion layer is large compared to the mean free path, so that the concepts of drift and diffusion are valid. The resulting current density equals:

$$J_p = \frac{q^2 D_n N_c}{V_t}\sqrt{\frac{2q(\varphi_i - V_a)N_A}{\varepsilon_s}}\left[e^{-\varphi_B/V_t}\left(e^{V_a/V_t}-1\right)\right]$$

The current therefore depends exponentially on the applied voltage, V_a, and the barrier height, φ_B. Considering $x_d=[2\varepsilon_s(\varphi_i-V_a)/qN_A]^{1/2}$, the prefactor can more easily be understood if one rewrites it as a function of the electric field at the metal-semiconductor interface, $E_{max}=(qN_Ax_d)/\varepsilon_s=[2q(\varphi_i-V_a)N_A/\varepsilon_s]^{1/2}$, yielding:

$$J_p = q\mu_p E_{max} N_c\left[e^{-\varphi_B/V_t}\left(e^{V_a/V_t}-1\right)\right]$$

where μ_p is the holes mobility from Einstein-Smoluchowski relation ($\mu=D/kT$), so that the prefactor equals the drift current at the metal-semiconductor interface, which for zero applied voltage exactly balances the diffusion current.

✓ *Thermionic emission*

The thermionic emission theory assumes that electrons, with an energy larger than the top of the barrier, will cross the barrier provided they move towards the barrier. The actual shape of the barrier is hereby ignored.

The current can be expressed as:

$$J_{MS} = A^* T^2 e^{-\varphi_B/V_t}\left(e^{V_a/V_t} - 1\right)$$

Where $A^*=(4\pi q m^* k^2)/h^3$ is the Richardson constant and φ_B is the Schottky barrier height. The expression for the current due to thermionic emission can also be written as a function of the average velocity with which the electrons at the interface approach the barrier. This velocity is referred to as the Richardson velocity given by $v_R=[kT/(2\pi m)]^{1/2}$, so that the current density becomes:

$$J_p = q v_R N_c e^{-\varphi_B/V_t}\left(e^{V_a/V_t} - 1\right)$$

✓ *Tunneling*

The tunneling current is obtained from the product of the carrier charge, velocity and density. The velocity equals the Richardson velocity, the velocity with which on average the carriers approach the barrier. The carrier density equals the density of available electrons, n, multiplied with the tunneling probability, Θ, yielding $J_p=qv_R n\Theta$, where the tunneling probability is obtained from:

$$\Theta = exp\left(-\frac{8\pi}{3}\frac{\sqrt{2qm^*}}{h}\frac{\varphi_B^{3/2}}{E}\right)$$

and the electric field equals $E= \varphi_B/L$. The tunneling current therefore depends exponentially on the barrier height, φ_B, to the 3/2 power.

5.1.2. Ohmic contacts

Metal-semiconductor contacts are an obvious component of any semiconductor device. At the same time, such contacts cannot be assumed to have a resistance as low as that of two connected metals. In particular, as already said, a large mismatch between the Fermi energy of the metal and semiconductor can result is a high-resistance rectifying contact. A proper choice of materials can provide otherwise a low resistance Ohmic contact. However for a lot of semiconductors there is no appropriate metal available. Instead one then creates a tunnel contact. Such contact consists of a thin barrier through which carriers can readily tunnel. Thin interfacial layers also affect contact formation. Most metal-semiconductor contacts are annealed or alloyed after the initial deposition of the metal in an effort to further improve the contact resistivity.

A metal-semiconductor junction results in an Ohmic contact (i.e. a contact with voltage independent resistance) if the Schottky barrier height, φ_B, is zero or negative.

In such case, the carriers are free to flow in or out of the semiconductor so that there is a minimal resistance across the contact.

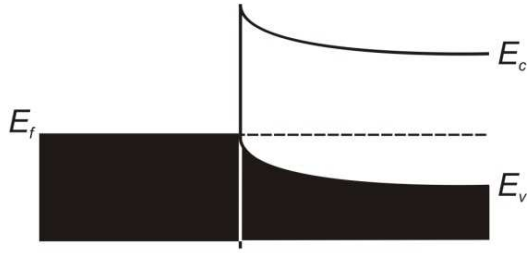
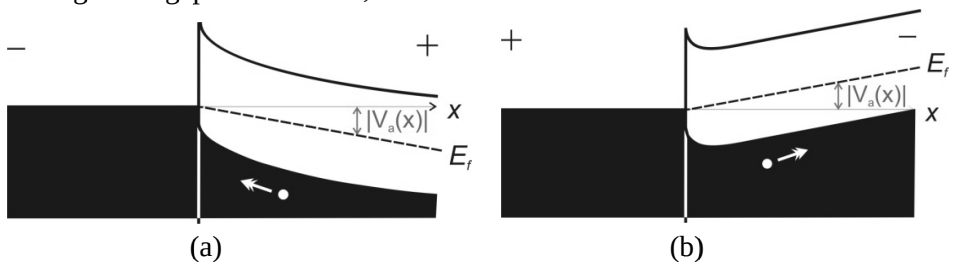


Figure 22 – Band diagram for an ohmic junction (*p*-type)

For an *n*-type semiconductor, this means that the work function of the metal must be close to or smaller than the electron affinity of the semiconductor. For a *p*-type semiconductor, it requires that the work function of the metal must be close to or larger than the sum of the electron affinity and the bandgap energy. Since the work function of most metals is less than 5 V and a typical electron affinity is about 4 V, it can be problematic to find a metal that provides an Ohmic contact to *p*-type semiconductors with a large bandgap such as GaN, SiC or Diamond.



(a) (b)

Figure 23 – Applied voltage drop is distributed beside x in the semiconductor, so the Fermi level has a dependence on x: a) direct bias, b) inverse bias

Considering a $\varphi_m > \varphi_s$ metal-semiconductor junction, Fermi levels are not aligned. The only condition for such an alignment is a holes enhancement at the semiconductor interface with the metal, that is an electrons flow from semiconductor toward the metal. In this case, the bands bend in the Schottky contact opposite way (figure 22).

For direct and inverse biasing condition, holes have no barrier to cross between semiconductor and metal: such a crossing is energetically favorite (figure 23a and 23b respectively).

✓ *Tunnel contacts*

An alternate and more practical contact is a tunnel contact. Such contacts do have a positive barrier at the metal-semiconductor interface, but also have a high enough doping in the semiconductor that there is only a thin barrier separating the metal from the semiconductor (x_d is proportional to N_A^{-1}). If the width of the depletion region at the

metal-semiconductor interface is very thin, on the order of 3 nm or less, carriers can readily tunnel across such barrier. The required doping density for such contact is theoretically higher than 10^{19} cm^{-3}.

✓ *Annealed and alloyed contacts*

The fabrication of Ohmic contacts frequently includes a high temperature step so that the deposited metals can either alloy with the semiconductor or the high-temperature anneal reduces the unintentional barrier at the interface. In the case of silicon, one can simply deposit a metal such as aluminium and obtain a reasonable Ohmic contact. However, subsequent annealing at 475°C in a reducing ambient such as forming gas (20:1 N_2/H_2) will further improve the contact resistivity. The temperature is chosen below the eutectic temperature of the Si/Al eutectic composition. Annealing at higher temperature causes the formation of Si/Al alloys, which in turn causes pits in the silicon. This effect is also referred to as spiking and when penetrating through an underlying p-n junction these "spikes" dramatically affect the quality of the p-n junction as can be observed in the form of an enhanced leakage current or reduced breakdown voltage. The use of a reducing atmosphere avoids any further oxidation of the metal during annealing, while it can also reduce any interfacial oxide between the metal and semiconductor. Aluminum deposited onto low-doped silicon (< 10^{15} cm^{-3}) tends to form Schottky barriers, so that it is advantageous to provided a more-highly doped contact region underneath the contact metal. The small barrier height can be overcome through thermionic emission, while the contact resistance is further improved by creating a tunnel barrier using degenerately doped contact layers.

Contacts to compound semiconductors require some more attention. Selecting a material with the right work function might still not result in the expected Ohmic contact. This is caused by pinning of the Fermi energy at the interface due to the large number of surface states at the metal-semiconductor interface. This only leaves the tunnel contact as a viable low resistance contact. To further improve the tunnel contact one adds dopants. An anneal at 400°C in a forming gas ambient for ten minutes causes the dopants to alloy with the semiconductor, thereby forming a thin high-doped region as desired for a tunnel contact.

✓ *Contact resistance to a thin semiconductor layer*

The contact between a metal and a thin semiconductor layer can be described with the resistive network shown in Figure 24.

This equivalent circuit is obtained by slicing the structure into small sections with length Δx, so that the contact resistance, R_1, and the semiconductor resistance, R_2, are given by $R_1=\rho_c/(W\Delta x)$ and $R_2=R_s\Delta x/W$ where ρ_c is the contact resistance of the metal-to-semiconductor interface per unit area with units of Ωcm^2, R_s is the sheet resistance of the semiconductor layer (the sheet resistance is formally a measure of resistance of

thin films that are namely uniform in thickness) with units of $\Omega_{/\square}$ (Ohms per square), and W is the width of the contact.

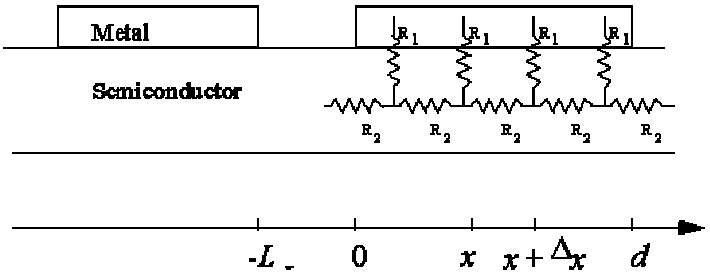


Figure 24 - Distributed resistance model of a contact to a thin semiconductor layer.

Using Kirchoff's laws one obtains the following relations between the voltage, *V(x)*, across the M-S interface and the current, *I(x)*, parallel to the interface at *x* and *x+Δx*.

$$V(x+\Delta x) - V(x) = I(x)R_2 = I(x)\frac{R_s}{W}\Delta x$$

$$I(x+\Delta x) - I(x) = \frac{V(x)}{R_1} = V(x)\frac{W}{\rho_c}\Delta x$$

By letting Δx approach zero and combining the two obtained differential equations into

$$\frac{\partial^2 I(x)}{\partial x^2} = I(x)\frac{R_s}{\rho_c} = \frac{I(x)}{\lambda^2} \text{ with } \lambda = \sqrt{\frac{\rho_c}{R_s}}$$

The parameter λ is the characteristic distance over which the current changes under the metal contact and is also referred to as the penetration length. The general solution for I(x) and V(x) are, where *d* is the distance:

$$I(x) = I_0 \frac{\sinh\frac{d-x}{\lambda}}{\sinh\frac{d}{\lambda}} \text{ and } V(x) = I_0 \frac{\lambda R_s}{W}\frac{\cosh\frac{d-x}{\lambda}}{\sinh\frac{d}{\lambda}}$$

The total resistance of the contact is:

$$R_c = \frac{V(0)}{I(0)} = \frac{\lambda R_s}{W}\coth\frac{d}{\lambda} = \frac{\sqrt{\rho_c R_s}}{W}\coth\frac{d}{\lambda}$$

In the limit for an infinitely long contact (or $d>>\lambda$) the contact resistance is given by:

$$R_c = \frac{\sqrt{\rho_c R_s}}{W}$$

5.2. Contacting Diamond

For diamond to be used as a semiconductor in devices, high quality contacts are essential and the requirements on such contacts vary from application to application. Metallurgical stability at elevated temperatures and good adhesion, such as for the bonding of components on CVD diamond heat sinks for multi-chip modules, are important for any of these. These two requirements, however, are difficult to meet with a single film, since good adhesion requires a reaction between the covalently bonded diamond and the metal. However, metallurgical interactions degrade adhesion and electrical properties at the bond, thus limiting the applicability of these metallizations[144]. In general the requirements for ohmic contacts can be summarized as follows [145]:

a) low contact resistivity (for ohmic/non-rectifying contacts);
b) good adhesion;
c) high thermal stability;
d) high corrosion resistance;
e) bondable top-layer;
f) suitable for micro-patterning.

Most metal contacts to semiconductors are non-ohmic due to surface depletion. The most common method used to achieve ohmic behaviour is to increase the doping concentration, and this has been employed in diamond.

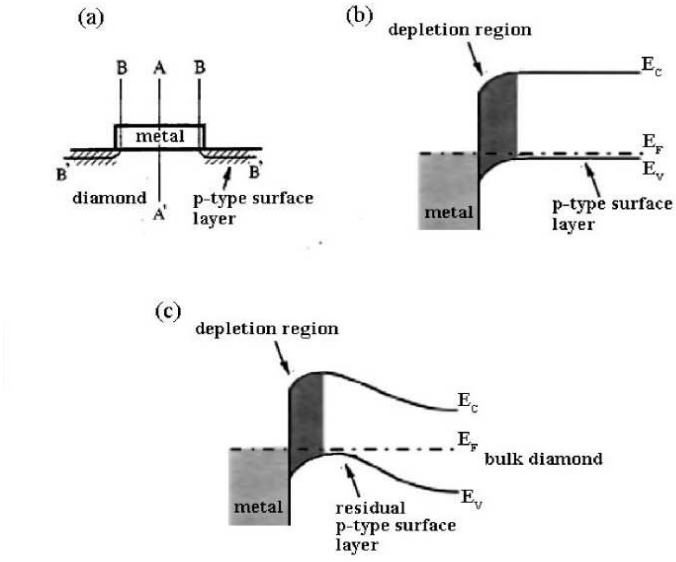


Figure 25 – Band diagram of metal-hydrogen terminated diamond junction: a) contact scheme, b) BB' band diagram, c) AA' band diagram

This has the effect of reducing the depletion width and hence the contact resistance by increasing tunnelling through the Schottky barrier. It has been found that by using carbide-forming metals (such as Mo, Ta, Ti) in combination with annealing, it is possible to make ohmic contacts to p-type diamond[146,147] with specific contact resistance as low as ~10^{-7} Ωcm^2[148]. This is thought to be due to enhanced conduction through areas in which metal-carbide formation has occurred. Ohmic contacts to *n*-type diamond have been much more difficult to realize. Kato *et al.*[149] reported Ti contacts to heavily phosphorus-doped diamond films (N_d~10^{20} cm^{-3}) that, although non-ideal, exhibited contact resistances down to 10^{-3} Ωcm^2. Schottky contacts to diamond have been fabricated using both non-carbide forming (e.g. Al, Pt) and carbide forming metals, although the latter metals should not be annealed.

Metal contacts to H-terminated electronic surface devices such as surface field-effect transistors often use Al for the gate and Au for the source and drain. Further details will be discussed in section 7.3.

Properties of a junction between *p*-type diamond and a metal can be interpreted with the already exposed Schottky barrier theory, taking in to account the high number of diamond surface defects that cramp the barrier height to a value independent on the metal work function[150,151] and considering the hydrogen terminated surface as a thin *p*-type semiconductor layer. The *BB'* part in figure 25a induces a band bending over as shown in figure 25b and therefore it acts like a metal-semiconductor junction. In order to be a rectifying junction on a p-type semiconductor (the hydrogen terminated layer) it has to be $\varphi_m < \varphi_s$ where φ_s is the distance between the Fermi level of the *p*-type layer and the vacuum level. The depletion region begins from the metal-diamond interface and its extension depends on the metal work function: a higher Schottky barrier for a smaller work function resulting in a higher band bending and depletion length.

The AA' section in figure 25a presents a path from metal, across hydrogen terminated surface, down to diamond (assumed ideally defects free). Considering the theoretical model of hydrogen as a acceptor states generator on diamond surface, the band diagram is shown in figure 25c. Besides, the depletion region is not deeply extended in the conductive layer, resulting in an up band bending. Going toward the bulk diamond, Fermi level returns the same as the bulk. Nevertheless, it is possible to point out a residual holes accumulation just beyond the depletion region: the junction depletion region length is smaller than the hydrogen terminated layer air exposed.

The following table presents a simple breviary of metals behavior on hydrogen terminated diamond surface.

Establishing high quality contacts to the diamond is also important. Repeated re-contacting of the same diamond device has shown that significant variations in performance can occur, for the same contact recipe. Evaporated gold can work well in

many circumstances but can suffer from low mechanical adhesion and thus poor longevity. Other successful schemes include layers with carbide formers such as Cr or Ti, and one type of DLC developed by Diamond Detectors Ltd[198].

Table 3 - metals behavior on hydrogen terminated diamond surface

Metal	Electron Affinity	Contact Behavior	Schottky Barrier Height (eV)	Rectification Ratio
Mg	1.2	Schottky	0.94	10^8
Zn	1.5	Schottky	0.92	10^7
Al	1.5	Schottky	0.85	10^7
Ta	1.5	Schottky	0.80	10^6
In	1.7	Schottky	0.81	10^6
Pb	1.7	Schottky	0.80	10^6
Ni	1.8	Schottky	0.58	10^4
Fe	1.8	Schottky	0.54	10^3
Ag	1.9	Ohmic	<0.3	-
Pd	2,2	Ohmic	<0.3	-
Au	2.3	Ohmic	<0.3	-
Pt	2.4	Ohmic	<0.3	-

6. Metal Semiconductor Field Effect Transistor (MESFET)

Even if a model for metal semiconductor field effect transistor is not completely accepted by scientific community, hydrogen terminated diamond based devices fabricated in this thesis could be associated to such a device. Here author reports a brief theoretical model of MESFET in order to relate following characterization results to this structure.

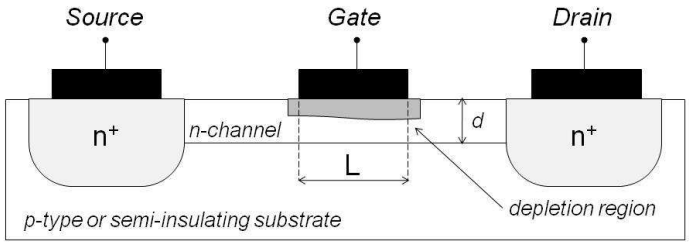


Figure 26 – Schematic of a n-type channel MESFET

Typical structure of a metal semiconductor field effect transistor is made up with a Schottky junction, acting like a control electrode (a gate), in between of two ohmic contacts, the source and the drain. Current between ohmic contacts depends on the

cross sectional of conductive channel under gate electrode, that in turn depends on applied voltage: the control of the channel is obtained by varying the depletion layer width underneath the metal contact which modulates the thickness of the conducting channel and thereby the current between source and drain. MESFET is basically a different kind of JFET (Junction Field Effect Transistor), an amplifier device that differ from MESFET in a *pn* instead of a Schottky junction. Schottky junction is actually important for semiconductors that present a difficult doping process.

The key advantage of the MESFET is the higher mobility of the carriers in the channel as compared to the MOSFET. Since the carriers located in the inversion layer of a MOSFET have a wave function, which extends into the oxide, their mobility - also referred to as surface mobility - is less than half of the mobility of bulk material. As the depletion region separates the carriers from the surface their mobility is close to that of bulk material. The higher mobility leads to a higher current, transconductance and transition frequency of the device. The drawback of the MESFET structure is the presence of the Schottky metal gate. It limits the forward bias voltage on the gate to the turn-on voltage of the Schottky diode. This turn-on voltage is typically 0.7 V for GaAs Schottky diodes. The threshold voltage therefore must be lower than this turn-on voltage. As a result it is more difficult to fabricate circuits containing a large number of enhancement-mode MESFET.

The higher transition frequency of the MESFET makes it anyway particularly of interest for microwave circuits. While the advantage of the MESFET provides a superior microwave amplifier or circuit, the limitation by the diode turn-on is easily tolerated. Typically depletion-mode devices are used since they provide a larger current and larger transconductance and the circuits contain only a few transistors, so that threshold control is not a limiting factor. The buried channel also yields a better noise performance as trapping and release of carriers into and from surface states and defects is eliminated.

The use of wide band gap semiconductors based rather than silicon MESFETs provides two more significant advantages: first, the electron mobility at room temperature is larger while the peak carriers velocity is higher; Second, it is easy to fabricate semi-insulating or insulating substrates, which eliminates the problem of absorbing microwave power in the substrate due to free carrier absorption.

6.1. MESFET Operation

The threshold voltage, V_T, of a MESFET is the voltage required to fully deplete the doped channel layer. This threshold voltage equals:

$$V_T = \varphi_i - \frac{qN_d d^2}{2\varepsilon_s}$$

where φ_i is the built-in potential and d is the thickness of the doped region. This threshold voltage can also be written as a function of the pinch-off voltage, $V_T=\varphi_i-V_P$, where the pinch-off voltage equals:

$$V_P = \frac{qN_d d^2}{2\varepsilon_s}$$

The derivation of the current in a MESFET starts by considering a small section of the device between y and $y+dy$. The current density at that point can be written as a function of the gradient of the channel voltage V_C:

$$J = qnv = qN_d \mu_n E = -qN_d \mu_n \frac{\partial V_C(y)}{\partial y}$$

The drain current I_D is related to the current density and the part of the MESFET channel that is not depleted.

$$I_D = -JW(d - x_n(y))$$

Where the depletion layer width at position y is related to the channel voltage, $V_C(y)$, by:

$$x_n(y) = \sqrt{\frac{2\varepsilon_s(\varphi_i - V_G + V_C(y))}{qN_d}}$$

The equation for the current can now be integrated from source to drain, yielding:

$$I_D = qN_d \mu_n d \frac{W}{L}\left(V_C|_0^{V_D} - \frac{(\varphi_i - V_G + V_C)^{3/2}}{\sqrt{V_P}}|_0^{V_D} \right)$$

Since the steady-state current in the device is independent of position, the left hand term equals I_D times L, so that integration results in (Fig. 27):

$$I_D = qN_d \mu_n d \frac{W}{L}\left[V_D - \frac{2}{3}\left(\frac{(\varphi_i - V_G + V_D)^{3/2}}{\sqrt{V_P}} - \frac{(\varphi_i - V_G)^{3/2}}{\sqrt{V_P}} \right) \right]$$

This result is valid as long as the width of the un-depleted channel $[d - x_n(y)]$ is positive, namely for $V_D \leq V_G - V_T$. This condition also defines the quadratic region of a MESFET. For larger drain voltage, the current saturates (Fig. 28) and equals that at $V_D=V_G-V_T=V_{D,sat}$. The corresponding current is the saturation current, $I_{D,sat}$:

$$I_{D,sat} = qN_d \mu_n d \frac{W}{L}\left[V_G - V_T - \frac{2}{3}\left(V_P - \frac{(\varphi_i - V_G)^{3/2}}{\sqrt{V_P}} \right) \right]$$

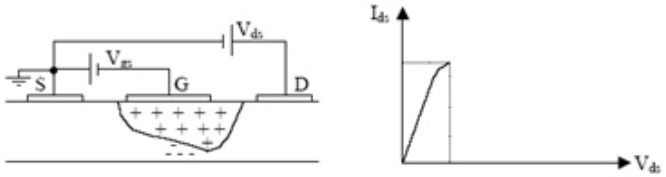


Figure 27 – linear operation region for a n-type channel MESFET

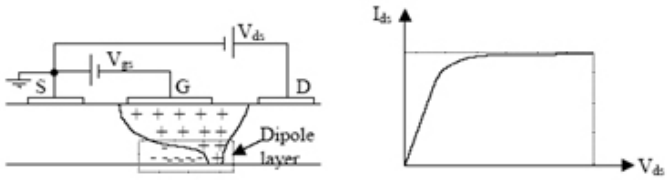


Figure 28 - saturated operation region for a n-type channel MESFET

An example of the resulting I-V characteristics is shown in figure below (Fig. 29).
The transfer characteristic of a MESFET is compared to a quadratic expression of the form:

$$I_{D,sat} = \mu_n \frac{\varepsilon_s}{w} \frac{W}{L} \frac{(V_G - V_T)^2}{2}$$

where *w* is the average depletion layer width in the channel layer. The quadratic expression yields the same current at $V_G=\varphi_i$ for $w=3d/8$. The close fit is at times used to justify using the simpler quadratic equation.

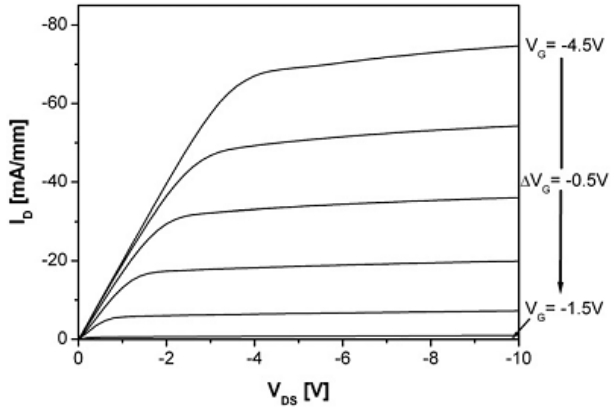


Figure 29 –DC output characteristic of a p-channel diamond MESFET with L_G=1 µm and W_G=20 µm. Drain current density reaches 75 mA/mm at V_{GS} =−4.5 V and pinch off is observed at V_{GS}=−1.5 V

6.2. Outline on parasitic elements and short channel effect

Gate length and gate width are two critical FET characteristics: a short and wide gate ensures higher performances. Nevertheless very small gate fabrication requires expensive and elaborate processes. In microwave electronics, little parasitic elements (i.e. gate resistance) cannot be neglected because of their device performances influence. Gate resistance can be considerable also if matched with gate-source capacitance: they establish a RC filter at FET input that reduces device gain. With the introduction of multifinger gate structures and T shapes, such parasitic elements can be strongly reduces, even if not erased. Source contact resistance is often an annoying parasitic element as well because it introduces a negative feedback reducing FET gain

and it affects device input characteristics spoiling noise figure: a lot of structures, basically recessed gate based, have been implemented to minimize this kind of effects.

Source contact inductance is a parasitic component that mostly affects power amplifier introducing a *real* parameter for input impedance that increases reducing FET gain: a solution to the problem is often to fabricate *vias* to ground the source.

Parasitic capacitances are the main limitation to FET operative frequencies. Gate to source capacitance is mostly formed by Schottky junction and gate-channel respective capacitances. To find the right equilibrium between channel doping and resulting channel conductance in the main key for a perfect device operation. In saturation region, Schottky capacitance is completely assignable to gate to source area and a shift toward source electrode is often suggested in order to minimize such a parasitic effect, increasing also gate to drain breakdown voltage.

As already said, a short and wide gate ensures higher performances: a device is considered to be short when the channel length is the same order of magnitude as the depletion-layer widths (x_{dD}, x_{dS}) of the source and drain junction. Nevertheless, as the channel length L is reduced to increase both the operation speed, and however obviously the number of components per chip, the so-called short-channel effects arise. Short-channel effect is an effect whereby a FET behaves differently from expected FETs operations. Such a effect can be attributed to two physical phenomena: the limitation imposed on electron drift characteristics in the channel and the modification of the threshold voltage due to the shortening channel length.

In particular five different short-channel effects can be distinguished:

*a) drain-induced barrier lowering and punch-through*when the depletion regions surrounding the drain extends to the source, so that the two depletion layer merge (i.e., when $x_{dS}+x_{dD}=L$), punch-trough occurs. Punch-through can be minimized with thinner oxides, larger substrate doping, shallower junctions, and obviously with longer channels. The current flow in the channel depends on creating and sustaining an inversion layer on the surface. If the gate bias voltage is not sufficient to invert the surface ($V_{GS}<V_T$), the carriers in the channel face a potential barrier that blocks the flow. Increasing the gate voltage reduces this potential barrier and, eventually, allows the flow of carriers under the influence of the channel electric field. In small-geometry FETs, the potential barrier is controlled by both the gate to source voltage V_{GS} and the drain to source voltage V_{DS}. If V_{DS} is increased, the potential barrier in the channel decreases, leading to drain-induced barrier lowering (DIBL). The reduction of the potential barrier eventually allows electron flow between the source and the drain, even if the gate-to-source voltage is lower than the threshold voltage. The channel current that flows under this conditions ($V_{GS}<V_T$) is called the sub-threshold current.

b) surface scattering: as the channel length becomes smaller due to the lateral extension of the depletion layer into the channel region, the longitudinal electric field

component E_y increases, and the surface mobility becomes field-dependent. Since the carrier transport in a FET is confined within the narrow inversion layer, and the surface scattering (that is the collisions suffered by the electrons that are accelerated toward the interface by E_x) causes reduction of the mobility, the electrons move with great difficulty parallel to the interface, so that the average surface mobility, even for small values of E_y, is about half as much as that of the bulk mobility.

c) velocity saturation: The performance short-channel devices is also affected by velocity saturation, which reduces the transconductance in the saturation mode. At low E_y, the carriers drift velocity v_d in the channel varies linearly with the electric field intensity. However, as E_y increases above 10^4 V/cm, the drift velocity tends to increase more slowly, and approaches a saturation value of $v_{d(sat)}=10^7$ cm/s around $E_y=10^5$ V/cm at 300 K. Note that the drain current is limited by velocity saturation instead of pinch-off. This occurs in short channel devices when the dimensions are scaled without lowering the bias voltages. Using $v_{d(sat)}$, the maximum gain possible for a FET can be defined as $g_m=WCv_{d(sat)}$.

d) impact ionization: it occurs due to the high velocity of electrons in presence of high longitudinal fields that can generate electron-hole pairs by impact ionization, that is, by impacting on substrate material atoms and ionizing them. Normally, in a nFET, most of the electrons are attracted by the drain, while the holes enter the substrate to form part of the parasitic substrate current. Moreover, the region between the source and the drain can act like the base of an npn transistor, with the source playing the role of the emitter and the drain that of the collector. If the aforementioned holes are collected by the source, and the corresponding hole current creates a voltage drop in the substrate material of the order of 6V, the normally reversed-biased substrate-source pn junction will conduct appreciably. Then electrons can be injected from the source to the substrate, similar to the injection of electrons from the emitter to the base. They can gain enough energy as they travel toward the drain to create new electron-hole pairs. The situation can worsen if some electrons generated due to high fields escape the drain field to travel into the substrate, thereby affecting other devices on a chip.

e) hot electrons: high energy electrons can enter the interface layer, where they can be trapped, giving rise to oxide charging that can accumulate with time and degrade the device performance by increasing V_T and affect adversely the gate's control on the drain current.

6.3. MESFET model

MESFET large signal model can be obtained from physical structure of such a device (Fig. 30). Figure 31 and 32 present small signal and large signal models and the relationships between physical structure and circuit elements. Small signal model is a

direct consequence of large signal model and it holds true up to more than ten gigahertz. Such a model can be split in two parts related to device intrinsic and extrinsic parameters respectively. Intrinsic parameters characterize device active area and depend on bias conditions while extrinsic ones can be roughly related to fabrication technology.

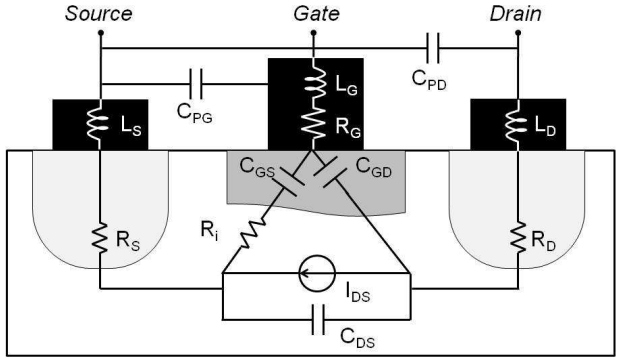


Figure 30 – Schematic MESFET model parameters origin

✓ R_G, R_S and R_D are the gate, source and drain resistances respectively and belong to model extrinsic section. R_D and R_S regard the ohmic contact resistance at the metal-semiconductor interface and other resistances between bulk and FET conductive channel. On the other hand, R_G is the metal resistance of gate Schottky contact. All these resistance values are in the order of few ohms.

✓ L_G, L_S and L_D are due to the contact pads inductances. In short channel FETs, gate inductance L_G is typically greater than the others, although it depends on device layout.

✓ R_i is the semiconductor resistance beneath the gate electrode, between source contact and conductive channel.

✓ C_{DS} is the drain to source capacitance, controlled by device geometrical parameters and usually considered as a constant.

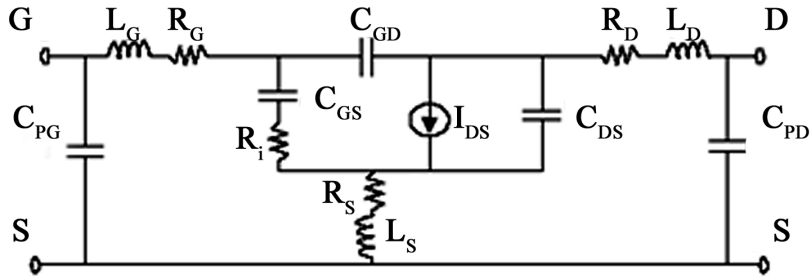


Figure 31 – MESFET small signal model

✓ C_{GS} and C_{GD} are channel capacitance, typically non linearly dependent on applied voltages. They model the space charge effect in the depletion region when gate to source and gate to drain voltages vary respectively. Keeping in to account capacitance

decreasing behavior when inverse bias increases in a Schottky junction, C_{GS} is noticeably greater than C_{DS}.

✓ I_{DS} is the controlled drain to source current.

✓ C_{PG} and C_{PD} are the gate and drain pads to source capacitance respectively. They depends on FET layout and they need particular off-devices structures to be extrapolated.

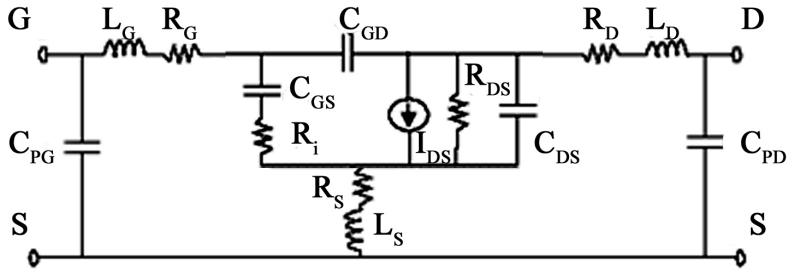


Figure 32 – MESFET large signal model

✓ g_m, named transconductance, is the I_{DS} variation increase dependence on input voltage V_{GS}. It is basically the slope of $I_{DS}(V_{GS})$ characteristic when V_{DS} is constant. Device transconductance is an indicative parameter for microwaves device performances.

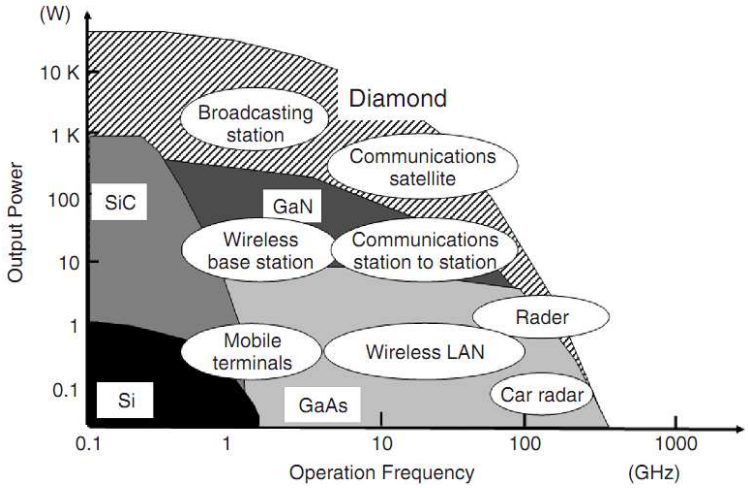
✓ R_{DS} describes the resistance between drain and source. It is often expressed in terms of output conductance $g_{DS}=R_{DS}^{-1}$, defined as the I_{DS} variation increase dependence on input voltage V_{DS} and so the slope of $I_{DS}(V_{DS})$ characteristic when V_{GS} is constant. Output conductance is an indicative characteristic for analogical operations because of its outstanding contribution to device maximum voltage gain and output impedance matching. Even if a low output conductance is suitable, it typically increases with gate length reduction.

7. Diamond based Transistors

7.1. Why diamond for power electronics?

New semiconductor technologies are currently in development in order to address the demanding requirements of the emerging telecommunication systems for devices able to operate in high frequency and high power range at the same time. For example, 120 W and 10 GHz are needed for communications satellites. Such performance is beyond the ability of conventional semiconductor devices, so these applications still rely on vacuum tubes. However, the power efficiency of vacuum tubes is quite low, because almost all of their input power is consumed as heat. Wide band gap semiconductors are the actual technological answer for the three fundamental requirements of emerging communication systems: high RF output-power density at more than 1 GHz , high energy efficiency in terms of power added efficiency (PAE)

and higher operation voltages with energy consumption as low as it is possible. Present days well-established technology of GaAs MESFETs largely used in base stations and radars offers about 1 W/mm for output-power density with a not negligible energy consumption.



Groundbreaking technology development of Gallium Nitride (GaN) seems to be the real step beyond for devices working in extreme conditions in terms communication satellites. However the extreme substrate cost and frailty added to the pestering self-heating effects shown by GaN based devices, encourages the research of alternative materials for applications in the same areas. Diamond is the widest band gap semiconductor (5.5 eV) and shows several physical properties that make it interesting for microwaves electronics. Already discussed very high breakdown electric field (10^7 V/cm), high carriers saturation velocity (10^7 cm/s) and mobility are advantages for high power applications: among all semiconductors diamond presents the best Johnson (J_{FoM}) and Keyes Figures of Merit[152,153], that could be easily related with available frequencies and expected RF output-power according to:

$$J_{FoM} = \left(E_{bd} v_{sat} / 2\pi\right)^2 \cong V_{MAX} \times f_{MAX}$$

Added to such promising characteristics, diamond presents the highest thermal conductivity: about 15 times larger than GaN and 50 than GaAs (see following table 4). These properties offer the possibility of realizing electronic devices with far superior performances regarding high frequency, power efficiency, power density, power loss, cooling and robustness in harsh environment. Owing to the potentiality of enabling high performance microwave power devices for RFICs, the technology of

diamond is currently receiving much interest for the fabrication of FETs with high cut-off frequencies and high output power.

Table 4 – Semiconductors Physical Properties

Material	Band gap	Thermal conductivity	E_b	Mobility	v_{sat}	ε_r
unit	*eV*	*W/cmK*	*10^6 V/cm*	*cm^2/Vs*	*$x10^7$ cm/s*	-
Diamond	5.5	20	10	2000	1.0	5.7
GaN	3.4	1.5	2.5	2000	2.5	8.9
SiC	3.27	4.9	3.0	1000	2.0	9.7
GaAs	1.42	0.55	0.4	8500	1.29	12.9
InP	1.34	0.68	0.5	5400	2.6	12.4
Si	1.12	1.5	0.3	1400	1.0	11.8
Ge	0.67	0.58	0.1	3900	1.0	16.2

7.2. Diamond transistors history

Even if diamond can be considered in its infancy as a semiconductor material, a wealth of proof-of-principle two-terminal and three-terminal devices has been fabricated and tested. Two-terminal diamond devices included the literature are *pn* diodes, UV emitting *pn* diodes, *p-i-n* diodes, various types of radiation detectors, Schottky diodes and photoconductive or electron beam triggered switches.

The first transistor action in diamond was reported by Prins[154] in 1982. He demonstrated a bipolar *npn* transistor made from natural p-type diamond. The n-type regions were created by carbon ion-implantation, creating zones with high defect concentration that exhibited *n*-type behavior (Fig. 33).

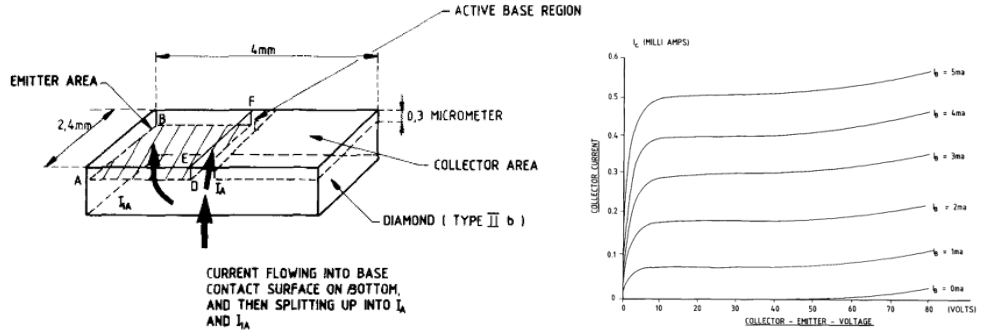


Figure 33 – First transistor action demonstrated on diamond by Prins in 1982[152]

However, it should be noted, that owing to the lateral geometry of the transistor, the current amplification factor h_F, the ratio of the collector current to the base current, is very low and equal to only 0.11. Prins supposed that this very low current gain was related to the fact that only the small junction area of 0.3 µm depth and 2.4 mm length, facing the similar sized area of the collector-base junction (Fig. 33), was involved in promoting transistor conduction between collector and emitter.

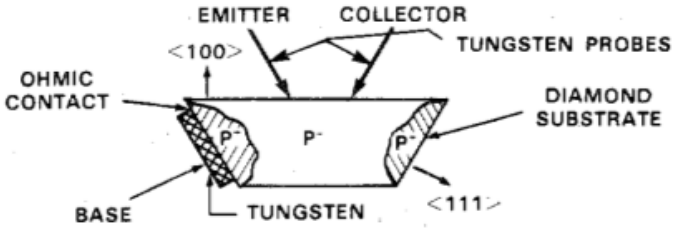


Figure 34 – Point contact transistor introduced by Geis in 1987[153]

More interesting for implementation in diamond are unipolar devices, such as MISFETs (metal-insulator-semiconductor field effect transistor), MESFETs (metal epitaxial semiconductor field effect transistor) and JFETs (junction field effect transistor). The experimental efforts in investigating such devices, however, have been largely focused on devices for RF applications. The development of diamond high-voltage/high-power devices poses some additional challenges since power devices require relatively large areas of near defect-free material. In addition, a high aspect ratio structure is necessary to allow for high forward currents.

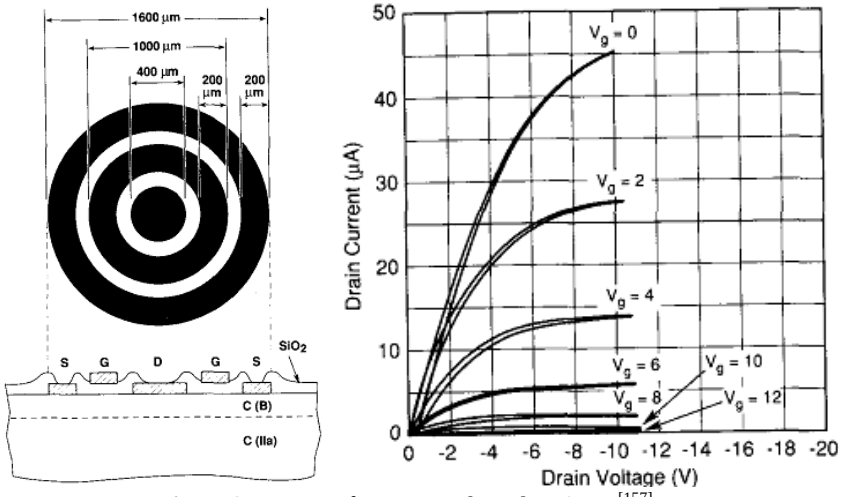


Figure 35 – Zeisse first ion-implanted MISFET[157]

The first transistor with significant gain was a point-contact transistor made by Gies[155] in 1987. Tungsten points were pressed against the surface of a synthetic

boron-doped diamond crystal, forming Schottky diode emission and collection regions in the bulk *p*-type base material (Fig. 34). At room temperature the small-signal current gain was about 20, decreasing to about 2 at an operating temperature of 783 K.

In 1989, Shiomi[156] reported MESFETs fabricated using boron-doped homoepitaxial diamond thin films. In 1991, Tsai[157] demonstrated tenfold modulation of the channel current in a MESFET. His device was made by rapid thermal processing using cubic boron nitride as a *p*-type dopant source. In the same year, Gildenblat[158] made the first diamond MISFET by deposition of silicon dioxide (SiO_2) onto a selectively grown homoepitaxial channel of boron-doped diamond.

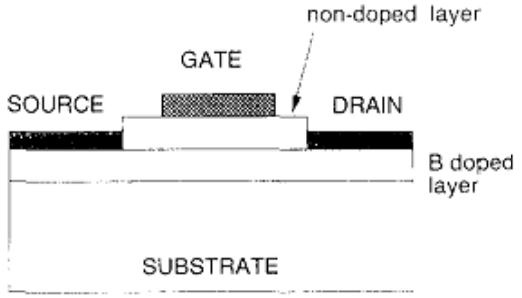


Figure 36 – Schematic of Fujimori first δ-doped-like transistor[159]

In 1991 as well, a p-type conducting layer has been formed in a substrate of semi-insulating natural diamond by boron implantation by Zeisse[159] (Fig. 35). It was the first reported use of ion implantation to fabricate a transistor on diamond. In that structure again, SiO_2 was deposited over conductive layer to make an insulated-gate field-effect transistor.

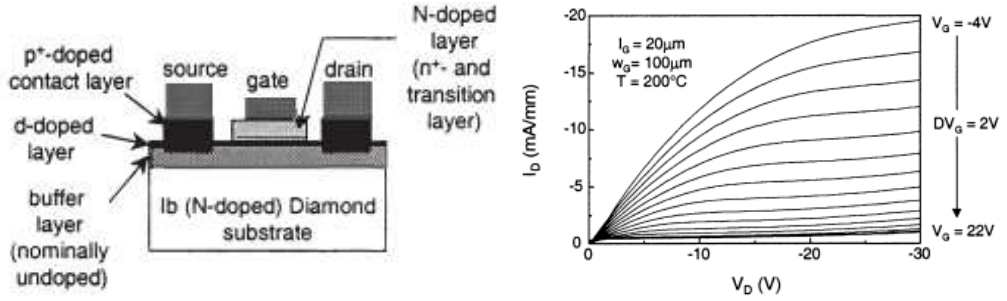


Figure 37 – Schematic of Aleksov δ-doped FETs with first remarkable characteristics[162]

The first demonstration of field effect transistors fabricated from polycrystalline diamond thin films was reported by Tessmer[160] in 1992. Ion implantation was employed to form a B-doped conducting surface channel, SiO_2 was used to form the gate dielectric structure and although the channel did not reach the pinch-off condition, modulation of the channel conductance was observed. In the same year, the first

δ-doped-like based transistor was demonstrated by Fujimori[161] (Fig. 36): this structure, having a non-doped layer between the gate electrode and the boron-doped layer, was fabricated using selective epitaxial growth, gate electrode was made of aluminum and the source and drain electrodes were made of tungsten. Such a device was found to have a tendency toward drain current saturation at room temperature even if it was still very far from an appreciable transistor effect evidence.

In 1995 and 1997, Shiomi[162] and Kohn[163] respectively, obtained preliminary successfully results for δ-doped diamond based transistor and 1999, Aleksov[164] fabricated δ-doped FETs with finally remarkable characteristics (Fig. 37), resulting in output currents up to 20 mA/mm.

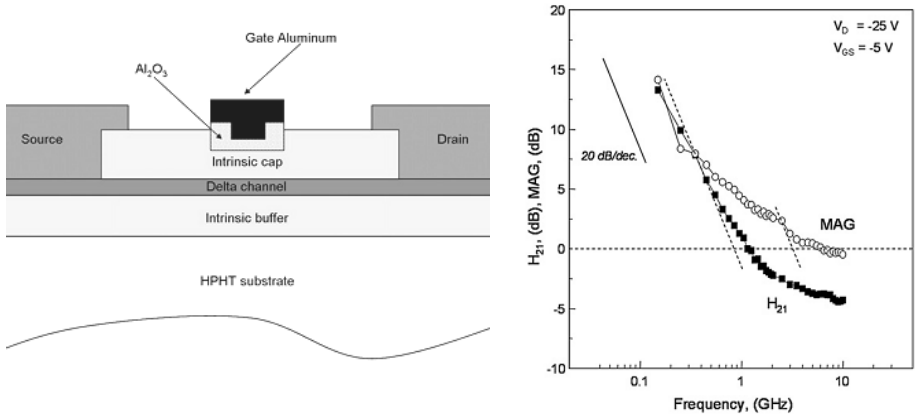


Figure 38 - El-Hajj δ-doped FET with an Al_2O_3 insulating layer recessed gate recess: f_T and f_{MAX} have been reported to be approximately 1 GHz and 3 GHz respectively[164]

In the last ten years a strong effort has been made by Kohn's Ulm University group in Germany together with Element Six Ltd. in order to improve δ-doped devices performance: in 2005 an in principle paper has been published by Denisenko[165], exhibiting the enormous potentiality of this technique and the collaboration first appreciable results, also in terms of RF performances, have been published in 2008 by El-Hajj[166] (Fig. 38). The δ-doping concept has been applied to a diamond field effect transistor structure with a gate recess with Al_2O_3 insulating layer, resulting in full channel carrier activation at room temperature and channel current modulation with complete pinch-off: a channel current density of more than 30 mA/mm and f_T (current gain cut-off frequency) and f_{MAX} (maximum available gain cut-off frequency) of approximately 1 GHz and 3 GHz respectively has been obtained with semi-enhancement mode operation.

The very hard process for δ-doped substrates fabrication, the lack of expectations comparable results and the impossibility, at the moment, to obtain a sharp doping profile, have slow down the research effort in this technique, and many involved groups have turned to hydrogen terminated surface MESFETs technology.

7.3. Hydrogen Terminated Diamond FETs

After the astonishing and revolutionary discovery of Landstrass and Ravi[109,110] in 1989 (see section 4.4), a new concept of active device has been assumed to be fabricated on diamond and such hydrogen terminated surface based FETs were pioneered by Kawarada[167]. For the first time, the transistor operation was based on the control of surface *p*-type conduction of a hydrogen terminated layer and boron doping was not used for the conduction. An aluminum contact was used for the Schottky gate and gold ohmic contacts were used for the source and drain (Fig. 39). Kawarada obtained transconductance of 200 μs/mm with a 10 μm gate length that was the highest value ever reported for diamond: it opened an alternative way for fabrication of high frequency and high power field effect transistors on diamond.

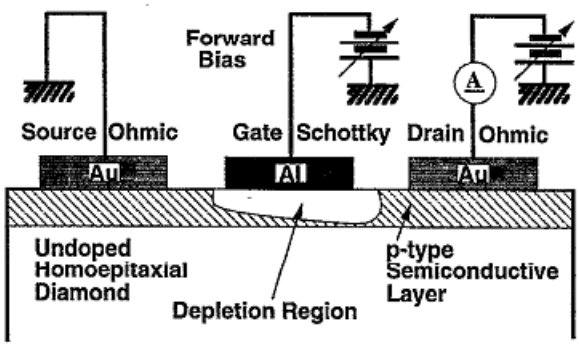


Figure 39 – Schematic of first hydrogen terminated diamond based MESFET by Kawarada[167]

Two different concepts of hydrogen terminated diamond based FETs with different gate structures have been studied in late 90s. In the first structure, the gate metal was evaporated directly onto the H-terminated diamond surface[167,168,169]. In the other, it was evaporated on a thin insulator layer on H-terminated diamond surface [170,171,172]. The first structure is MESFET and the latter structures are called a MISFET. In the latter, thin insulator layers, CaF_2[170,171,172] and Al_2O_3[173], have been used. Also MOSFET structure has been proposed using SiO_x as gate oxide[174]. MISFETs with a CaF_2 insulator layer show a large drop in RF current due to deep traps in the insulator layer[172] and therefore do not seem suitable as RF power devices. However, even for the first structure, the electrical properties show MISFET-like behavior, rather than MESFET behavior.

First worthy of remark demonstration of RF performances for hydrogen terminated diamond based MESFETs has been reported in 2001 by Taniuchi[175]. Cu was used for the fabrication of a 2 μm gate-length MESFET on a hydrogen terminated diamond with a carriers mobility of approximately 40 cm^2/Vs, showing transconductance g_m of 70 mS/mm and f_T and f_{MAX} of 2.2 GHz and 7 GHz respectively. In 2002, the same

group[176,177] improved such promising results with a MISFET structure, using a CaF2 insulating layer for a 0.7 µm gate-length electrode and obtaining g_m of 100 mS/mm and maximum drain to source current of about 160 mA/mm: cut-off frequencies of 10 GHz and 17 GHz for f_T and f_{MAX} respectively have been reported. For the reasons explained above, MISFET structure, except for few unremarkable works on nanocrystalline and black diamond, has been abandoned. Between 2002[178] and 2004[179], Aleksov and Kohn's group at Ulm University in Germany reported in two main papers, the summary of their studies, already exposed in some conferences[180,181], on RF small and large signals performances: 0.2 µm gate-length MESFETs fabricated on a homoepitaxial hydrogen terminated diamond layer (with a carriers mobility of 150 cm^2/Vs) resulted in a maximum current gain cut-off frequency f_T of 25 GHz and a f_{MAX} of 63 GHz, achieving a saturated output power density of 0.35 W/mm at 1 GHz. The author's group, *S²DEL* (Solid State and Diamond Electronics Lab), is active in this context since 2006[182] obtaining encouraging results: on homoepitaxial diamond grown by Marinelli's group in Tor Vergata Univerisity laboratories in Rome, a 4 µm gate-length MESFET results in a f_T of 0.8 GHz and f_{MAX} of 2 GHz[183] while for polycrystalline diamond, a 0.35 gate-length device achieved approximately 1 GHz and 5 GHz for f_T and f_{MAX} respectively, both on commercial available substrate[184] and Russian Academy of Science small grain size developed diamond[185].

7.4. State of Art

DC and RF higher performances regarding H-terminated surface diamond based MESFETs have been achieved by Japanese groups of H. Kawarada at Waseda University on homoepitaxial diamond and of M. Kasu at NTT Basic Research Laboratories on polycrystalline diamond. Here the author reports and briefly discusses a review of best results taken from literature.

7.4.1. MESFETs technology

Figure 40 shows a schematic cross-section of an H-terminated diamond FET fabricated by the University of Ulm and NTT[189]. In this case, a T-shaped gate with a length of 0.2 µm was fabricated by using electron-beam lithography. The T-shape can reduce gate resistance in RF and increase the cut-off frequency.

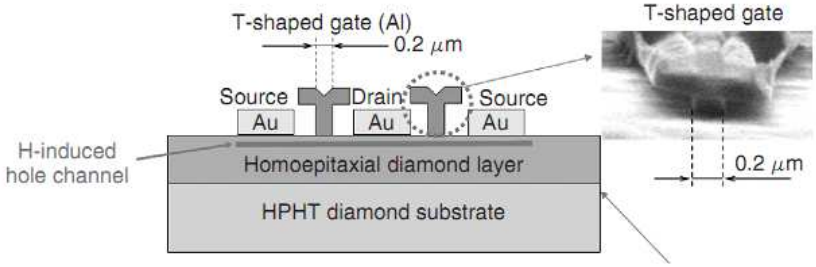


Figure 40 – MESFET schematic structure developed by Kasu at NTT laboratories

In this structure, Au is used for ohmic contacts fabrication and it is directly deposited on hydrogen terminated surface. Al is instead used for Schottky contacts. Gate electrode is typically fabricated with the self aligned technique, in order to obtain a drain to source resistances and capacitances reduction. Further mentionable improvements have been implemented by Waseda University group, successfully using TiC ohmic contats and later hydrogenation technique[193] (Fig. 41).

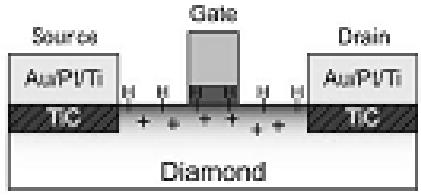


Figure 41 – MESFET schematic structure developed by Kawarada's group at Waseda University

Recently, Kueck published his results about the passivation of FETs by using Al_2O_3 and AlN deposited by Atomic Layer Deposition (ALD)[194,195], with a negligible reduction of performances, opening the road to a better understanding of channel properties, reliability and stabilization of diamond FETs (Fig. 42).

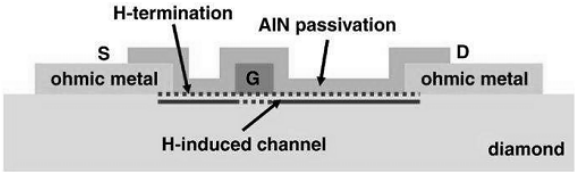


Figure 42 – MESFET schematic structure developed by Kueck and Kohn at Ulm University

In this structures, also a boron doped layer has been used beneath Au for the fabrication of very low resistance ohmic contacts[196] and a first test of field plate implementation has been carried on[194]. Interesting examination by Kohn's group, point out the possibility of keep only a small part of hydrogen terminated surface under the Au layer in order to improve the mechanical adhesion of metal upon the substrate surface[195]. It is very important to remark how Kohn's group, after a long period of studies upon δ-doped diamond FETs with Element Six Ltd., is now fabricating again surface channel MESFETs on hydrogen terminated surface.

In conclusion, author would like to mention the fabrication by Glasgow University of the smallest diamond FET with a gate length of 50 nm[197] (Fig. 43).

7.4.2. DC Characteristics

In 2010, the maximum value for drain to source current I_{DS} has been reported by Hirama[186]. Such a great result cannot be discussed without mentioning the speculation that involved Kawarada's group in the last decade about the contribution of the diamond substrate crystallographic orientation to devices perfromances.

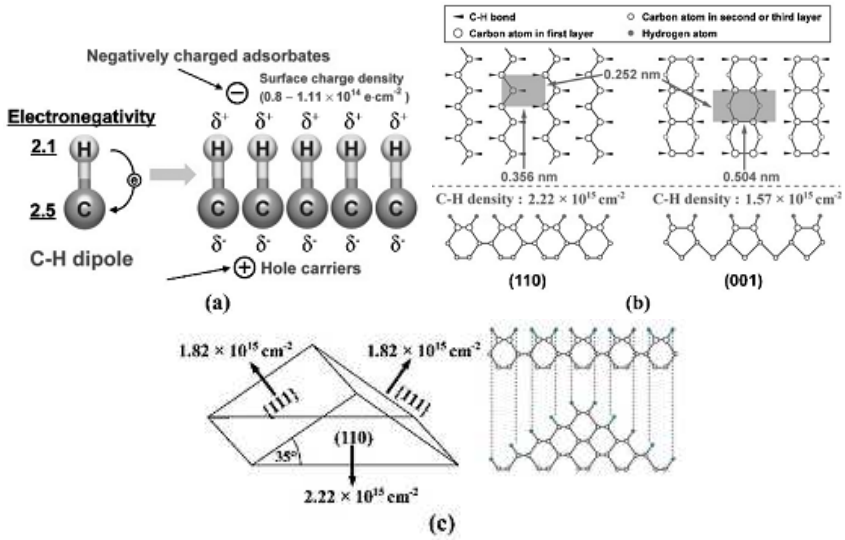


Figure 43 – a) Spontaneous polarization model for hole accumulation layer. b) Top and cross-sectional views of H-terminated (001) and (110) surfaces. c) (111) faceted pits on (110) diamond surface. The H-terminated (111) surface exhibits 1×1 geometry, and the C–H bond density is 1.82×10^{15} cm^{-2}.

In the summary[187] of such a speculation, he found that the hole carrier density of the hole accumulation layer depends on the orientation of the hydrogen terminated diamond surface, for which (110) preferentially oriented films show 50%–70% lower sheet resistance than a (001) substrate so he proposed the spontaneous polarization model: hole density of the surface accumulation layer is proportional to the C–H bond density on the surface.

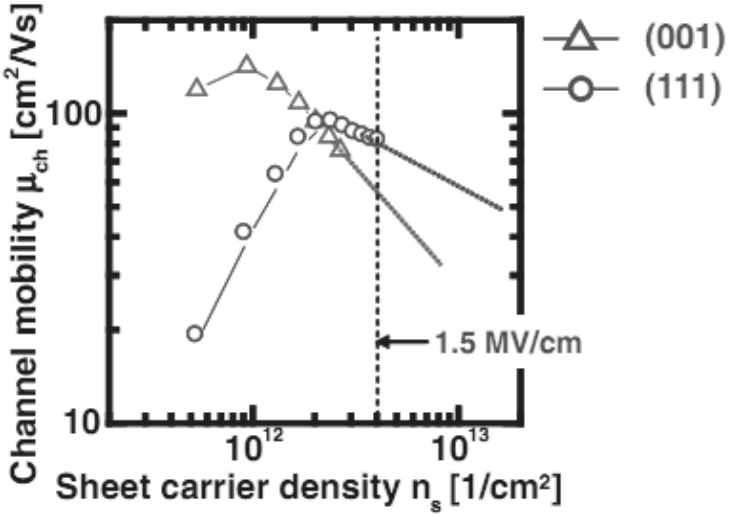


Figure 44 - Sheet carrier concentration dependence of channel mobility on (001) and (111) diamond surfaces.

In this model, the C–H dipole is indispensable for the accumulation of holes. The effective electric surface charge density due to the C–H dipole density is 1×10^{14} cm^{-2}, which provides the sites for negatively charged adsorbates on the surface. Through the enhancement of hole accumulated density near hydrogen-terminated (111) diamond surfaces, low sheet resistance (5 kΩ/sq) has been obtained compared with commonly used (001) diamond surfaces (10 kΩ/sq). Using the hole accumulation layer channel, a high drain current density of 850mA/mm was obtained in *p*-channel transistors. The high drain current on the (111) surface is attributed to two factors: the low source and drain resistances owing to the high hole carrier density n_s and the high channel mobility μ_{ch} at a high gate–source voltage on the (111) surface compared to standard (001) oriented surface (Fig. 41). μ_{ch} on the (111) and (001) surfaces at room temperature have been evaluated to discuss the high I_{DSmax} on the (111) diamond surface. In the low n_s region, μ_{ch} increases with n_s. In addition, μ_{ch} decreases with n_s in the high n_s region. This tendency is similar to that of silicon MOSFETs.

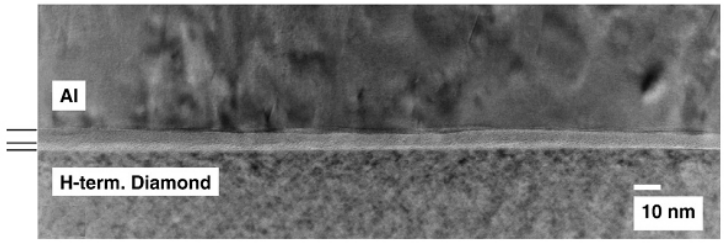


Figure 45 - Cross-sectional transmission electron microscopy (TEM) images of hydrogen-terminated field-effect transistor gate region (Al on H-terminated diamond)

It is worth to notice that Kawarada considers such a device as a metal-oxide-semiconductor FET (MOSFET), because of the spontaneous oxidation of the first 30 nm of deposited aluminium gate electrode. This theory finds a strong confirmation in a study from Kasu about an interfacial layer formation between thermal evaporated aluminium and diamond hydrogen terminated surface[188], layer that is not present under Au ohmic contacts.

The 0.3 µm gate length diamond MOSFET fabricated on H-terminated (111) surface exhibited I_{DS}-V_{DS} characteristics with excellent current saturation and pinch-off characteristics. The I_{DSmax} and transconductance (g_m) are 850 mA/mm and 160mS/mm, respectively (Fig. 43). This I_{DSmax} is, up to now, the highest value for diamond FETs. As already said, one of the reasons for the high I_{DSmax} of 850 mA/mm is the low sheet resistance on the H-terminated (111) surface.

On the other hand, for polycrystalline diamond, the maximum obtained drain current has been reported by Kasu[189] with a I_{DSmax} of 550 mA/mm (Fig. 44) corresponding to a maximum transconductance of approximately 150 mS/mm. Two interesting studies by Kubovic and Kasu[190,191] demonstrate the possibility of

increasing sheet carriers density by surface exposition to NO_2 gas and subsequently molecules absorption.

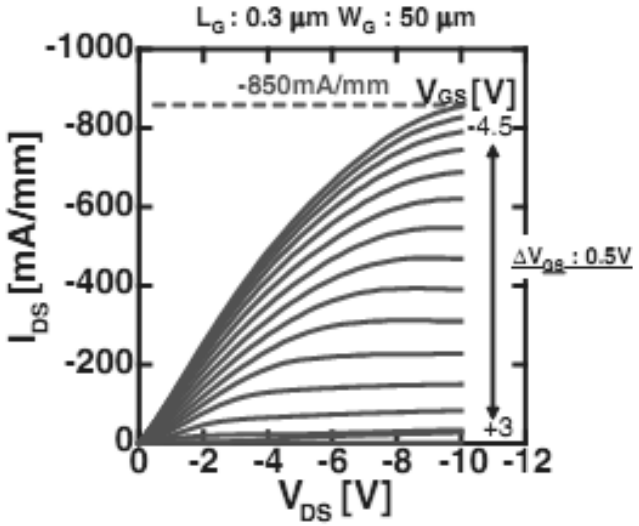


Figure 46 - I_{DS}–V_{DS} characteristics of 0.3 µm-gate-length FET on the (111) single crystal diamond surface

Output characteristics obtained by Kasu on result from a homoepitaxial layer grown above a polycrystalline substrate supplied by Element Six Ltd. Such a very high quality layer ensures a scattering phenomena reduction and a higher holes concentration. In fact, in the bulk, the diamond layer contains residual impurities that result in bulk conduction. In FETs operation, both the bulk and the surface conduction occur in parallel. From the environment, adsorbates adsorb on the surface and influence the surface conduction.

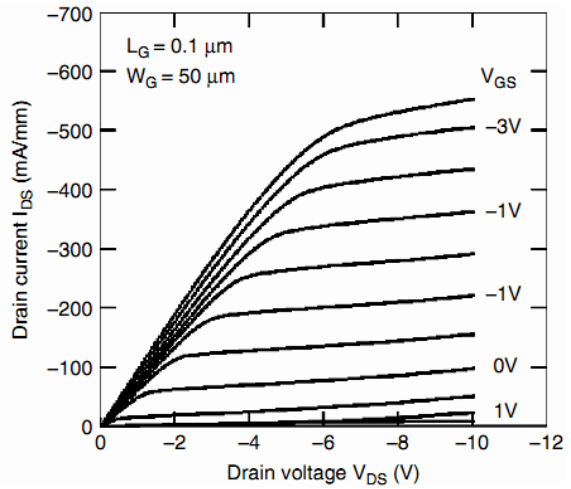


Figure 47 - I_{DS}–V_{DS} characteristics of 0.1 µm-gate-length FET on the polycrystalline diamond surface

Few boron impurities unintentionally residual in the bulk result in a high buffer leakage and short channel effects. That is why, even in reverse bias conditions, it is possible sometimes to find remarkable drain currents.

The contacts resistivity ρ_C, both for single crystal and polycrystalline diamond, is reported to be in the order of 1×10^{-5} Ωcm^2[189] and the very high on-resistance, approximately 250 Ω, can be easily reduced by implementation of ultrashallow TiC contacts with the re-hydrogenation technique ($\rho_C=2.7\times10^{-7}$ Ωcm^2)[192] or by fabrication of DLC/Pt/Au contacts (approximately 10^{-6} Ωcm^2)[193].

7.4.3. RF performances

RF performances are typically evaluated by the analysis of scattering parameters. Scattering parameters (or S-parameters) describe the electrical behaviour of linear electrical networks when undergoing various steady state stimuli by electrical signals. Each 2-port network presents S-parameter described as follow:

S_{11} is the input port voltage reflection coefficient,

S_{12} is the reverse voltage gain,

S_{21} is the forward voltage gain,

S_{22} is the output port voltage reflection coefficient.

These parameters can be used to define other important parameters for the evaluation of RF characteristics and performances.

The Maximum Available Gain (*MAG* or G_{MAX}), described as the theoretical maximum power gain available in a transistor stage and it is seldom achieved in practical circuits because it can be approached only when feedback is negligible, is defined as:

$$MAG = \frac{|S_{21}|}{|S_{12}|}\left(K - \sqrt{K^2 - 1}\right)$$

Where K is the Rollet' stability factor, a way of demonstrating unconditional stability achieved when $K>1$ and $|\Delta|=S_{11}S_{22}-S_{12}S_{21}<1$.

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{21}S_{12}|}$$

The maximum stable gain (*MSG*) is instead defined as G_{MAX} with $K=1$ and therefore $MSG=|S_{21}|/|S_{12}|$.

Unilateral power gain (U) is the gain that would be achieved if the transistor were "unilateralized" (feedback set to zero) and conjugately matched.

$$U = \left\{\frac{1}{2}\left|\frac{S_{21}}{S_{12}} - 1\right|^2\right\} \Big/ \left\{K\left|\frac{S_{21}}{S_{12}}\right| - Re\left(\frac{S_{21}}{S_{12}}\right)\right\}$$

Power Gain (G_P) is the tuned gain of a device when the output is presented with the appropriate load-line Γ_L to produce some specified output power, and the input is matched for minimal reflection.

$$G_P = |S_{21}|^2 \frac{1 - |\Gamma_L|^2}{|1 - S_{22}\Gamma_L|^2}$$

In the end, the forward current gain $|h_{21}|^2$ is defined as:

$$|h_{21}|^2 = \left| \frac{2S_{21}}{S_{12}S_{21} + (1 - S_{11})(1 + S_{22})} \right|^2$$

Figure 48 shows the frequency dependence of the current gain $|h_{21}|^2$ and the power gains, the maximum stable gain (*MSG*) maximum available gain (*MAG*) ratio and the unilateral power gains (*U*).

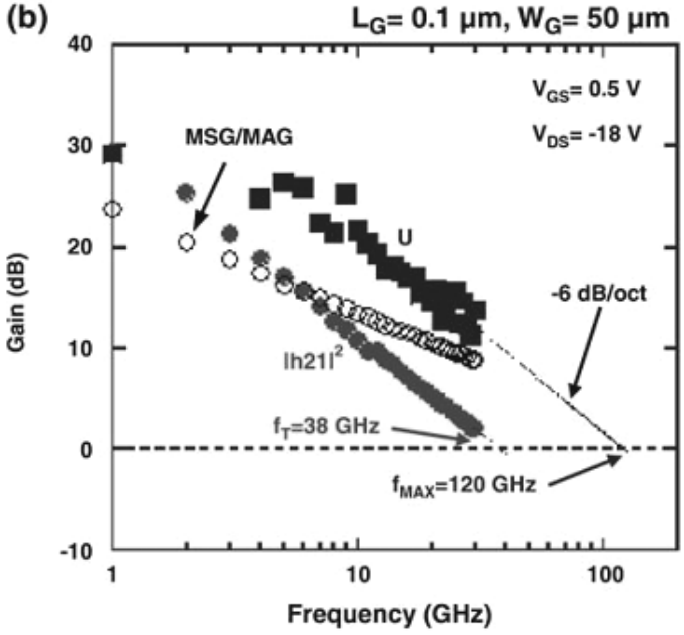


Figure 48 – Small Signal Performances of Diamond MESFETs

The FET in figure is fabricated with a L_G of 0.1 µm and W_G of 50 µm. The cut-off frequency was extracted by the slope, −6 dB/oct, from the gain values at lower frequency, and the cut-off frequencies for current and power gains were obtained as 45 and 120 GHz, respectively[189]. The f_T value becomes the maximum near the pinch-off condition (I_{DS} becomes almost zero) [179], because C_{GS} drops faster than g_m. The f_{MAX} value increases with negative V_{DS}, because with negative V_{DS}, the depletion layer of the gate extends on the drain side and C_{GD} decreases. Another characteristics of H-

terminated diamond FETs is a high f_{MAX}/f_T ratio (~2.6), probably because of high drain conductance (the background resistance of diamond is extremely high). Figure 49 is the diamond-FET equivalent circuit extracted from an RF analysis [199].

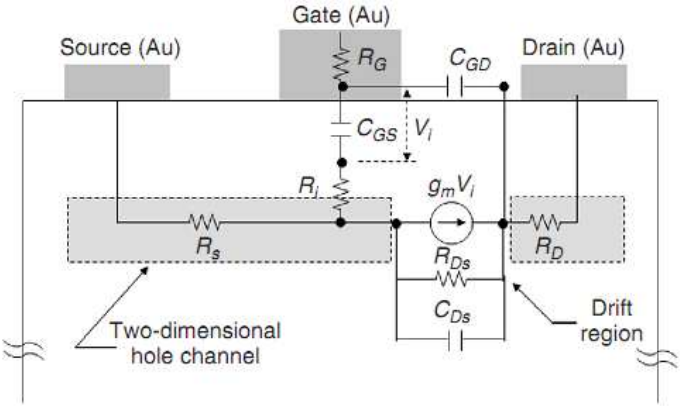


Figure 49 - Equivalent circuit of the H-terminated diamond FET.

Anyway, conclusively, it is important to mention that the reason why large-grain polycrystalline diamond FETs exhibit higher performance than (001) homoepitaxial diamond FETs is still not understood. Author hypothesis are related to the better adhesion of ohmic contacts on polycrystalline diamond and the following lower power consumption on the source electrode.

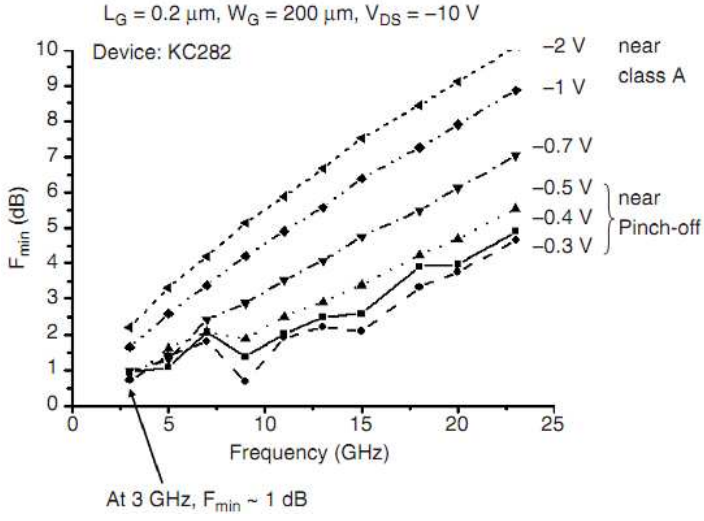


Figure 50 - The minimum noise figure (F_{min}) as a function of frequency. Near the pinch-off condition, the lowest F_{min} is obtained

Low-noise amplifiers (LNAs), characteristics of RF receivers front end, are qualified by the minimum noise figure, F_{min}: a small F_{min} means low noise generated from inside the device during amplification. In Figure 50, the F_{min} value seems to

increase linearly with frequency in the high frequency range[179] because of quantum noise. A value F_{min} of 0.72 dB at 3 GHz (I_{DS}=45 mA/mm) has been obtained at the bias point corresponding to that of the maximum f_T and f_{MAX} values. The F_{min} value (0.72 dB) is lower than Si MOSFET (0.88 dB at 2 GHz). Due to the high-impedance level at this bias condition, the optimum reflection coefficient Γ_{opt} had a very high magnitude of 0.951 and the noise resistance R_n was 151 Ω.

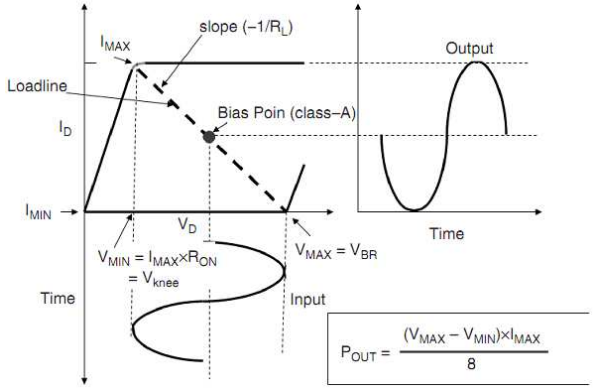


Figure 51 - Relationship between DC signal and RF output power in drain current–voltage characteristics.

Figure 51 explains how RF output power is extracted from the output (drain) voltage (V_{DS}) and current (I_{DS}). The high voltage and current result in high output power. The maximum voltage, V_{MAX}, is limited by the breakdown voltage V_{BR}, and the maximum current, I_{MAX}, is proportional to the product of the square of the maximum carrier concentration obtainable and the mobility.

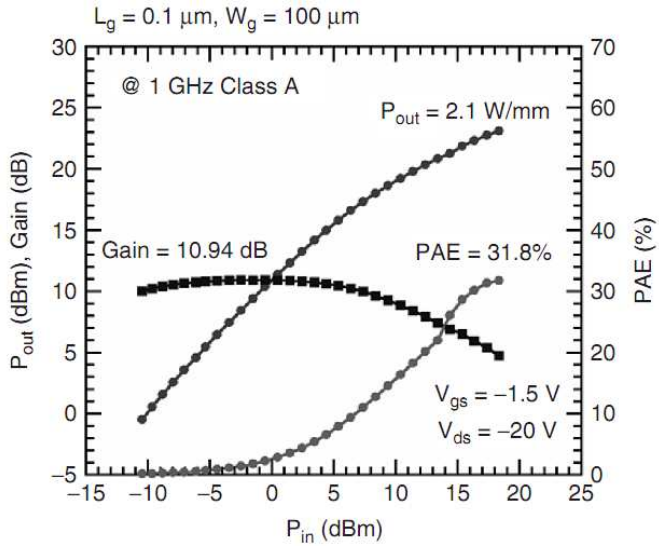


Figure 52 - RF input–output power characteristics measured at 1 GHz in Class A operation of ahomoepitaxial diamond FET.

When specific applied output voltage (V_O) and load resistance (R_L) are chosen, V_{DS} and I_{DS} change following the load-line as $V_{DS}=V_O - I_{DS}R_L$. The load-line intercepts V_O and a slope ($-1/R_L$). When the bias point is set at the middle point of I_{MAX} and V_{MAX} (Class A operation), the maximum RF output power is obtained without signal distortion. In Class A operation, the maximum output power is estimated as $P_{OUT}=[(V_{MAX}-V_{MIN})\times I_{D\_MAX}]/8$. If V_{MAX} is set at V_{BR} and V_{MIN} is set at V_{KNEE}, the knee voltage, at which I_{D_MAX} is obtained when the linear and saturation regions meet, P_{OUT} becomes the maximum (Fig. 51).

Figure 52 shows a RF power sweep at 1 GHz of a FET fabricated on single crystal diamond in Class A operation[200]. The maximum output-power density, P_{OUT}, is 2.1W/mm, and the power added efficiency (PAE) is 31%. The maximum power gain is 10.9 dB (12 times). This P_{OUT} is twice that of widely used GaAs MESFETs, about 1 W/mm[201]. The diamond FET structure is a very simple structure that does not use a field plate to weaken the maximum field between the gate and the drain contacts. The best results for RF power performance on polycrystalline diamond has been obtained by the author group[202] during this PhD thesis and will be discussed in the following. In contrast, the highest values reported for a GaN FET without and with a field plate are 10 W/mm at 30 V[203], and 32 W/mm at 120 V[204]. With a field plate and an optimized device configuration, the maximum RF output power of diamond FET with boron delta-doping is predicted to be 75 W/mm[165].

Chapter 2

In this chapter, diamond based MESFETs fabrication technology will be briefly exposed even if each step will be deeply discussed in order to justify and understand the different choices and techniques implemented to obtain a technological process as stable as possible. The entire process has been many times reiterated and each step has been investigated and analyzed during this three years work hence a lot of information has been obtained about the transistors behavior as well as on the hydrogen termination stability. Each step here reported can be considered as a summary of the technological improvement due to characterization results reading.

Most of this work has been carried on within the Solid State and Diamond Electronics Lab (*S^2DEL*) at the Electronic Engineering Department of Roma Tre University in collaboration with the National Council of Researches (CNR), in particular with the Institute of Photonics and Nanotechnologies (IFN) and the Institute of Inorganic Methodologies and Plasmas (IMIP).

Moreover, part of this thesis has been carried out in collaboration with Diamond Detectors Ltd. in Poole, UK, developing the implementation of their property contact patent with S^2DEL transistor technology. Interesting results of this collaboration will be shortly discussed.

1. MESFETs Fabrication Technology

Metal Semiconductor Field Effect Transistors developed during this work are a direct consequence of S^2DEL past studies and this PhD thesis represents a summary of the technology improvement.

Basically, two main technique has been implemented for gate electrode fabrication: self aligned technique and what we will call "standard" technique, consisting in a fixed drain to source channel distance definition. Besides, first devices was fabricated using a GaN oriented transistor layout supplied by *SELEX Sistemi Integrati* in a previous collaboration, then such a layout has been modified and improved for diamond characteristics by means of microwave devices dedicated software.

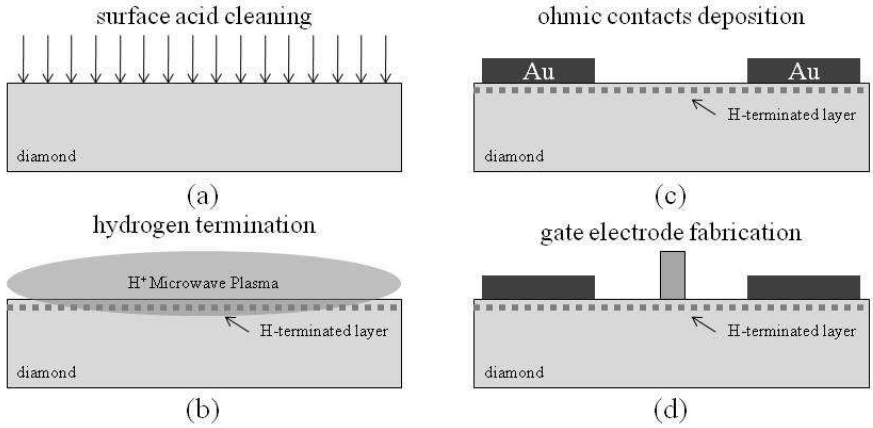


Figure 53 – Schematic of MESFETs fabrication steps

The fabrication process is schematically outlined in figure 53. After acid surface cleaning (*a*), diamond sample surface is hydrogen terminated by means of a microwaves plasma treatment (*b*). Hence, ohmic contacts (*c*) and schottky gate electrode are fabricated (*d*). Evidently, there are not only the four schematically represented steps because each one presents different conceptual issues due to fabrication techniques. In the following sections the processes involved in diamond MESFETs technology will be discussed.

2. Diamond Samples

Diamond samples used during this PhD thesis has been supplied by General Physics Institue of Russian Academy of Science (RAS) in Moscow, within a scientific collaboration with Prof. Viktor Ralchenko, and purchased by Element Six Ltd in UK. In the following, Russian Academy of Science custom made samples and Element Six Ltd. commercial available diamond substrates will be indicated as RAS and E6 respectively.

RAS Diamond substrate are grown by Microwave Plasma CVD (see section 3.2) by means of a custom reactor developed jointly with *Optosystems Ltd.* (www.cvd-diamond.ru), DF-100 model with microwave power up to 5 kW at 2.45 GHz (Fig. 54).

Typical growth conditions for polycrystalline films, are:

- ✓ Gas composition: (1-5%) CH_4/H_2
- ✓ Pressure: 100-160 Torr
- ✓ Flow rate: 500-1000 sccm
- ✓ Substrate temperature: 700-900ºC
- ✓ Substrate diameter: 50-75 mm
- ✓ Growth rate: 1-9 µm/hour

Polycrystalline substrates grown in these conditions on a Si wafer upon a Mo substrate holder, typically presents a columnar structure (Fig. 55a) and the growth side is lapped and polished in order to obtain a surface roughness of 2-8 nm (Fig. 55b): cast-iron wheel for polishing is charged with 20-28 µm diamond powder and rotates at 3000 rpm speed.

Figure 54 - CVD reactor DF-100 developed by GPI-RAS and *Optosystems Ltd*

The high quality of such polycrystalline diamond samples is pointed out by the extremely narrow Raman's peak (Fig. 56a) and the low impurities concentration

(Fig.56b). The average grain size is 100-200 µm in diameter and typical dimensions are 8×8 mm^2 of surface for a 200-500 µm thickness.

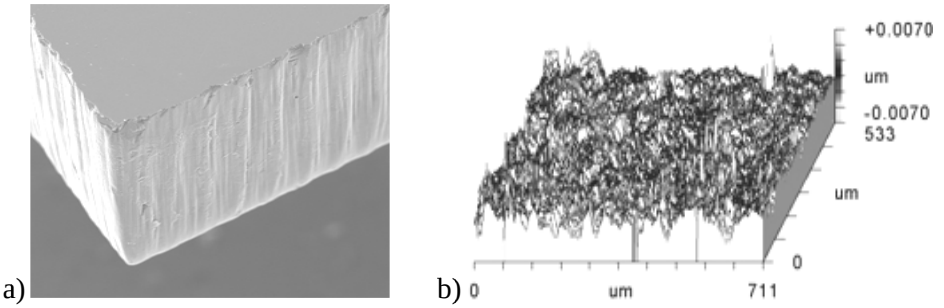


Figure 55 – Scanning Electron Microscopy (SEM) picture of a polycrystalline diamond by RAS (a) and its surface roughness profile (b)

Overall Nitrogen impurities change between 5×10^{17} and 2×10^{18} cm^{-3} while thermal conductivity is estimated to be 21 W/cmK at room temperature[205].

Recently, General Physics Institute developed 0.1-1 µm thick homoepitaxial layer grown on highly polished HPHT commercial substrates. Growth rate is approximately between 0.5 and 3 µm/hour, surface roughness around 6-8 nm and (110) and (100) crystallographic orientation. Preliminary characterization results of characterization point out the high quality of these samples.

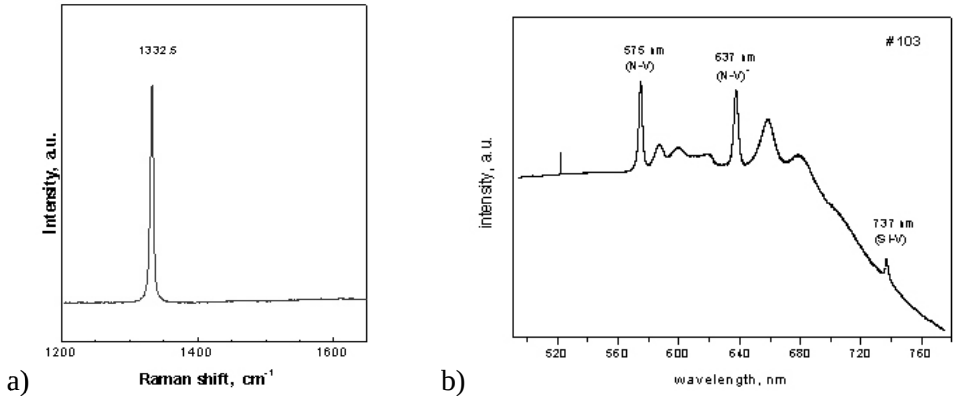


Figure 56 – Raman's peak (a) and impurities concentration (b) for RAS diamond

Polycrystalline and Single Crystal diamond directly purchased by Element Six Ltd. (www.e6cvd.com) are synthesized with a microwave plasma assisted CVD reactor operating at a frequency of 2.45 GHz, the main diamond synthesis route that has been developed and refined by the company. No information about growth process are available, Element Six Ltd. never published papers or deposited patents about growth conditions as well as only few information about quality of samples have been declared.

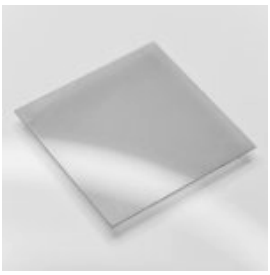
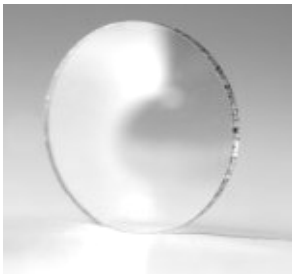
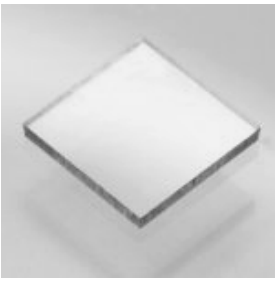
a)  b)  c) 

Figure 57 – Different diamond grades by Element Six Ltd: a) Thermal Management Grade, b) Optical Grade, c) Single Crystal Plate

Element Six diamond samples used for MESFETs fabrication in this thesis are of three different quality: thermal management grade, optical grade and standard single crystal diamond plates.

Thermal Management Grade diamond sample dimensions are 10×10 mm^2 for a 250 µm thickness. Thermal conductivity (Fig. 57a) is 18 W/cmK and declared surface roughness is less than 50 nm. Grain size is quite variable (average can be considered around 100 µm for diameter) and the two faces surface is extremely different (it presents both growth side and nucleation side as well). Spectral photoconductivity of this sample typology shows the presence of many defects under the gap and a wide Urbach tail (not shown). Such a sample has been often used essentially because of its low cost and so easy availability. Optical grade polycrystalline CVD diamond (Fig. 57b) ensures broad transparency, durable and wear resistant, it is basically suitable for use in IR and high power laser optics. It comes with a circular shape with 8 mm diameter for a 500 µm thickness. Thermal conductivity is declared to be more than 19 W/cmK for a less than 30 nm surface roughness. Single crystal diamond plates (Fig. 57c) are 500 µm thick for 4.5×4.5 mm^2 grown upon HPHT substrate even if it comes as an entire CVD sample (laser cut). The crystallographic orientation is (100) for Ib grade: Element Six declares less than 1 ppm and less than 0.05 ppm for Nitrogen and Boron impurities respectively. Thermal conductivity is not declared but it is plausibly around 20 W/cmK. Surface roughness is less than 30 nm.

3. Surface cleaning

Surface cleaning is obviously a nodal point for micro and nanotechnologies. Most of the mainly diffused solutions for semiconductors cleaning are oxidant and so they cannot be used for H-terminated surface because of the hydrogen extreme ease to oxygen linking. On the other hand, also reactive ion etching (RIE) is often oxidant and it cannot be applied to H-terminated surface. Here I report the methods used for surface cleaning during this PhD thesis.

As grown diamond surface, after polishing process, is called “clean” surface. It naturally tends to oxidation. This oxidized surface can be clean with a lot of acid solutions without damaging it. Such solutions are important for residual metallization removing and graphitic layers due to annealing or other processes deleting. Typical surface cleaning process is composed of n steps:

1. *Sulphochromic* solution, an aggressive mixture of $K_2Cr_2O_7$ and H_2SO_4 useful for its corrosive power to remove metals. About five minutes boiling is often enough to remove most of metals.
2. *Aqua regia*, another highly corrosive, fuming yellow or red solution, also called nitro-hydrochloric acid. The mixture is formed by mixing nitric acid HNO3 and hydrochloric acid HCl in a molar ratio of 1:3 respectively. It was named so because it can dissolve noble metals like gold and platinum.
3. *RCA clean*, standard cleaning steps for silicon industry developed by Werner Kern in 1965 while working for RCA, the Radio Corporation of America. It three steps:
   a) Organic Clean, performed with a 1:1:5 solution of NH_4OH , $H_2O_2$and H_2O at 80 °C for 10 minutes. This treatment results in the formation of a thin oxide layer that shall be removed in subsequent steps.
   b) Oxide Strip, a short immersion in a 1:50 solution of HF and H_2O at 25 °C, in order to remove the thin oxide layer and some fraction of ionic contaminants.
   c) Ionic Clean, performed with a 1:1:6 solution of HCl, H_2O_2 and H_2O at 80 °C. This treatment effectively removes the remaining traces of metallic (ionic) contaminants.
4. Any residual graphite or ion impurities are removed by the so-called “*Kalish*” cleaning solution, a mixture of HNO_3, $HClO_4$ and H_2SO_4 (1:1:1).

During the period spent in UK at Diamond Detectors Ltd., another effective cleaning method has been learned and applied to diamond surfaces. Such a method directly comes from Element Six laboratories and involves H_2SO_4 and KNO_3. A beaker containing 10 cl of H_2SO_4 is heated up to 300°C with an hot plate until it begins to give off white fume. When the solution is fuming, the KNO_3 is added to the beaker, a spatula-full at a time to a suggested ratio(10 g to 100 ml). The solution turns a bright yellow-orange colour and will bubble gently. After approximately 10 minutes of heating, diamond samples have to be washed with de-ionized water into an ultrasonic bath for approximately 15 minutes.

Hydrogen terminated diamond surface, as already said, cannot be cleaned with the previous reported oxidant method. This is a further reason, in addition to small dimensions, why H-terminated diamond technology can be considered difficult. However, it is possible to use few industrial solvents: acetone, trichloroethylene and isopropyl acid. Acetone is the organic compound with the formula (CH3)2CO and it is used, in our case, for removing organic residual; its operation can be improved heating

it or by an ultrasonic bath. Trichloroethylene (TCE) is a chlorinated hydrocarbon commonly used as an industrial solvent for a variety of organic materials: its greatest use has been as a degreaser for metal parts. Isopropyl alcohol (also known with the abbreviation IPA) is a common name for a chemical compound with the molecular formula C_3H_8O and like acetone, it dissolves a wide range of non-polar compounds while it is also relatively non-toxic and evaporates quickly; thus it is widely used as a solvent and as a cleaning fluid, for dissolving lipophilic contaminants such as oil essentially (i.e. cleaning electronic devices, magnetic tape and lenses of lasers in optical disc drives).

Aqua Regia at room temperature for 10 minutes has been also tested as a solvent for H-terminated surface and experimental evidences point out conductivity persistence after such a process. Trials have been run as well with a solution of HCl, H_2O_2 and water (1:1:10) at room temperature without conductivity decreasing.

The most interesting result for hydrogen terminated diamond surface cleaning has been obtained using acetone. H-terminated samples sheet resistance R_S has been measured by four point probe technique for different current value and, before processing it has been cleaned by means of ultrasonic bath in acetone. R_S has been measured again for the same current values and it resulted lower than before. Repeating this process few times, sheet resistance has a “saturation” value (read as “it cannot be lower”).

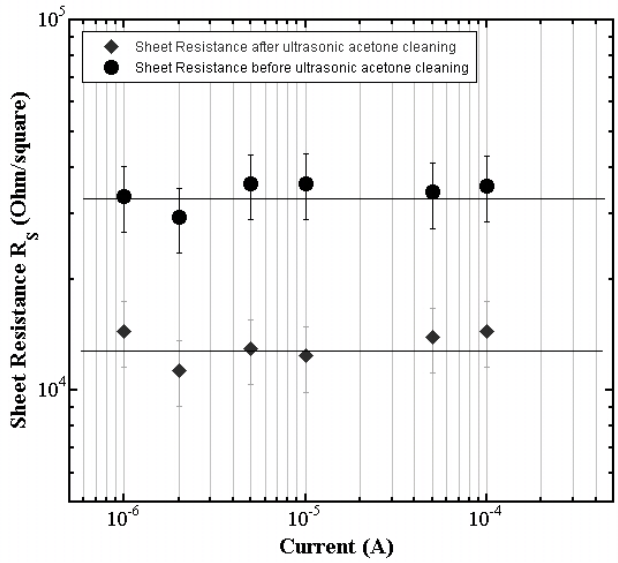


Figure 58 – H-terminated surface sheet resistance values obtained before and after ultrasonic acetone cleaning

Figure 58 shows sheet resistance values obtained before and after ultrasonic acetone cleaning. This process has been repeated many times with three different diamond

samples, obtaining the same results. It is probable that the adsorbate layer does not involve water particles and the conductivity is enhanced when the surface upon the hydrogen terminated layer is clean. This experimental results obviously needs more accurate studies and close examination, but also state the needing for a passivation technology that preserve surface from air interaction.

4. Hydrogen termination

Hydrogen termination is obtained by means of a microwave plasma assisted CVD chamber with easily commercial available microwave generators. High purity hydrogen gas at low pressure (10-100 mbar) subjected to an electric field, constant or time dependent, ionizes and produces a cold plasma, a plasma with electrons equivalent temperature higher than gas temperature (700-800°C). H^+ ions are generated by collisions of high energy electrons, equivalent temperature around 5000°C, with cold species (positive ions and neuters particles). Generally, before the hydrogen termination process, oxidized diamond samples are heated for about an hour at 850-900°C in high vacuum (approximately 10^{-7} mbar) in order to obtain a desorption of CVD growth residual hydrogen, a oxygen removal and to maximize the number of available diamond surface dangling bonds. Besides, at the end of process, chamber is slowly cooled down from 900°C to room temperature in hydrogen atmosphere in order to avoid a quick hydrogen desorption and surface oxidation.

Diamond samples used during this three years thesis have been hydrogen terminated with two different processes by General Physics Institute in Moscow and by Institute of Inorganic Methodologies and Plasmas (IMIP) in Rome.

✓ *General Physics Institute (RAS, Moscow)*

The smoothed film surface was treated in a high-temperature microwave hydrogen plasma by using an Astex PDS19 CVD system (5 kW power, 2.45 GHz frequency). The reaction chamber was initially heated at 650-750°C under vacuum; once the temperature was stabilized, a purified hydrogen flow-rate of 500 sccm was established maintaining the chamber pressure around 60-80 Torr. The hydrogen plasma is then ignited at 1.6-2.1 kW for 10 min. After the treatment, the chamber is left to decrease naturally to room temperature under argon flow before the sample removal.

✓ *Institute of Inorganic Methodologies and Plasmas (CNR, Rome)*

Diamond sample is introduced in a high-temperature hydrogen plasma obtained in a Astex S-1500 CVD system (2 kW power, 2.45 GHz frequency). The reaction start at 700°C and the chamber pressure is maintained at 80 Torr while a flow-rate of 200 sccm of hydrogen gas is injected in the chamber. The hydrogen plasma is the ignited at 1.22 kW for 30-35 min. After the treatment, the chamber is left to decrease naturally to room temperature under argon flow before the sample removal.

5. Device layout design

Diamond MESFETs layout has been studied during this PhD thesis in order to improve RF and DC performances. Typical butterfly shaped two gate fingers structure has been used MESFETs fabrication.

Figure 59 shows the first implemented device layout, developed in a previous degree thesis in collaboration with *Selex Sistemi Integrati* in Rome. Such a layout is an arrangement to hydrogen terminated diamond of a pre-existing Gallium Nitride based HEMTs (High Electron Mobility Transistors) structure, Selex leading-edge technology. This structure has been obviously modified for our technology requirements and presented a 4 µm drain to source channel in order to allow optical lithography of at least ohmic contacts and an I-shaped gate structure to fabricated by electron beam lithography. Besides, the first step was the fabrication of ohmic contacts directly on the h-terminated surface, a following isolation step in order to allow the conduction only in the drain to source channel and finally the gate electrodes.

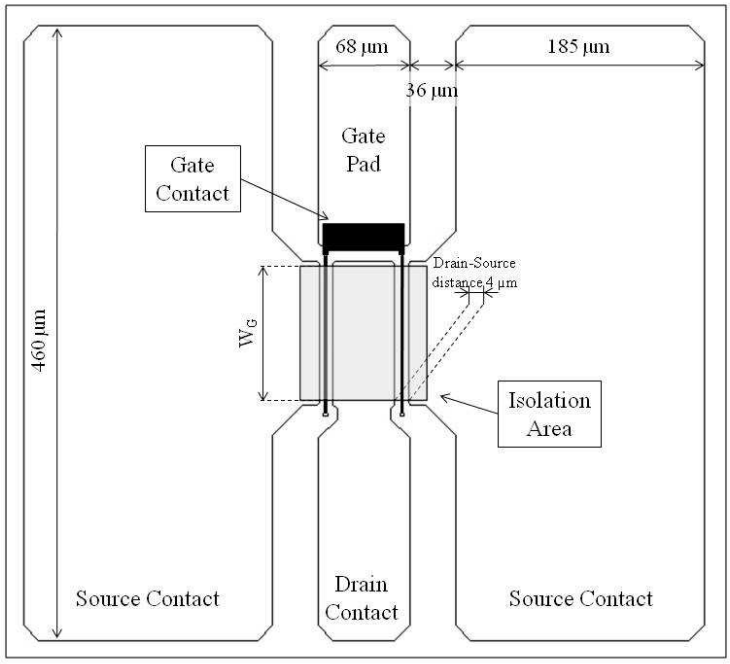


Figure 59 – the first implemented device layout, developed in a previous degree thesis in collaboration with *Selex Sistemi Integrati* in Rome. Such a layout is an arrangement to hydrogen terminated diamond of a pre-existing Gallium Nitride based HEMTs (High Electron Mobility Transistors) structure.

The characterization results obtained for that layout based transistors and the new technological ideas and issues, lead to a new structure finally based on diamond characteristics. By means of TxLine tool of AWR MicroWave Office software it has

been possible to evaluate the correct dimensions for the coplanar wave guides for obtaining a suitable input-output impedance matching of FETs. The layout has been then redesigned with the new dimensions using the free license cad LASI (LAyout System for Individuals), version 7.0.69.

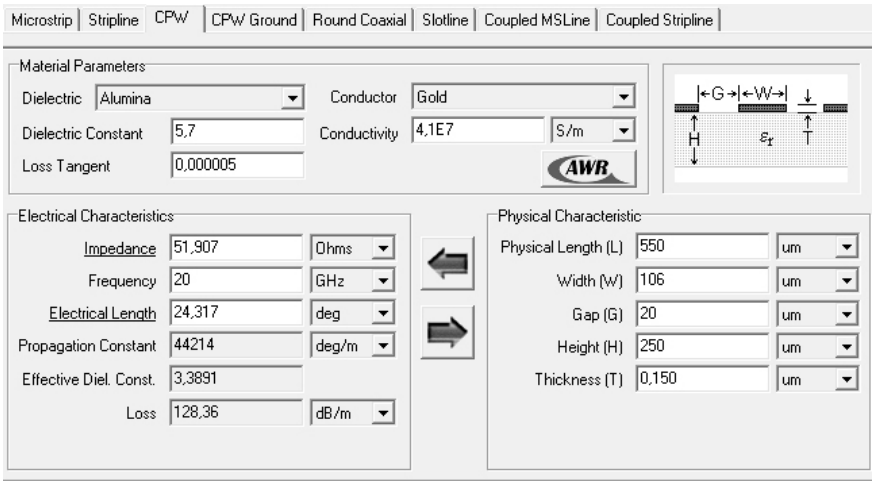


Figure 60 - TxLine tool of AWR MicroWave Office software

Figure 60 is a thumbnail of the very easily software interface: it is possible to insert the substrate parameters (dielectric constant ε_R=5.7 and loss tangent minor than 10^{-5} from literature) and the contact metallization conductivity in the first window and fixing the device layout dimension, the software simulates the impedance matching and the electrical length (electrical length is the length of a transmission medium or antenna element expressed as the number of wavelengths of the signal propagating in the medium) or vice-versa. After many attempts, approximations and calculations, the better compromise for an approximately 50 ohms impedance matching has been obtained for a device with a gap between drain and source pads of 20 µm and a drain pad of 106 µm (Fig. 61). In this structure, after the hydrogen terminated active area definition, ohmic contacts are fabricated on oxygen terminated diamond except for a small part in proximity of drain-source channel in order to obtain a better adhesion of gold and a higher mechanical and electrical stability to contacts. Figure 62 shows the schematic section of such a structure. An on-wafer calibration kit has been also projected and fabricated by S^2DEL group in collaboration with Tor Vergata Univeristy[206]: a calibration procedure able to remove systematic errors due to measurement set-up non-idealities (related to VNA, cables, connectors and planar probes). On-wafer calibration ensure the possibility to access the intrinsic device without implementing de-embedding procedure, obtaining more accurate information on active device characteristics and performance.

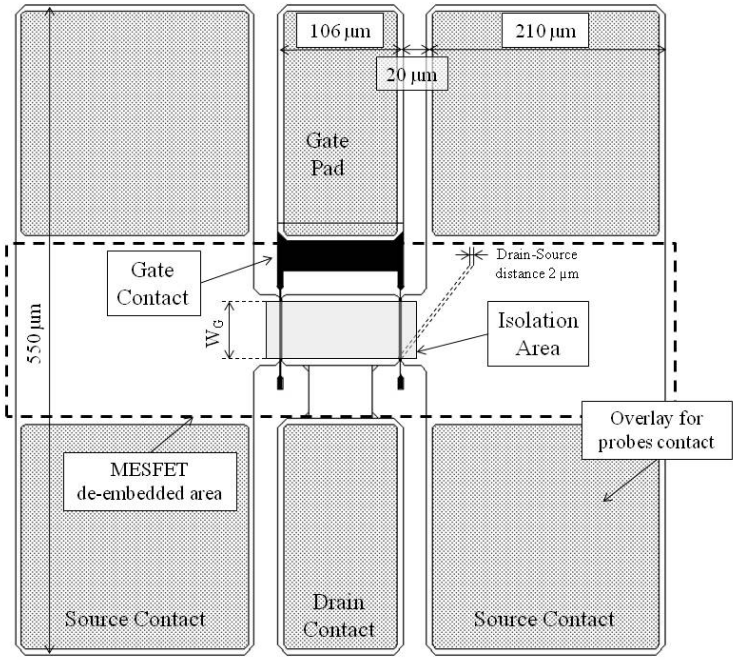


Figure 61 – S^{2}DEL Diamond based MESFETs layout

The solution proposed has been a Line-Reflect-Reflect-Match (LRRM) calibration which uses a space conservative standard set which consist of a matched Line (Thru) of short delay, two Reflection standard (Open and Short) partially unknown (only the phase is needed) and a Match that must be know only in the DC resistance component of its impedance.

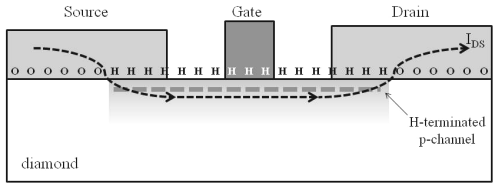


Figure 62 – Schematic section of S^{2}DEL MESFETs structure

Moreover, the dimension of the gate contact has been projected to be as resistive as the final part of the drain pad. Simply according to the Ohm's law, keeping in to account the metallization thickness for gold and for aluminum and the respective specific resistivity, it has been possible to fabricate two different geometric areas for gate and drain final parts in order to have approximately equally resistive contacts: $(\rho_{Al} \times d_{Gate})/A_{Gate} = (\rho_{Au} \times d_{Drain})/A_{Drain}$ so, considering d as the metal thickness and A as the contact area, $A_{Gate} = A_{Drain} \times (\rho_{Al} \times d_{Gate})/(\rho_{Au} \times d_{Drain})$. Overlay pads have been in addiction designed to preserve the ohmic contacts during the characterization.

6. Ohmic Contact

Ohmic contacts for hydrogen terminated diamond technology is probably the most critical issue. H-terminated surface acts like a sort of oiled pavement for the contact metals, creating many adhesion problems. Moreover, the worst adhesion has been found for gold. This means that devices are quite unstable and each measurement cannot be reiterated. Gold directly on hydrogen terminated layer typically presents scratches after probes contacting and in this sense it is impossible to obtain the same behavior in a second measurements run. It cannot be accepted for a technology that would like to be industrialized, so many tricks have been found in order to avoid this annoying phenomenon. Anyway, best way is to change contact material and/or technology. Nevertheless, for reasons that will be clear in the following, gold is the only metal that could be easily used for self-aligned technique: gold can be easily wet etched by means of a non-oxidizing solution of KI and I_2, avoiding in this way the hydrogen atoms removing and the consequently conductivity loss.

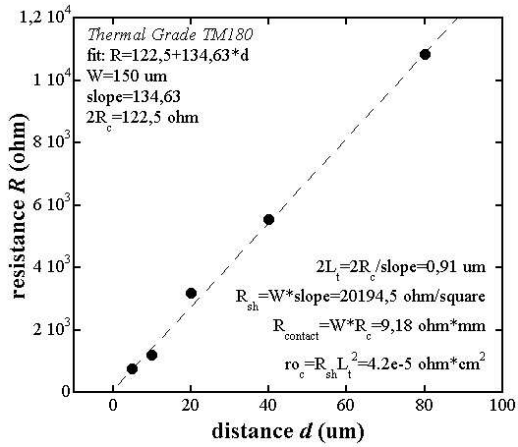


Figure 63 – TLM characteristics for a hydrogen terminated polycrystalline diamond

Even if good results have been obtained in terms of performances with an ohmic contact of gold entirely deposited on hydrogen terminated surface, an alternative will be discussed. A first solution to adhesion issues has been thought to be the deposition of part of the contact upon oxidized diamond surface that, because of group's previous experiences, ensure a good gold mechanical adhesion. It has been possible after TLM (Transfer Length Method) structure results interpretation (in Figure 63 an example of TLMs structure characteristics for a hydrogen terminated polycrystalline diamond): such a structure fabricated on few hydrogen terminated samples pointed out a very small transfer length L_T (almost always smaller than 1 µm) so the conduction can be considered even lateral. In other words, the hydrogen terminated area has been reduced and it confined in few microns around the gate area, assuring a unchanged conduction

and a better gold adhesion (Fig. 62). This remarks have also been important for projecting different kind of contacts like an annealed Titanium/Gold alloy (subject of another S^2DEL PhD thesis). In fact, the almost uselessness of hydrogen presence underneath the metal and the hypothesis of lateral conduction, allow the fabrication of contacts also with techniques that could damage or destroy hydrogen layer beneath them.

After this brief introduction, techniques and instruments used for ohmic contacts fabricated in this thesis will be reviewed and a section will be dedicated to the integration of Diamond Detectors Ltd. (in the following, DDL) proprietary contact with S^2DEL technology.

6.1. Photolithography

Most of technological steps of devices fabrication could be, and has been, carried out with standard optical lithography because of the non critical dimensions involved. Two contact mask aligners have been used during this thesis: Karl Suss MA6 at S^2DEL and Karl Suss MA150 at IFN-CNR. Megaposit SPR 220-3 and Shipley Microposit S18-13 positive photoresist have been used. SPR 220-3 has been spun for 1 minute at 4000 rpm in order to obtain a 3 µm thickness and then soft-baked for 80 seconds in oven at 120°C; exposure with Karl Suss MA6 equipped with 275 W lamp, varies between 20 and 40 seconds, depending on the structure complexity; after the post exposure bake (PEB) of 80 seconds at 120°C, lithography is developed with NaOH based solution Microposit MF-321 for 30-90 seconds, depending on structures again. S18-13 has been spun for 1 minute at 3000 rpm to obtain a 1.6 µm thickness and then soft-baked for 60 seconds in hot plate at 115°C; exposure with Karl Suss MA150 equipped with a 350 W lamp changes in between of 15-30 seconds and after the PEB, lithography is developed for 20-60 seconds.

For DDL contact fabrication, a clean room has been build up, set up and equipped with contact mask aligner Cobilt CA800. Image reversal photoresist AZ 5214 has been used. Prebake of 2 minutes at 90°C has been performed with hot plate, first exposure of 3 seconds followed by a post bake, for image reversing, of 1 minute and 30 seconds. Sample has been light for last exposure for 15 seconds.

6.2. Electron Beam Lithography

Optical photolithography presents high resolution limits in contrast with the needing for dimensions reduction. The best alternative is the Electron Beam Lithography (EBL) that, using the low electrons wavelength, is able to avoid diffraction effects and allows a very high resolution. EBL system produces an electrons beam with a set current densisty by means of an electron emitter with a

thermoelectronic emission tungsten (W) cathode. Such an electrons beam is focused for the desired high resolution and the direction is determined by interdiction electrodes and deflection coils controlled by a software. Because of the high resolution, substrate position is critical and needs a precise placement and moreover, the system needs high vacuum conditions to assure perfect beam guidance.

Figure 64 - Leica Microsystem EBPG5HR at Institute of Photonics and Nanotechnologies (IFN-CNR)

EBL system used for MESFETs fabrication during this thesis is the *Leica Microsystem EBPG5HR* (Fig. 64) nearby Institute of Photonics and Nanotechnologies. Electrons Emitter is a Schottky Field Effect Gun (FEG) with a (100) oriented tungsten tip, a ZrO tank and polycrystalline tungsten filament. Schottky emission is obtained by supplying to emitter's electrons a thermic energy higher than their work function so that electrons can ionized and be emitted by cathode.

Electronic resist used for MESFET fabrication is PMMA 600K (Polymethyl methacrylate), spun on the sample for 60 second at 3000 rpm obtaining a thickness of approximately 800 nm, after pre-heating at 170°C for 5 minutes.

6.3. Standard technique

Figure 65 is a schematic process steps of the standard technique for ohmic contact fabrication, so-called "standard" because in contrast with the self-aligned gate technique (see next section). With this technique, the drain to source distance is pre-defined and fixed. Such a process has been carried out both by optical and electronic lithography, within different runs, and in figure only the EBL steps are presented: for optical lithography the steps are basically the same, without the Cr layer, useless in this case.

After MESFET active area definition steps (see section 7), sample is prepared and cleaned in hot acetone, IPA and de-ionized water, and so resist is spun upon the surface (Fig. 65a), then a thin layer of chromium is evaporated on the resist in order to avoid phenomena of beam reflection and deflection due to substrate transparency (b). The

mask of the ohmic contact layout is then exposed (in the EBL sense of beam focused and structures written on the selected areas by means of software controls) for structure design (c). Hence, after sample removal from machine and Cr etching, resist is developed and remains only on the areas where metal has not to be deposited (positive resist, Fig. 65d). 150-200 nm of ohmic contacts metallization are so evaporated by thermal or electron beam procedure (e) and after hot and/or syringe assisted acetone lift off, ohmic contacts are ready (f).

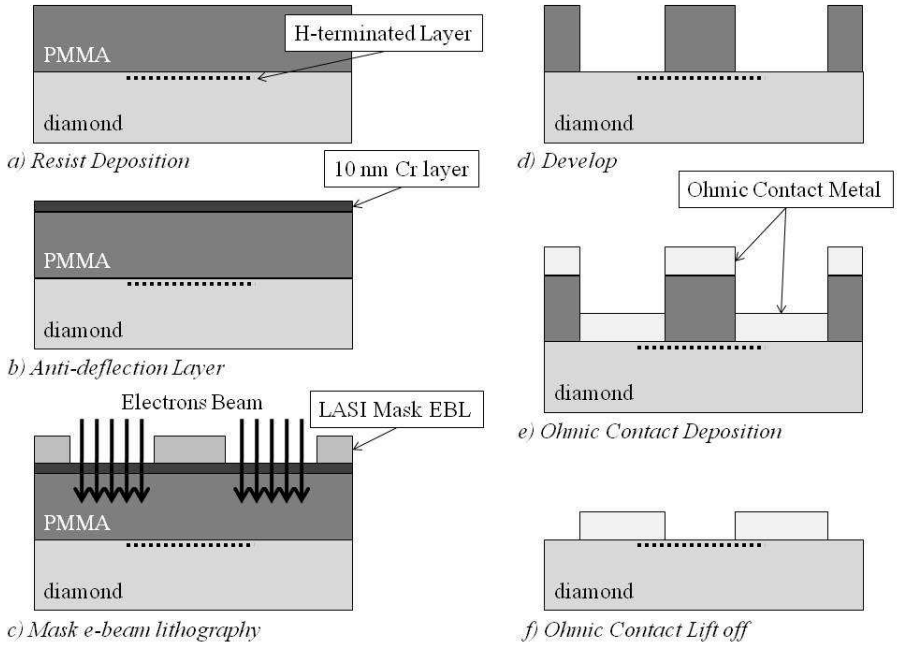


Figure 65 – Ohmic contacts standard fabrication procedure

This standard process can be applied to a lot of different metals because it does not involve wet etching steps and so preserve the hydrogen terminated layer from damaging solutions. The same technique has been applied for DDL contact[198] fabrication. Figure 66 shows a schematic section of such a contact[207]: a thin layer of Diamond-like-Carbon (DLC) is fabricated at the metal-diamond interface.

DLC is a form of amorphous carbon between diamond and graphite, containing significant portion of sp^3 bonded atoms in the matrix. DLC films can be grown when carbon is deposited under energetic (~10–100 eV) bombardment, where the instantaneous local high temperature and pressure induce a proportion of carbon atoms to bond as diamond. The conditions for DLC deposition are obtained during a variety of methods, including CVD, laser ablation, magnetron sputtering, cathodic arc, and ion beam deposition. The novel contact consists of a very thin (1–3 nm) diamond-like carbon film which was formed on a diamond substrate by means of Argon magnetron

sputtering. The very thin DLC layer allows for the injection of both holes and electrons in the diamond substrate.

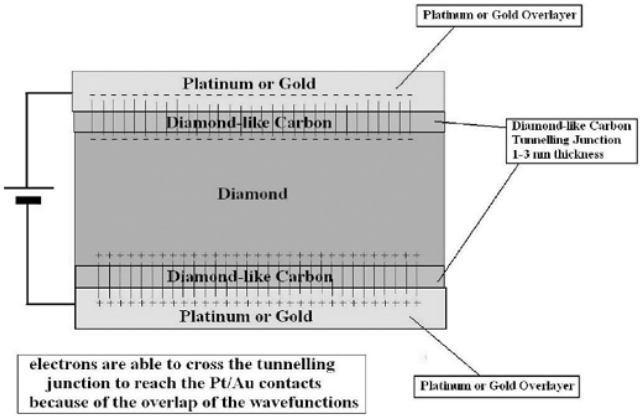


Figure 66 - schematic section of DDL proprietary contact[198,207]

At the same time the DLC layer becomes a seed for the sputter deposition of high work function noble metals (Pt, Au) which allows metals to stick on the diamond surface. Having both platinum and gold a higher work function than diamond this translates into the ability for electrons present at the diamond surface to be driven towards the noble metals via quantum mechanical tunnelling through the thin DLC layer acting as a quantum mechanical tunnelling junction.

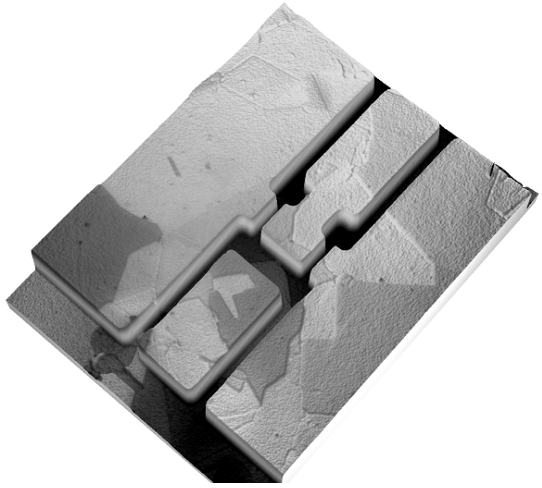


Figure 67 – MESFET fabricated with DDL contact on large grain size polycrystalline diamond (picture by Veeco Wyko NT9100 Optical Profiler)

Figure 67 shows a picture taken by Veeco Wyko NT9100 Optical Profiler of a MESFET fabricated on a highest quality Element Six polycrystalline diamond sample, with such a DLC/Pt/Au ohmic contact. The fabrication process, entirely carried out in

Diamond Detectors Ltd. laboratories except for hydrogen termination step, includes a surface damaging that do not obstruct conductivity and it is even possible to suppose that do not seem to remove hydrogen termination.

The same technological process has been also used for the realization of annealed titanium/gold contacts resulting in a TiC/Au structure. In this case, the hydrogen termination process is the following step. First results for this approach are very encouraging in terms of adhesion and conduction and will be deeply analyzed in another group's member PhD thesis.

6.4. Self Aligned Gate Technique

Hydrogen termination is essential for generating hole carriers and in order to retain the H-termination there are some restrictions on self-aligned gate (SAG) process. For example, the following processes, which are generally used for Si technology, cannot be applied to H-terminated diamond devices.

- ✓ Baking or heating in the atmosphere in the presence of oxygen molecules at temperatures over 150 °C
- ✓ Dry etching (CCP, ICP, and Ashing)

Due to these restrictions, the baking temperature cannot be increased up to the recommended temperature for photo and EB resists or polyimide materials (~300 °C). Also, it is difficult to deposit high-k materials on a H-terminated surface because the high-k materials have high melting points and are generally deposited using sputtering. Therefore, most of structures or patterns on a H-terminated surface have been formed by the self-alignment gate process that consists only of wet-etching and vacuum evaporation.

Figure 68 shows the self-aligned gate process flow. Also in this case, after MESFET active area definition steps, sample is prepared and cleaned in hot acetone, IPA and de-ionized water, and so resist is spun upon the surface (Fig. 68a), then a thin layer of chromium is evaporated on the resist in order to avoid phenomena of beam reflection and deflection due to substrate transparency (b). The mask of the ohmic contact metallization is then exposed (c). So, after sample removal from machine and Cr etching, resist is developed and remains on the areas where metal has not to be deposited (d).

150-200 nm of metal are so evaporated by thermal or electron beam procedure in this case also upon the drain to source channel (e). Then again sample is prepared and cleaned for lithography process (f, g). The gate electrode is then aligned by EBL and resist is written and so developed (h, i). The last step is the most critical one: a wet-etching of the ohmic contact metal is performed in order to "open" the drain to source channel (l).

This self-aligned technique arrangement allows a high drain to source channel reduction. Several analysis point out a drain to source channel distance of approximately $(0.8+L_G+0.8)$ µm. In the case of figure 69a (SEM) and 69b (AFM), for a gate length of 400 nm and 1 µm, 2 µm and 2.5 µm channel respectively have been obtained with SAG technique. It is also possible to see how the ohmic contacts profile is unmarked and imprecise, creating obvious electric field issues. This relevant problem is due to the low controlled wet-etching process.

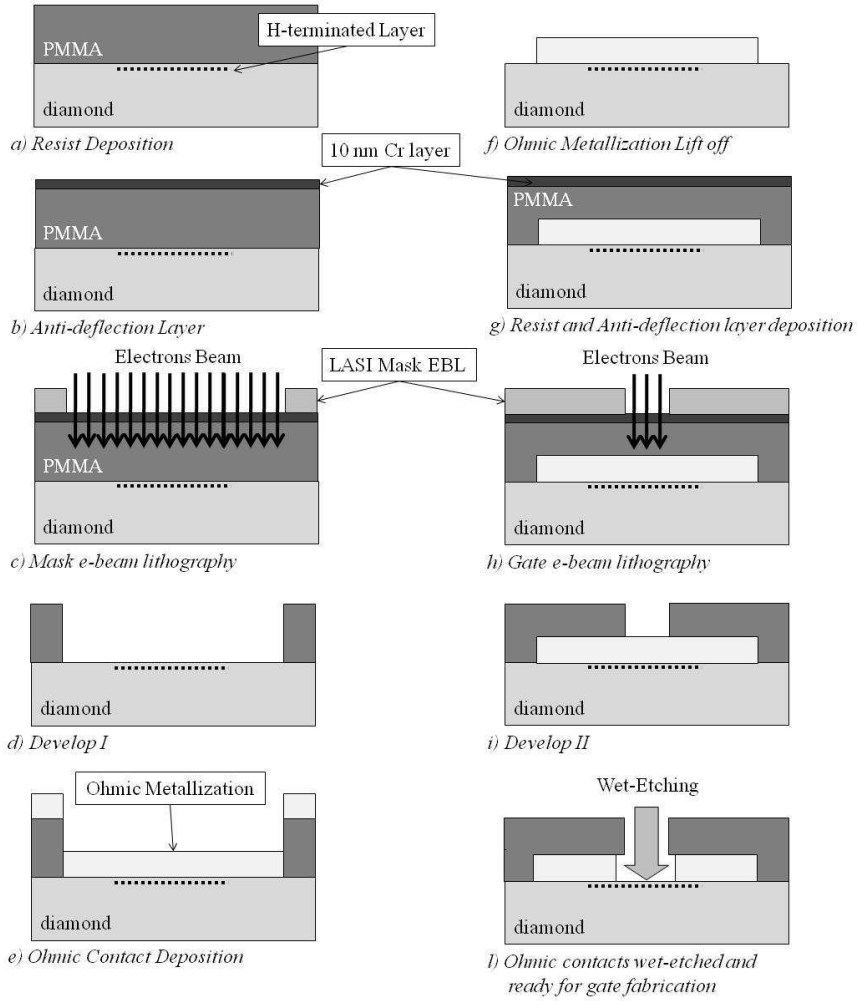


Figure 68 - Ohmic contacts self-aligned fabrication procedure

As already said, dry etching cannot be performed without hydrogen termination damaging. And, on the other hand, the only ohmic metal that can be wet-etched with a non-oxidant solution (in particular KI and I_2), is gold. In addition, the bad controllability of the process, gives low repeatability to device technology.

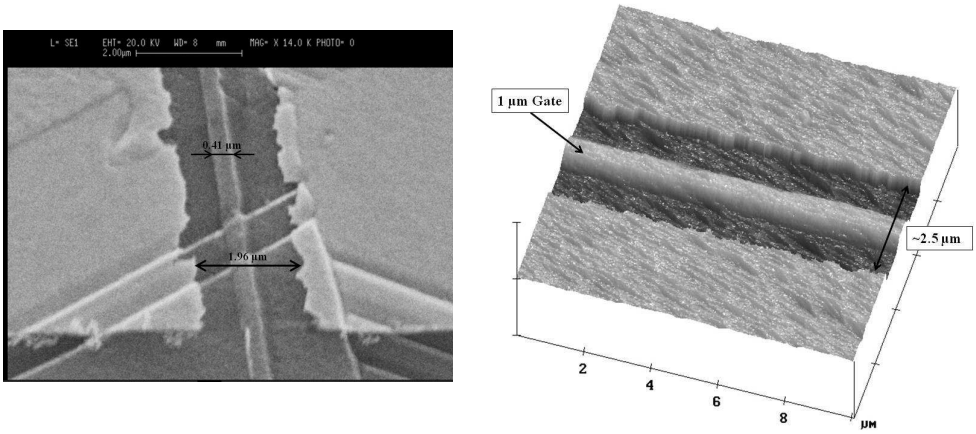


Figure 69 -Scanning Electron Microscopy (SEM) picture of a 0.4 µm SAG (a, left) and Atomic Force Microscopy (AFM) picture of a 1 µm SAG (b, right)

7. Device Isolation

Device Isolation is performed together with active area definition step. After lithography for marker definition (Ti/Au), the mask for isolation is aligned. Then the sample is treated with a Reactive Ion Etching (RIE) for hydrogen removing and oxygen termination: it is well-known that diamond oxygen terminated surface presents a very high resistance (~10^{12}-10^{13} Ω). Up to the acquired experience, 60 seconds of RIE performed in Argon and Oxygen atmosphere (10 sccm Ar, 50 sccm O_2) with 50 W RF power assure an excellent device isolation and a good preservation of hydrogen termination under the resist film. Figure 70 shows an AFM picture of the hydrogen terminated surface interface with oxygen terminated one and it is possible to appreciate the absence of evident discontinuities in the diamond film after RIE process.

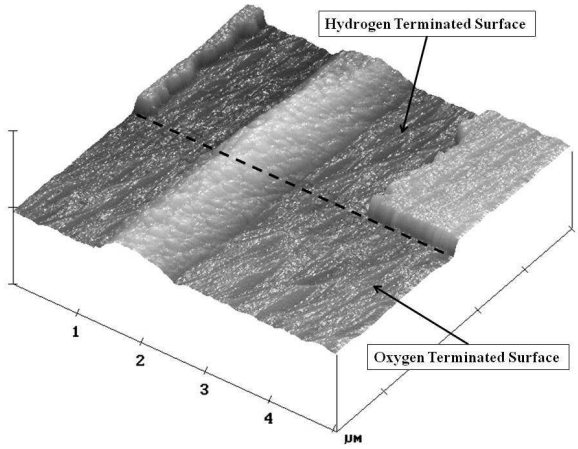


Figure 70 - AFM of the hydrogen terminated surface interface with oxygen terminated one: it is possible to appreciate the absence of evident discontinuities in the diamond film after RIE process

Such a process has been also successfully carried on using only Argon (10 sccm) for 3 minutes at 50 W RF power and with a Oxygen/ Nitrogen mixture (1:5) for 30 seconds at 400 W DC power. The same processes can be used for etching diamond.

8. Gate Electrode

Gate electrode is fundamental for device operation and of course it is decisive for performances. Optical lithography allows the possibility to fabricate a 3-4 µm gate length, interesting for device behavior analysis but unfulfilling for remarkable performances.

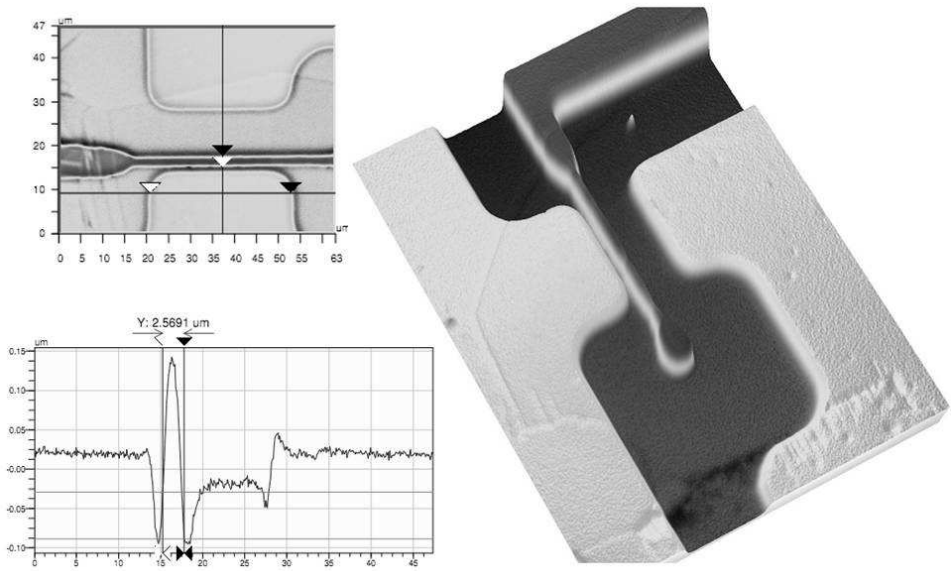


Figure 71 – Gate electrode of a MESFET fabricated with DDL contact on large grain size polycrystalline diamond (picture by Veeco Wyko NT9100 Optical Profiler)

Best performances with an optical lithography fabricated gate has been obtained by means of self-aligned gate technique and notwithstanding a f_{MAX} of approximately 2 GHz has been achieved[183] with a 4 µm gate length and a drain to source channel of thereabout 6 µm. Also MESFETs fabricated at DDL (Fig. 71 has been aligned with an optical lithography, but without self-aligned technique and even if gate length achieved is approximately 2.5 µm, the high drain to source channel distance (~12 µm) makes RF performances unremarkable and however estimated around 200 MHz for f_{MAX}.

Performance improvement needing leads to the use of EBL. With this technology it has been possible to reduce gate electrode length down to approximately 100 nm (Fig. 72). It has also been possible to try different gate section (for example T-gate) even if without remarkable results: polycrystalline diamond surface roughness and the grain boundaries presence make this technology quite difficult.

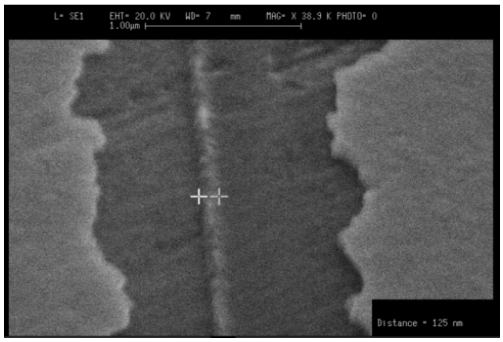


Figure 72 – a 125 nm self aligned gate electrode

Figure 73 shows the current-voltage behavior of different metals used as gate electrode for diamond based MESFETs. It is clear that aluminum presents the best rectification ratio and for this reason it has almost always been used for Schottky contacts fabrication. Nickel seems to present a quasi-ohmic behavior while chromium is visibly worse than Al.

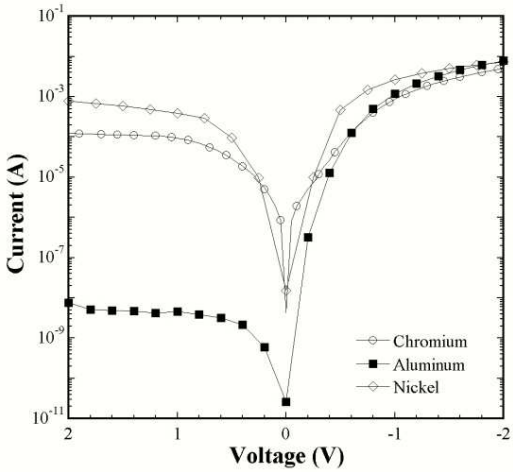


Figure 73 – current-voltage behavior of different metals used as gate electrode for diamond based MESFETs

Aluminum used for gate fabrication has been deposited on diamond surface by different techniques: thermal evaporation, e-beam evaporation, flash evaporation and RF sputtering. Best results in terms of MESFETs performances have been obtained depositing aluminum by means of thermal and flash evaporation. Electron beam evaporation and RF sputtering very high deposition rates do not allow aluminum to create its oxidized layer and so gate leakage currents are typically very high. Thermal evaporation, on the other hand, enables an aluminum oxidation at the interface H-terminated diamond/metal, creating a few nanometers AlO_x layer that enhances FET operation.

9. Hypothesis for improvement and development

Many technological improvements can be applied for development of higher performances MESFETs. The lack of means in terms both economic and of workforce, makes the technology development very slow and subject to institutes timetables. Anyway, many improvements have been hypothesized and lot of them have been first tested with encouraging results. In this section, author presents the technological improvements that would like to applied to MESFETs structure in order to obtain the desired stability and performances increase.

First step would be the realization of stable and stress-resistant ohmic contacts. Of corse, the possibility of creating a thin layer of carbide at the metal-diamond interface is a great strategy, but the possibility of a shallow implantation of boron beneath the metallization would allow a higher charge transport between the contact and the hydrogen terminated layer.

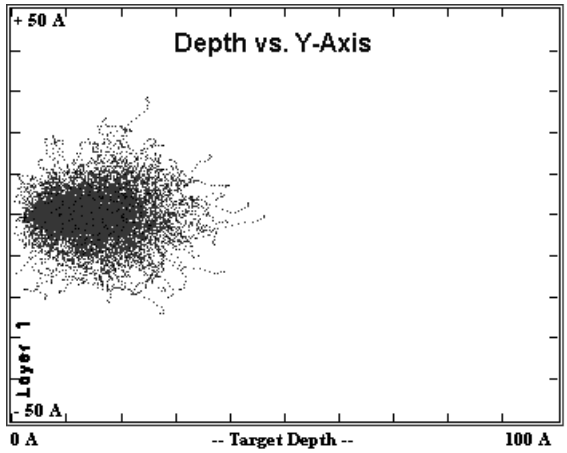


Figure 74 - SRIM calculation for boron soft implantation (0.5 keV) in diamond

Such a boron layer could be easily fabricated by energetic sputtering of a boron target: SRIM calculation (Fig. 74) points out the possibility of obtaining a shallow implantation (2-3 nm) with a low energetic sputtering (0.5 keV). After a rapid annealing (4 minutes a 650-700°C) graphite is formed upon the boron doped layer and it could be etched or used as a buffer layer for contact fabrication, that could be in addiction electroplated in order to obtain a higher thickness and a subsequently lower contact degradation during measurements.

Hydrogen termination process could be then performed and a passivation layer of 10-20 nm of ceramic material could be fabricated in order to preserve the hydrogen termination from atmospheric interaction (see section 3 of this chapter). Such a ceramic material can be Al_2O_3 or AlN, sputtered or deposited by Pulse Laser Deposition (PLD) or Atomic Layer Deposition (ALD).

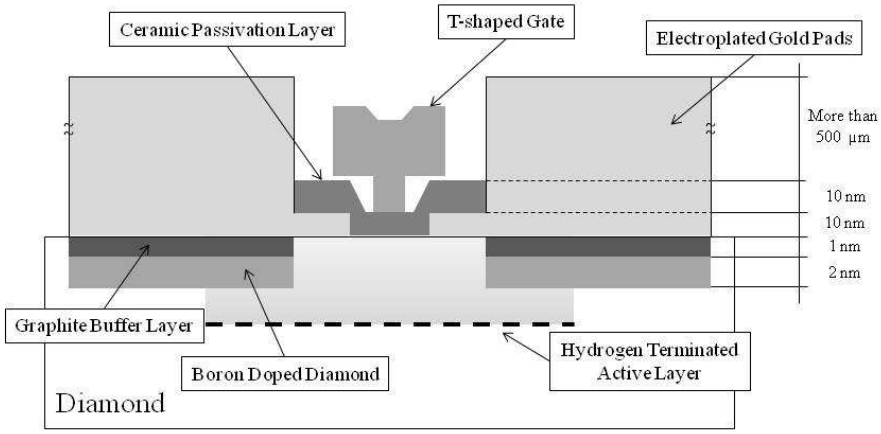


Figure 75 - hypothesized MESFET structure

Such a layer can be also usefull for fabrication of a field plate and/or a T-shaped gate electrode. It is important to notice that such hypothesis are supported by experimental results and observation for other diamond based devices obtained during several collaboration by the author during this thesis period and by a scrupulous literature research. Figure 75 shows the hypothesized device structure. Morevoer, it is worth to notice that, in order to improve self aligned gate technique, a very thin layer of gold could be deposited (10-20 nm) for a more controlled wet etching.

Chapter 3

In In this chapter, fabricated MESFETs operation will be exposed and discussed. MESFETs have been fabricated on different diamond samples, polycrystalline and single crystal, with both layouts previously discussed.

The differences and the analogies between examined devices will be investigated in order to obtain information about the hydrogen terminated surface behavior, the most critical point, and the fabrication issues. It will be possible to demonstrate how the characterization data will fit with the theoretical MESFETs model previously illustrated.

MESFETs characterization has been carried on in Roma Tre laboratory (S^2DEL) as far as it concerned the direct current (DC) and the low frequency behavior. Small signal analysis and modeling has been accomplished in collaboration with the Electronic Engineering Department of Tor Vergata University in Rome while the large signal characterization is the result of a scientific collaboration with the Department of Electronics at Politecnico di Torino.

Other interesting devices characterization has been carried out in collaboration with the Department of Physics and the National Institute of Nuclear Physics (INFN) section of Roma Tre University.

It is worth to notice, before any results exposition, that our technology is based on “as supplied” diamond: up to now, our technological facilities do not allow a diamond structure modification, a custom crystallographic orientation, a further high purity layer growth nor a surface roughness reduction. This is a key point for data understanding:

even if they are very encouraging and of remarkable value compared with literature. Other groups working on the same field obtained their results on customized diamond samples, choosing the crystallographic orientation and the purity level.

Most of the following data have been published in few papers and presented successfully in many conferences during such three years. Remarkable results in terms of RF output power density have been obtained for polycrystalline diamond MESFETs that, up to now, are the best in literature. Small signal characteristics are comparable as well.

1. Hydrogen Terminated Layer Characterization

Hydrogen terminated layers have been characterized by means of Hall bar structures fabricated on diamond surface. Low temperature carriers' behavior has been investigated in vacuum in the 17-300 K temperature range and results are here reported for different samples analyzed.

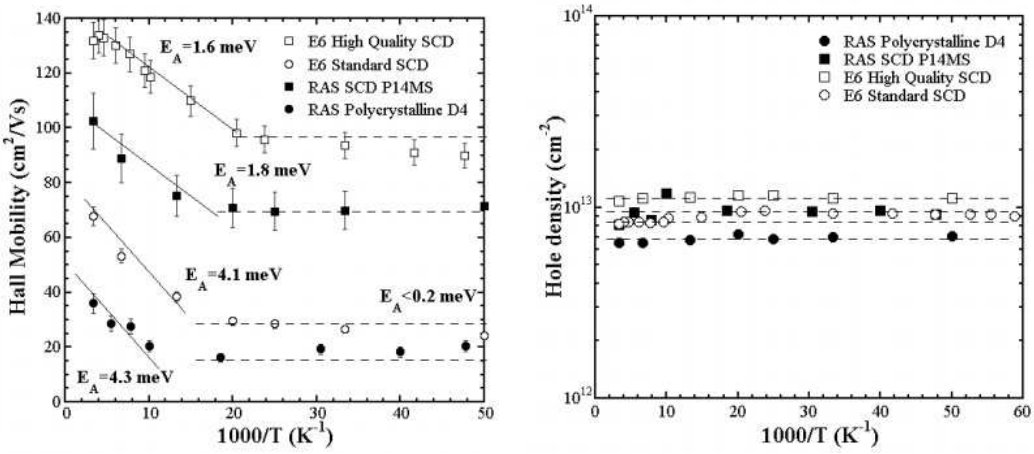


Figure 76 – Hall mobility (a, left) and hole density (b, right) of different diamond samples as a function of temperature inverse

Figure 76a show the Hall mobility dependence on the temperature. Samples present similar behaviors, two different regimes are apparent: the mobility is temperature independent at low T whereas, around 50K, an increasing trend is observed as the temperature rises. In general, higher mobility values, up to 130 cm^2/Vs, are achieved for higher quality diamond plates (E6 HQ SCD, RAS SCD P14MS) corresponding to an almost equal activation energy. Lower quality single crystal (E6 St. SCD) and polycrystalline plate (RAS PolyD4) shows a higher activation, around 4.2 meV. Moreover, polycrystalline sample mobility is evidently the lower and it can be ascribed to the grain boundaries scattering phenomena, mainly due to different crystallographic

orientations. It is easily possible to notice that mobility activation for all samples occurs around 50 K. Figure 76a also allows to venture the hypothesis of a relation of mobility and carriers activation energy E_A with diamond surface quality, in particular it could be related both to surface roughness and crystallographic defects as well. For lower temperature, mobility seems to be temperature independent with an E_A smaller than 0.2 meV. Figure 76b presents the carriers density for the same samples. Such a value is almost temperature independent and around 10^{13} cm^{-2} for all investigate diamond plates, as expected for 2D transport in extended states and in the absence of localizations. Anyway, probably due to uncontrolled crystallographic orientation, hole density results a little lower for RAS PolyD4.

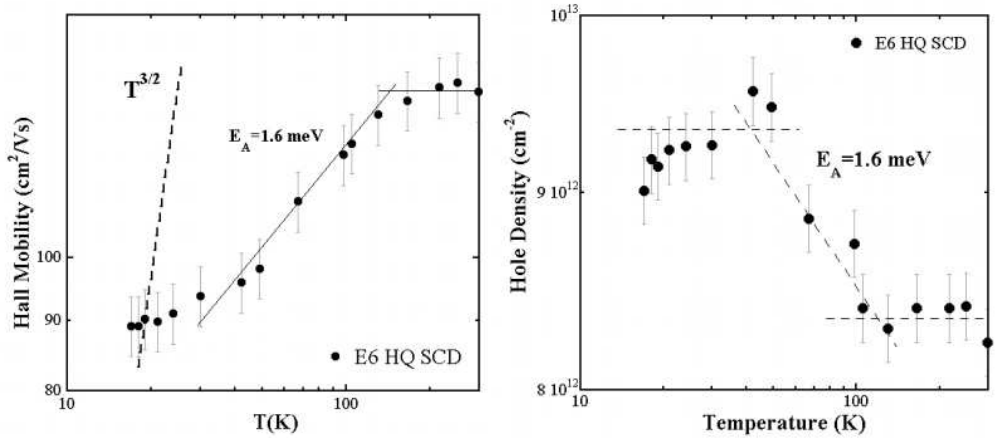


Figure 77 - Hall mobility (a, left) and hole density (b, right) of and high quality single crystal diamond plate as a function of temperature

Figure 77a shows the Hall mobility behavior of the investigated E6 HQ SCD diamond sample as a function of the temperature. A sigmoid trend is apparent in this figure. After an almost flat trend below 20K, the mobility increases, hydrogen terminated layer is activated with E_A of 1.6 meV to flat again up to room temperature. In figure it is also reported the $\mu \propto T^{3/2}$ trend, which is evidently different from H-terminated layer behavior so that the dominant scattering mechanism cannot be ascribed to ionized impurities. It is possible that frozen ions in hydrogen terminated layer, below 50 K, are limited by a Rutherford-like scattering; the activation that occurs around 50 K is still not clear. Even if compared with figure 77b, in which the little reduction of carriers density for higher temperature is similar to literature reported behavior of a theoretical two-dimensional electrons gas (2DEG)[210], it results very difficult to infer holes mobility trend of hydrogen terminated layer also with electron-hole scattering models: it could be suggested that temperature inducted potential fluctuations on diamond surface, probably caused by the presence of charged ions or residual adsorbates, give rise to a situation in which more-conductive and less-

conductive regions coexist and generate potential barriers which enhance the transport[211]. For T higher than room temperature it is possible to suppose a mobility reduction due to phonon scattering. Figure 78a and 78 b show the Hall mobility of the investigated samples in the lower temperature range and the activation energies E_A comparison for oxygen terminated and hydrogen terminated surfaces.

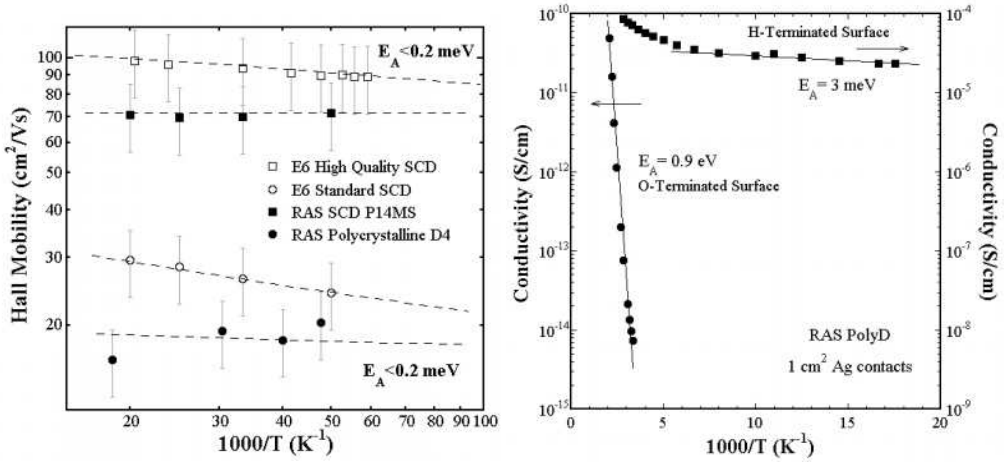


Figure 78 – Hall mobility dependence of different samples on low temperature inverse (a, left) and conductivity of hydrogen and oxygen terminated diamond as a function of temperature inverse

Figure 79 presents a comparison of results achieved in this thesis and literature ones. In the low temperature range, the mobility behavior is comparable while obtained values are evidently higher

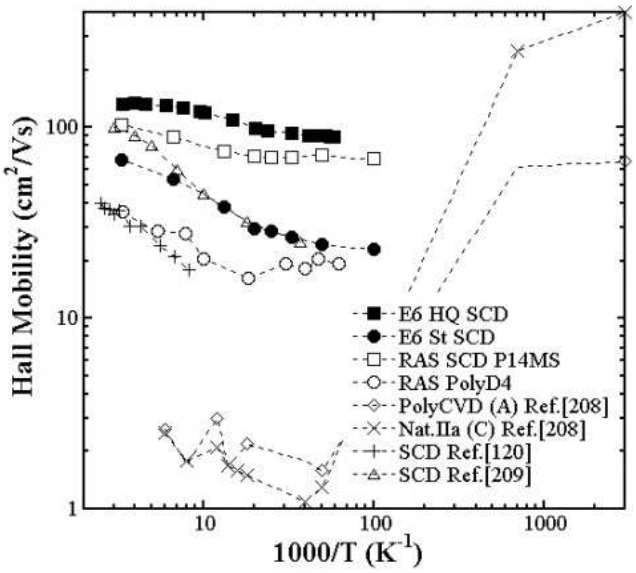


Figure 79 – comparison of results achieved in this thesis and literature for Hall mobility

It is worth to notice that other groups declared higher room temperature values[186]. For very low temperatures, an inversion of trend has been found, resulting in mobilities in excess of 400 cm2/Vs.

However, mobility mechanism is still a key point for understanding of hydrogen terminated surface behavior and up to now no hypothesis seem to be completely satisfying. In fact, 2DHG formation and surface transport are strictly dependent on the surface roughness, grains orientation, average dimension, etc, in such a way different groups - working on different substrates, and with different hydrogenation recipes - report quite different trends. It is our auspice, in the future, to have the possibility to work on well established diamond plates where all such interdependent effects might be fixed.

2. Gate Junction

Gate junction has been characterized in DC and low frequency AC mode. Current-Voltage (I-V) and Capacitance-Voltage (C-V,ω) measurements have been performed in order to understand junction quality and carriers bias dependent behavior.

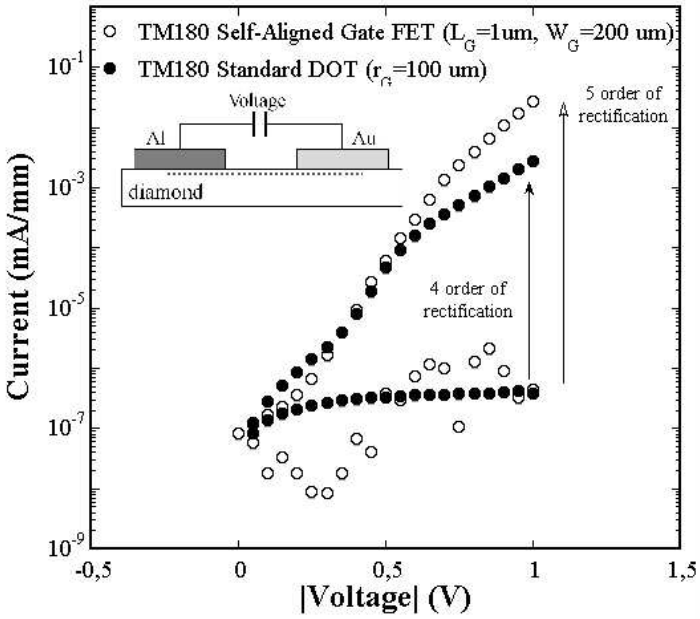


Figure 80 – Current dependence on voltage of two diode structures fabricated on nominally identical samples (TM180 by E6) with the two different gate technology techniques.

Characterization has been carried out on different diamond samples. Here, results obtained for devices and structures fabricated mainly on Thermal Management Grade diamond plates by Element Six (in the following called TM180) will be reported and

deeply discussed, without ignoring to notice any non similar results achieved on other substrates during this thesis. It is important to remark that all TM180 surfaces are hydrogen terminated by means of the same process at IMIP-CNR.

Information have been obtained for both standard and self-aligned gate structures, pointing out few remarkable analogies and interesting trends. From C-V curves it has been possible to extract charge carriers profiles and built-in voltage value. Low temperature measurements in this optics will be useful for confirming and extending the discussion. Field effect mobility has been achieved as well from both C-V and I-V data, finding good agreement with Hall bars characterization results. Following characterization has been performed with HP4140B picoammeter and HP4192C Impedance Analyzer.

Figure 80 shows the current dependence on voltage of two diode structures fabricated on nominally equal samples (TM180 by E6) but with the two different gate technology techniques. In the inspected range (-1 V, 1 V), the self-aligned diode shows a higher rectification ratio due to the smallest electrode distance. On the other hand, reverse current feels the effect of rugged border of ohmic contact, consequence of the wet etching: unparallel and inconstant electric field loses the diode reverse bias behavior and surface scattering controls charge transfer. Surface scattering maybe the dominant mechanism, for these low quality samples, reverse bias current is very high if compared with other analyzed devices fabricated on higher quality substrates.

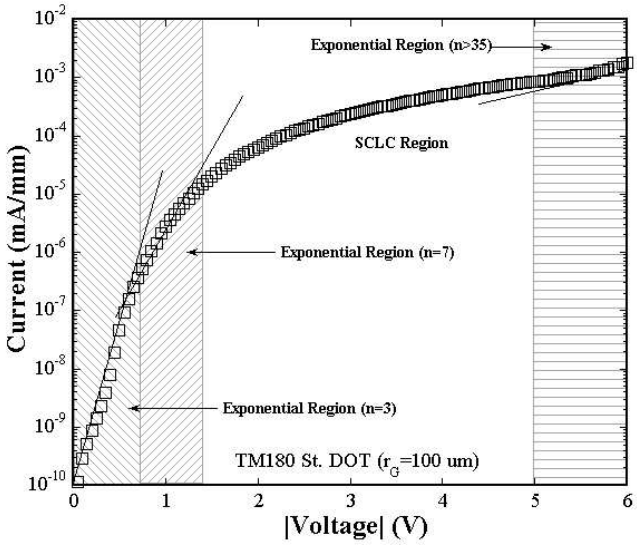


Figure 81 - Forward bias extended region for standard technique fabricated diode (a, left) and logarithmic plot of the same diode (b, right)

Figure 81 presents the forward bias extended region for the previously shown standard technique fabricated diode. Here it is possible to see two main regions of

operation, at least: the first exponential region spanning four orders of magnitude, typical of diode behavior; the second one, shows an increasing value of the quality factor that change from 3, in the diode regime, to 30 around 4V. Such behavior can be ascribed to a bad alignment of the planar diode circular structure (see figure 82), in such a way the annular crown area defining the lateral distance of diode changes continuously, leading to the effect found. This change of diode ideality factor has actually been found in several devices, especially if based on polycrystalline samples, without evident series resistance phenomena both for forward and inverse bias conditions. It is possible that surface roughness, grain boundaries scattering and different grain mobility enhance or deplete conduction. A suggestive supposition could be the change of quantum level in hydrogen induced two dimensional hole gas (2DHG) but it needs low and high temperature investigation to find a check. In between of 1.5 and 5 volts, a dependence on $V^{3/2}$ seems to found for current that could result in a space charge limited current region that could be caused both by hydrogen partial ionization toward bulk diamond and by a charge injection from electrodes due to local temperature increase. It would also mean a presence of only holes in the conductive region between the electrodes, supporting the 2DHG interpretation of the hydrogen terminated layer. Further measurements will be necessary to find a complete explanation for this behavior.

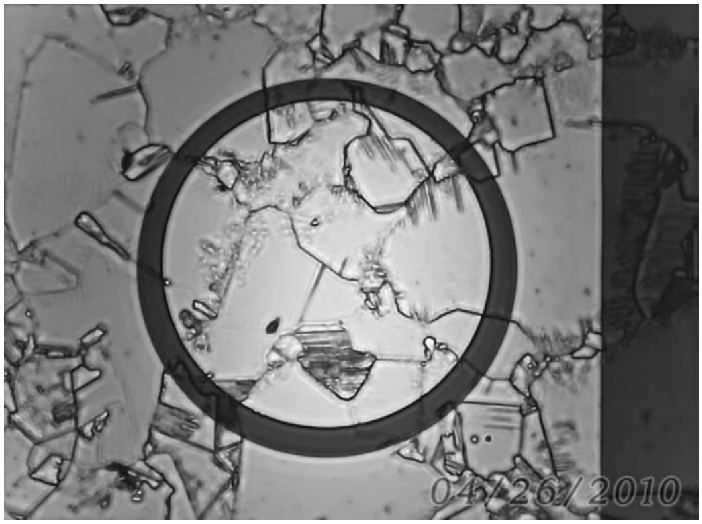


Figure 82 – TM180 by E6 based diode: a bad alignment of the planar diode circular structure could explain the diode ideality factor change pointed out by I-V characteristic.

When voltage is higher than 5 V, another diode is activated with a bad ideality factor (more than 35): the explanation for the presence of such a unexpected region could be found in the electric field breakdown achievement for the Schottky electrode and the formation of this diode with a current flow in bulk diamond.

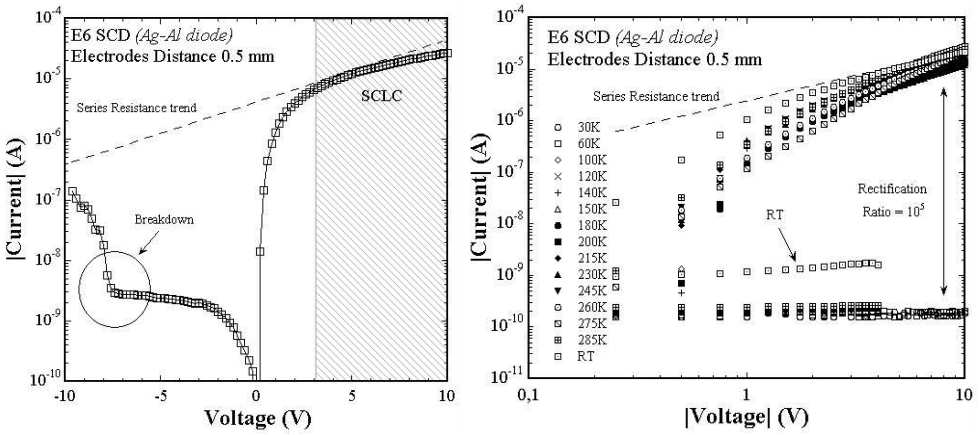


Figure 83 – I-V characteristics of a standard quality Element Six single crystal plate: active regions (a, left) and temperature dependence (b, right)

Measured hydrogen termination layer thickness is around 20 nm and the applied voltage results in a electric field comparable with E_B (10^7 V/cm). It results also evident from figure 83a: in inverse bias conditions, breakdown occurs around 7 V. Figure 83a shows the I-V characteristic of a planar diode structure fabricated on single crystal diamond where the ohmic contact is silver Ag. Similar trend for forward bias has been pointed out. Figure 83b plots the same diode for different temperatures in the rang 30-300 K. A clear inverse current reduction and an increase of rectification behavior can easily be seen.

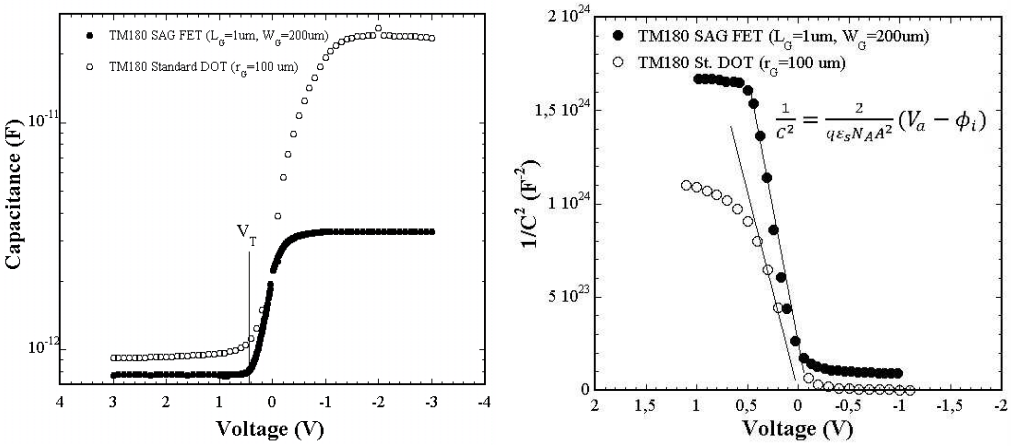


Figure 84 – Capacitance and $1/C^2$ behavior for two TM180 based diode structure (a, left and b, right respectively)

Capacitance of hydrogen terminated based devices has been measured in the range 100 Hz – 13 MHz. Figure 84a presents the capacitance dependence on applied voltage of the two already analyzed diode structures fabricated on a TM180, when the AC frequency is 1 MHz: self aligned structure shows a lower capacitance value due to the

smaller geometrical distance between electrodes. At a high forward bias, capacitance increases as the hole accumulation layer extended toward the ohmic electrode side of the Schottky contact and the electrode insulator capacitance became the dominant part of C. From the $1/C^2$ plot in figure 84b it has been possible to find a first approximation of the built-in voltage φ_i, almost equal for both structures and equal to 0.1-0.2 eV.

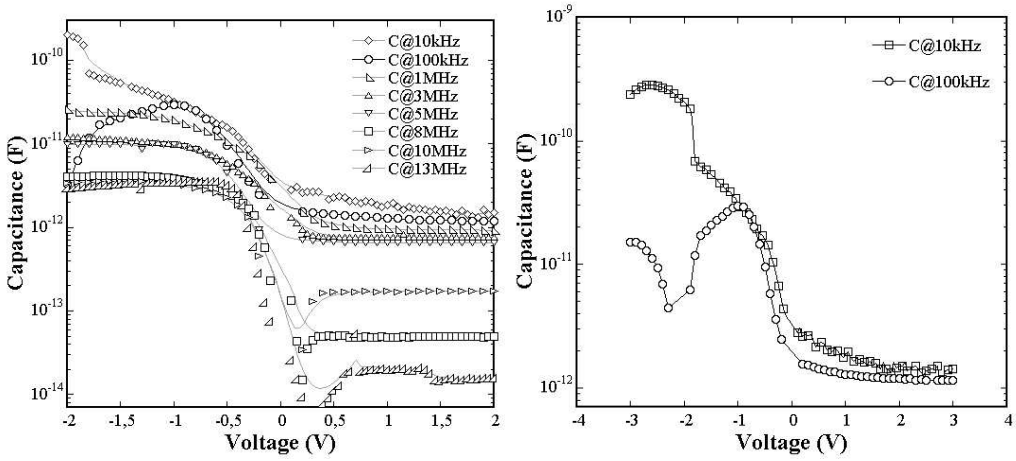


Figure 85 – Capacitance behavior of a standard fabricated diode for different frequency values (a, left) and for low frequencies (b, right)

From this results, the Schottky electrode bias dependence of the hole carrier concentration can be explained as follows: In the sub-threshold region, when applied voltage (V_a) is higher than threshold voltage (V_T), the hole channel under the electrode is empty and measured capacitance is the series of connected gate insulator and depletion layer capacitance. As V_a approachs V_T, the depletion region decreases so that when $V_a=V_T$ hole accumulation layer connects together ohmic and Schottky contacts. In forward bias condition, hole carriers are accumulated and capacitance saturates.

Figure 85a presents the capacitance behavior of standard diode structure for all the investigated frequencies that shows a capacitance value reduction with the frequency increase. Particularly interesting is the lower frequency behavior (Fig. 85b), in which device shows a steeply increase of capacitance in forward bias condition: this characteristic is seen in hetero-junction FETs or high electron mobility transistors under a higher forward V_{GS} and, according to literature, indicates that, because the energy-barrier height is finite, in this applied voltage range, the energy barrier becomes a triangular potential barrier penetrated by holes with the consequently capacitance second increase.

In figure 86 the frequency behavior of the measured capacitance for a standard diode structure, points out a sort of cut-off frequency around 10^6 Hz. Anyway, the low capacitance found for low or sub-threshold voltage values with the capacitance

reduction for higher frequency, enhance the perspective of RF high performances expected for hydrogen terminated diamond MESFETs.

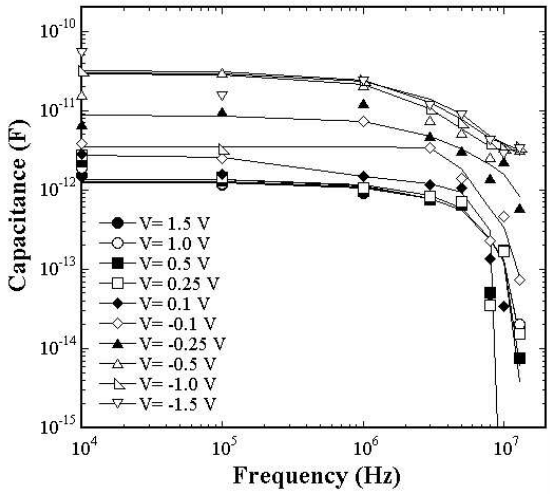


Figure 86 – Capacitance dependence on frequency for different applied voltages

From C-V measurements, carriers concentration profile could be easily approximately estimated according to:

$$N(x_d) = \frac{2}{q\varepsilon_s}\frac{1}{\partial C^{-2}/\partial V} = -\frac{C^3}{q\varepsilon_s}\left(\frac{\partial C}{\partial V}\right)^{-1}$$

where x_d is the depletion region width, approximately equal to ($\varepsilon_0\ \varepsilon_r/C$) where ε_0 is the vacuum dielectric permittivity and ε_r the substrate material relative dielectric constant.

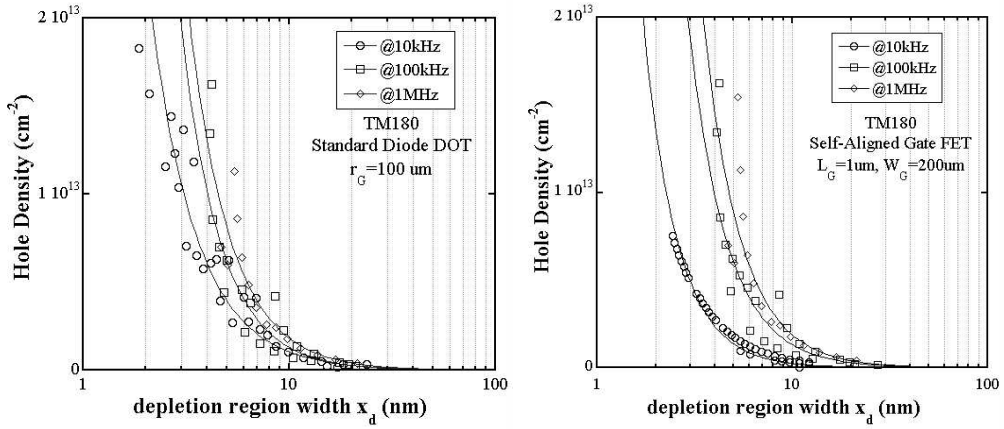


Figure 87 – Hole density dependence on depletion region width for a standard diode (a, left) and for a self aligned diode (b, right)

Figures 87a and 87b show the hole density profiles of the standard diode and self-aligned structure respectively. As expected, hole density maximum is not dependent on

structure but only on hydrogen termination: samples, hydrogen terminated with the same process point out similar hole density value around 1-2×10^{13} cm^{-2}, absolutely according Hall bars measurements previously presented results. Both plots remarks the maximum of hole density few nanometers below diamond surface and carriers are essentially confined in 10 nm, gradually disappearing above x_d higher than 20 nm. Such a confinement is shorter than De Broglie wavelength for holes in diamond (about 100 Å), a condition that points out a two dimensional density of states for hydrogen terminated surface.

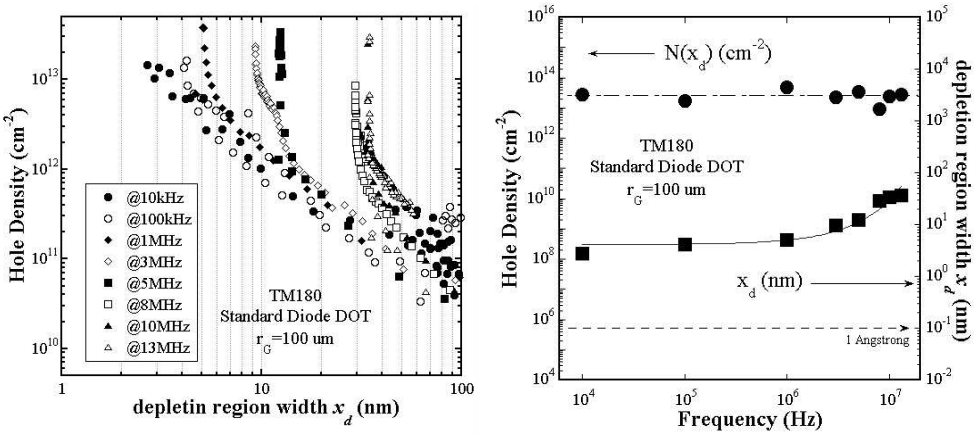


Figure 88 – Hole density as a function of depletion region width (a, left) and hole density and xd behavior as a function of frequency

Figures 87 highlight the depletion region width dependence on frequency, probably due to accumulation phenomena in the channel probably due to carriers velocity approach to saturation. Such a behavior, more deeply studied for the standard diode TM180 St. DOT (Fig. 88a), points out a channel re-population around x_d=30 nm: the formed hole channel could be supposed to extend to substrate, giving actually rise to an presumable three dimensional density of states. It is worth to notice that carriers density remains basically the same in the analyzed frequency range (Fig. 88b), while depletion region width fits to and exponential trend.

Combining results achieved for I-V and C-V characterizations, channel field effect mobility could be obtained according to:

$$I = \frac{1}{2}\mu C \frac{W}{L}(V_a - V_T)^2$$

And so, easily:

$$\mu = \frac{2}{C}\frac{L}{W}\left[\partial\sqrt{I}\Big/\partial(V_a - V_T)\right]^2$$

Figure 89 presents the field effect channel mobility as a function of carriers density. The maximum of field effect mobility is around 50 cm^2/vs, according to polycrystalline

values achieved with Hall bars measurements. In figure 90, trends remarked in figure 89 appear more evident, in correspondence of applied voltage (V_a).

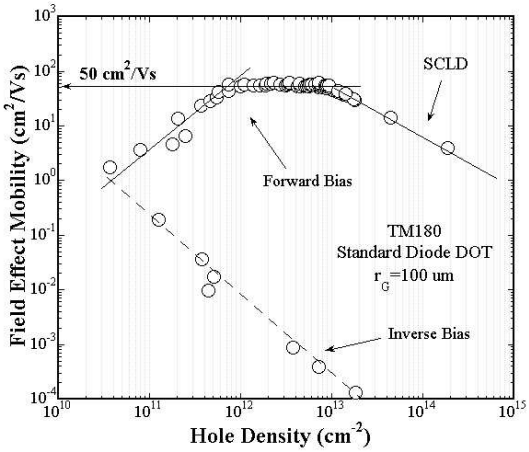


Figure 89 – Field effect mobility behavior as a function of hole density

A very low mobility is obviously noticed in inverse bias conditions, values that increase from threshold voltage V_T, to find a maximum in effective forward bias conditions. When space charge limited current regime occurs, mobility starts decreasing.

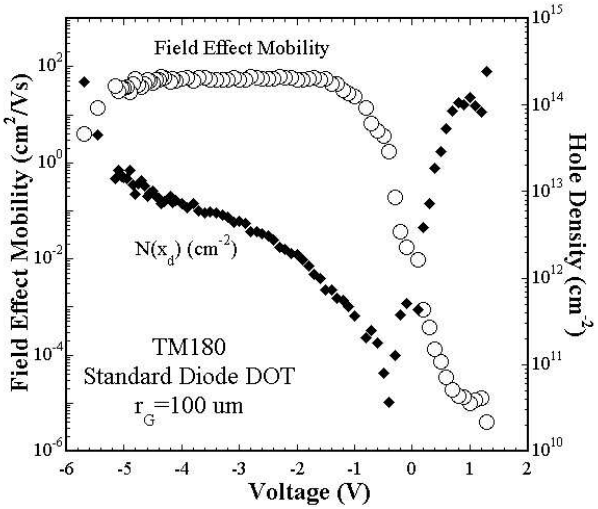


Figure 90 – Field effect mobility and hole density behavior dependence on applied voltage

Very interesting is the carriers density behavior: in forward bias, hole density increases remarking an enhancement-like behavior of the junction. Moreover, in inverse conditions, hole density increases as well, even if mobility values are very low: this could be explained as a change of active carriers in the junction, a sort of carriers concentration active in the bulk diamond. Such a hypothesis could be applied also to

the forward bias values higher than the supposed breakdown voltage in forward bias condition, in which, as already said, a bulk conduction could occur.

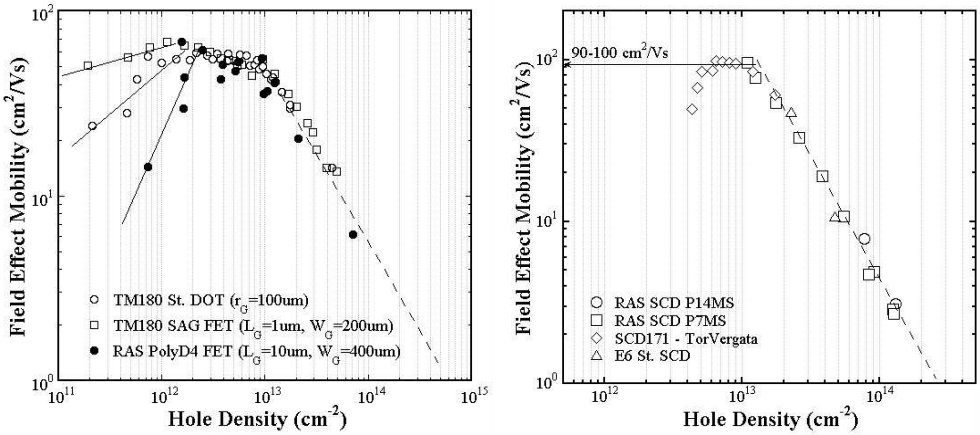


Figure 91 - Field effect mobility behavior as a function of hole density for polycrystalline diamond plates (a, left) and for single crystal diamond samples (b, right)

Figure 91, in conclusion, clearly remarks that such a mobility dependence on hole density is typical of hydrogen terminated surface based devices. Figure 91a shows three polycrystalline diamond based diodes in forward bias condition: mobility values are very similar, as expected, and the different behavior for low carriers concentration could be due to grain boundaries scattering, different in each one because of different surface morphology. The same trend has been found for different single crystal diamond based devices where, even if few data has been achieved for these structures, mobility values are higher. Data achieved in these sense confirm hydrogen termination dependence on substrate quality.

3. Ohmic Contact

Ohmic contact represent probably the most critical point, up to now, for MESFETs technology and at the same time, the first limitation to device performances. Of course, the introduced trick of hydrogen terminated area reduction beneath gold layer decreases leakage currents and increase contact stability. Few experiments with other contact concepts are actually encouraging and open the road to a technology change. Here data achieved by Transfer Length Method during this thesis will be reported and discussed. Figure 92 summarizes sheet resistance (R_S) values achieved for different diamond samples. Measurements have been performed by Keithely current supplier 6221 matched with Keithley 2182A nano-voltmeter.

Sheet resistance results higher for polycrystalline diamond samples, according to previously presented mobility data. It is important to remark that sheet resistance

values achieved for RAS polycrystalline samples has been obtained with another measurement setup.

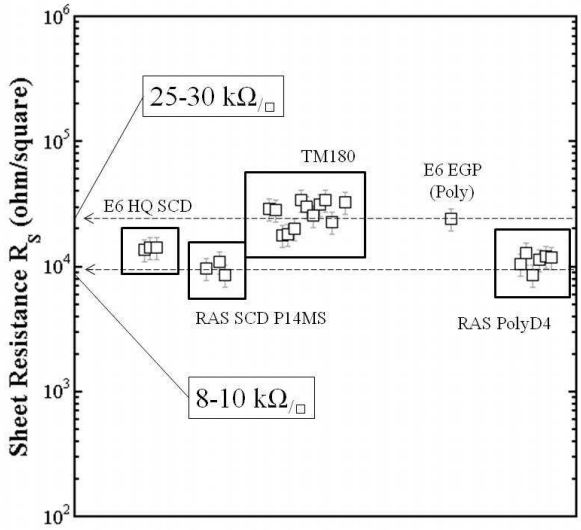


Figure 92 – Sheet resistance achieved for different diamond samples

Single crystal diamonds show lower sheet resistance. In figure 93, contact resistivity ρ_C values achivied for ohmic contacts fabricated with different recipes are presented. It is immediately possible to notice the high instability of gold ohmic contacts. Medium value could be considered 5-10×10^{-5} Ωcm^2, very high but sufficient for a good device operation. DlC/Pt/Au and TiC/Au result in lower values, but the case record is not enough to discuss a trend. Anyway, transfer length L_T results from TLMs characterization almost always smaller than 1 µm.

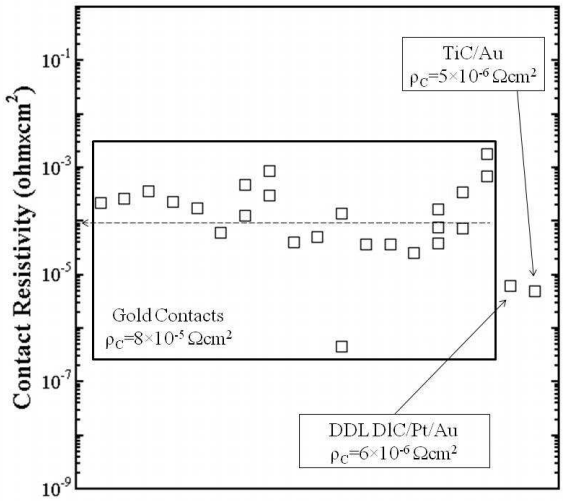


Figure 93 – Contact resistivity obtained from different contact metallization

In conclusion, ohmic contact needs a technology effort for improvements, not only as far as it concerns mechanical stability and strength, but also in the sense of a lowering of contact resistivity in order to reach values comparable with other well established technologies. Sheet resistance values achieved, agree to mobility discussed behaviors. It is important to remark that such R_S measured data are obtained with TLMs characterization and agree with data obtained with Hall bars measurements and data obtained from the discussion on the gate junction, absolutely different characterization techniques and different measurement setups.

4. MESFETs DC Characterization

4.1. Input Characteristics

MESFETs DC performances have been measured by means of HP 4140B picoammeter. Data presented in the following have published and discussed in few papers during this thesis work: here the author will report them for completeness. Relevant results will be briefly discussed in order to remarks differences and analogies between devices fabricated with self-aligned and standard gate technique; between the first GaN based layout and the diamond optimized structure. Figure 94b shows the input characteristics improvement obtained for FETs fabricated with standard technique using the diamond based RF layout (see section 5, chapter 2) compared to a similar structure with first non-optimized layout (Fig. 94a).

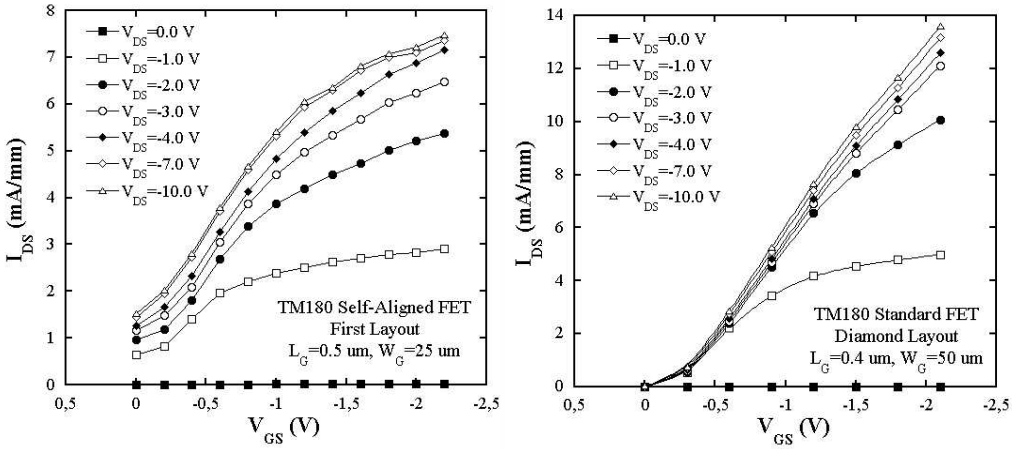


Figure 94 – Input characteristics of a self-aligned gate FET (a, left) and of a standard gate FET (b, right) with L_G=500 nm

Higher current values results in figure 94b in the same bias conditions of figure 94a, with higher linearity in saturation region and an evident threshold voltage reduction. Such an improvement could be due to sub-threshold currents reduction (hydrogen termination is smaller around active area) and a better impedance matching.

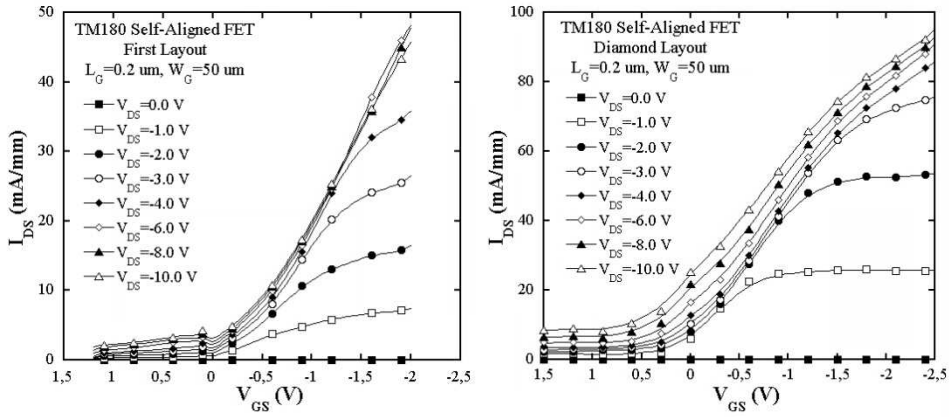


Figure 95 - Input characteristics of a self-aligned gate FET (a, left) and of a standard gate FET (b, right) with L_G=200 nm

Higher current densities have been always found for self-aligned gate FETs (Fig. 95). Also in this case, new layout ensures higher currents values (Fig. 95b) even if sub-threshold current results lower in the first layout FET (Fig. 95a): probably it is only an effect due to the very high currents and the small gate length. In addition, almost linear trend of input characteristics, noticed for smaller gate length, points out short channel effects.

4.2. *Transconductance* g_m

Transconductance is obtained from input characteristics as $g_m=(dI_{DS}/dV_{GS})$. Results achieved for standard structure FETs are presented in figure 96a and 96b.

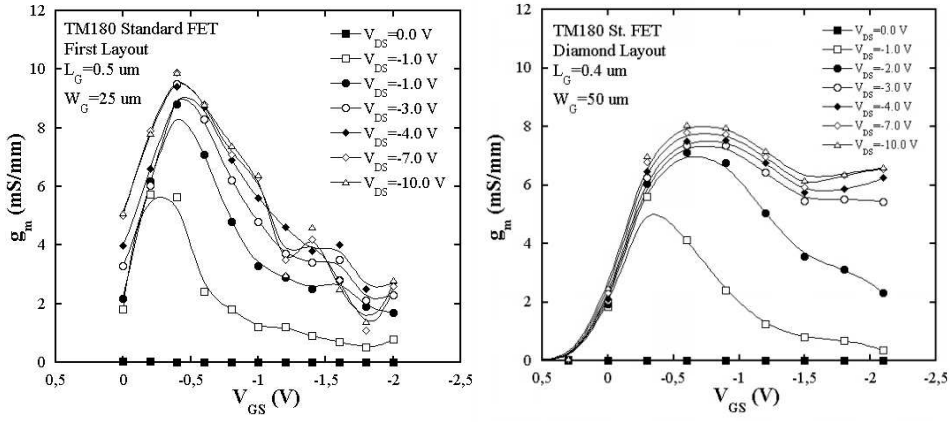


Figure 96 - Transconductance of a standard gate FET (a, left) and of a self-aligned gate FET (b, right) with L_G=400 nm

The peak for the standard structure with first layout (Fig. 96a) results in 10 mS/mm while the new layout FET only achieves 8 mS/mm (Fig. 96b), strange behavior that could be brought back to the larger gate width so that different scattering at the grain

boundaries is active in the gate region. Self-aligned gate FETs achieved extremely higher transcondutance values, due obviously to the smaller gate-drain and gate-source distances, with very similar g_m maximum of 34 mS/mm for first layout based FET (Fig.97a) and 43 mS/mm for the new structure (Fig. 97b).

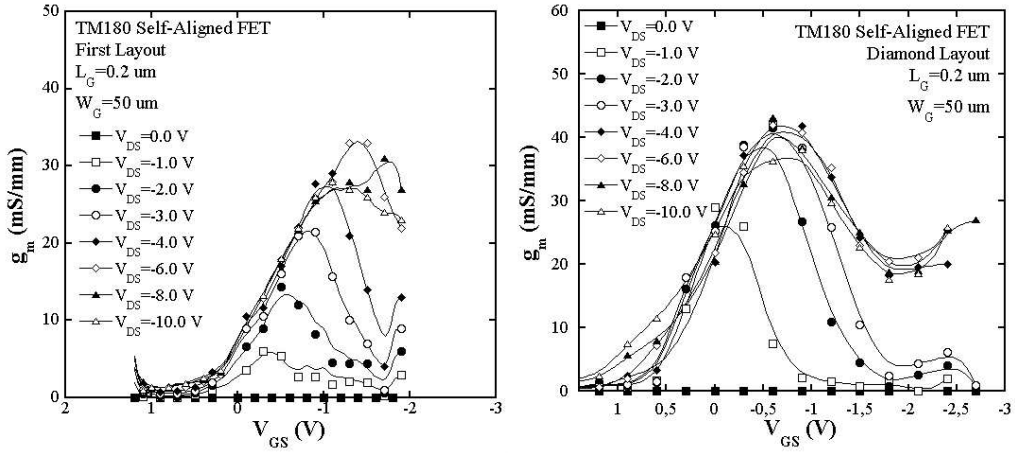


Figure 97 - Transconductance of a standard gate FET (a, left) and of a self-aligned gate FET (b, right) with L_G=200 nm

Most of analyzed transistors show the presence of a second peak for higher gate-source voltages and it is worth to notice the shift of g_m peak toward higher V_{GS} in dependence of applied drain-source voltage V_{DS} (Fig. 98).

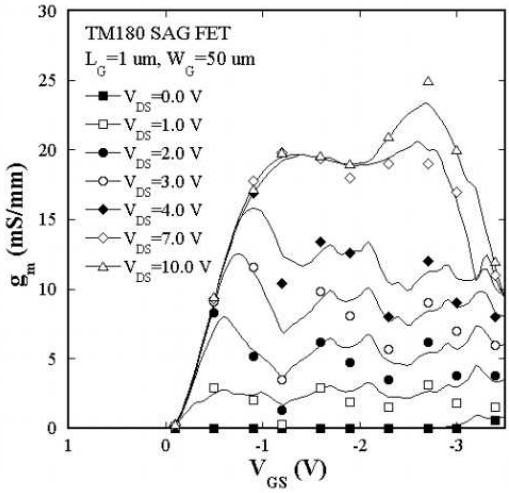


Figure 98 – Transconductance of a self-aligned gate FET with L_G=1 µm, showing a second peak

Such a shift is typically noticed in high electrons mobility transistors based on two dimensional channels and the remarkable second peak could be hypothesized as the

population of the second energetic state of the two dimensional hole gas induced by hydrogen termination. Another possible cause of such charge increase might be due to holes entrapped to grain boundary below the channel are emitted by field assistance in such a way contributing to the channel current.

4.3. Threshold Voltage V_T

Devices analyzed in this thesis work have been found to demonstrate a quasi-enhancement behavior with a threshold voltage between -0.3 V and 0.3 V. Short channel effects seem to occur beneath 0.5 µm gate length, pointing out the typical induced threshold voltage shift: devices with L_G=0.2 µm usually show V_T closely to 1.0 V. Data will not be shown but from input characteristic already presented in previous sections, it is possible to see how threshold seems to depend basically on gate length.

4.4. Output Characteristics

Output characteristics of MESFETs are plotted as I_{DS}-V_{DS} in figure 99a and 99b for standard technique fabricated devices with first and new layout respectively. First layout based MESFET shows a higher current density value of about 25 mA/mm, anyway very similar to the one presented by new layout based transistor. However, figure 99b remarks a better channel modulation and saturated operation for newest FET that does not show parallel resistance effects.

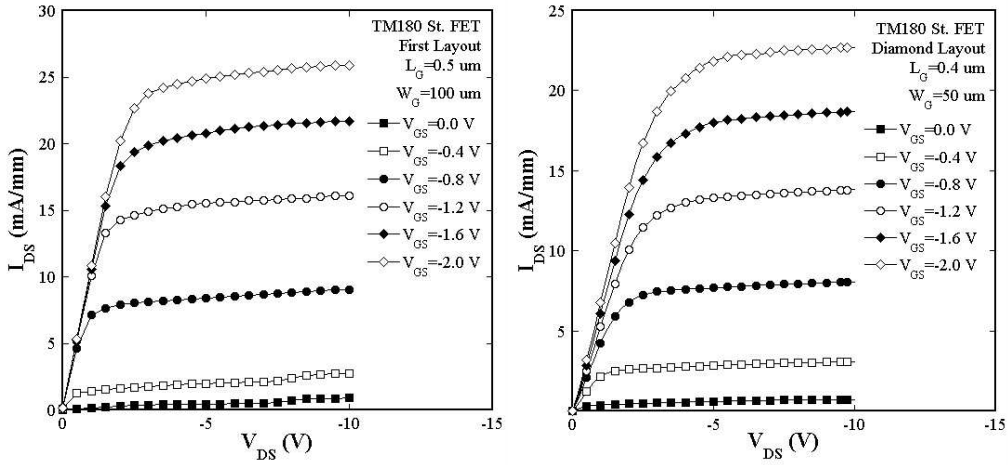


Figure 99 – Output characteristics of two standard gate FET fabricated with first layout (a, left) and with diamond optimized layout (b, right) with L_G=500 nm

Self aligned devices output characteristics are presented in figure 100a and 100b for the two analyzed layouts, respectively. Such devices result in higher current density,

obviously due to smaller geometrical channel length. Diamond based layout FET shows better maximum current value, up to 40 mA/mm with a lower R_{ON}. channel modulation appears to be very good for both devices.

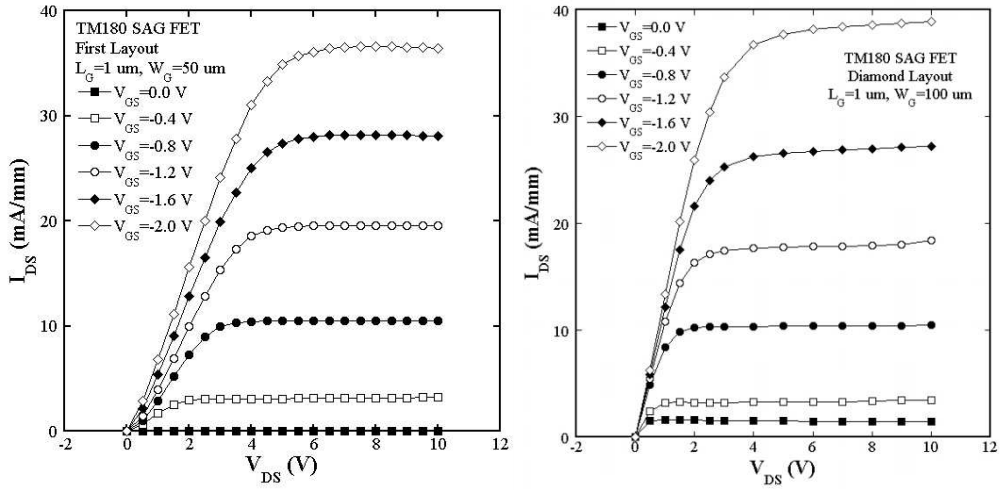


Figure 100 - Output characteristics of two self-aligned gate FET fabricated with first layout (a, left) and with diamond optimized layout (b, right) with L_G=1 µm

The measured DC output characteristics clearly show that in the linear region the drain current is almost independent of V_{GS}: when output conductance for V_{DS} approaches 0.0 V, it is not controlled by the gate voltage, contrasting what happens in conventional FETs. This phenomenon could be related to the fact that the channel charge-control model exhibits, after a region where the sheet hole density linearly depends on V_{GS}, saturation of the channel mobile charge for large V_{GS} absolute values.

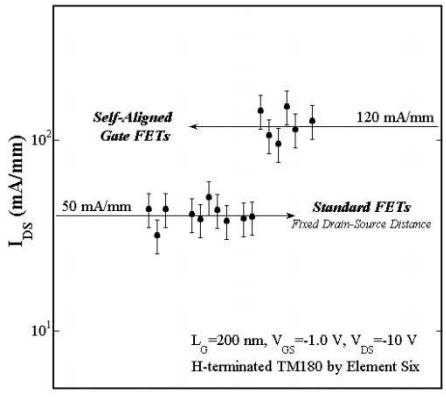


Figure 101 - statistic for 200 nm gate length transistors FETs fabricated on hydrogen terminated TM180

Within the framework of a device model based on the gradual channel approximation, due to the interplay between the gate and drain potential, the saturated

charge-control model yields the typical saturated trans-characteristics shown in previous paragraph. Such a charge-control model exhibiting saturation is formally similar to the *tanh* control model proposed for AlGaAs/GaAs HEMTs by Rodin and Roblin[212].

Presented results indeed suggest that this HEMT-like charge-control model can be effectively exploited, together with multi-bias scattering parameter measurements, to develop large-signal models based on the Chalmers approach[213].

Figure 101 presents a statistic for 200 nm gate length transistors FETs fabricated on hydrogen terminated TM180. Normalized current density values in bias condition V_{GS}=-1.0 V and V_{DS}=-10.0 V have been plotted: standard FETs achieve a medium value of 50 mA/mm and self-aligned FETs approach 120 mA/mm. For effective geometrical factor W_G/L_G, L_G has to considered as the drain-source distance, so that a self-aligned 200 nm gate electrode results in an effective L_G=1.8 µm (according to section 6.4, chapter 2). Standard FETs have been fabricated with a fixed drain-source distance of 4 µm: ratio of the two effective gate lengths explains the current densities difference.

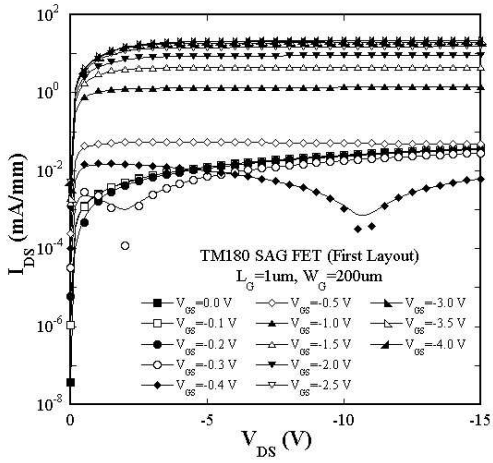


Figure 102 – Output characteristics of a 1 µm self aligned gate length diamond FET

Remarkable behavior of output characteristics is pointed out by a logarithmic plot, here represented for brevity only by figure 102. Close to threshold voltage, very low normalized currents have been found, demonstrating that the concentration of residual acceptors in the diamond is extremely low. The peaks observed for lowest gate-source voltage could be associated to a sort of built-in voltages related to carriers change for inverse bias conditions.

Figures 103a and 103b show the best I_{DS}-V_{DS} characteristics obtained in this thesis for hydrogen terminated diamond. Polycrystalline and single crystal diamond samples, one from Element Six Ltd and the other form Russian Academy of Sciences, respectively, result in a maximum drain to source current of about 120 mA/mm. It is

worth to notice that applied drain voltage for single crystal diamond is 80 V, corresponding to an applied electric field of more than 2 MV/cm, very high but still far from expected breakdown of 10 MV/cm. Maximum transconductance of such a device exceed 70 mS/mm. In both cases, devices are not affected by self-heating effects that typically occur in wide band gap semiconductors devices. Expected power density is over 2 W/mm for single crystal diamond.

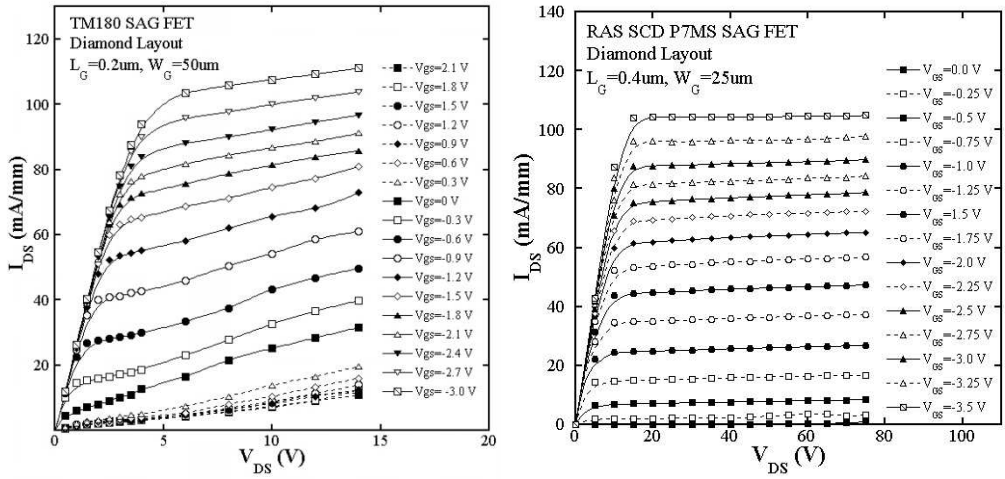


Figure 103 – best results achieved for output characteristics for polycrystalline diamond (a, left) and single crystal diamond (b, right)

In conclusion, DC characteristics of hydrogen terminated diamond based MESFETs are essentially dependent on drain to source channel distance and so, self-aligned gate technique based FETs typically show higher current densities. Hydrogen terminated area reduction does not affect performances. Optimized layout basically affects devices, even if, as already said, fabrication technique is the most decisive parameter: self-aligned gate FET result in higher current and transconductance values.

5. MESFETs RF Performances

Field effect transistors based on hydrogen terminated diamond fabricated in this thesis have their first obvious application in the microwaves because of the unmatched physical properties of diamond, especially the very high breakdown electric field, high carriers mobility and saturation velocity together with the low dielectric constant. In addition, the unequalled thermal conductivity, even higher than copper, allows diamond based devices to avoid self-heating effects that typically affect GaN and other wide band gap materials.

RF performances of devices fabricated in this thesis are steadily in the range of S and X bands of the radio spectrum, pointing out many times higher performances up to

K band. Such encouraging results allow devices to operate as satellite television broadcasting, microwave relays, WiMAX, inter-satellite links, high resolution radars, directed-energy weapon and security screening applications.

Achieved results will be presented in the following firstly for small signals and then for large signals. Such characterizations have been carried on in collaboration with the group of prof. E. Limiti at Tor Vergata University in Roma and with the group of prof. G. Ghione at Politecnico di Torino, respectively.

Also in this case, data achieved for different technological structures fabricated on low quality TM180 diamond plates will be discussed and results obtained on higher quality substrates will be presented for completeness. It is worth to notice that RF performances are deeply affected by substrate quality, for example because of the grain boundaries induced scattering.

5.1. RF Small Signal performances

Small signal characteristics have been measured in collaboration with Tor Vergata University group of Electronic Engineering Department. Characterization has been performed in the range 40 MHz-40 GHz by means of HP8510C and Anritsu 37397D Vector Network Analyzers, a Cascade RF1 Probe Station equipped with coplanar Ground Signal Ground (GSG) Probe GGB Picoprobe (with pitch of 200 μm) and CS5 Calibration kit (even if a diamond based calibration kit is eventually available).

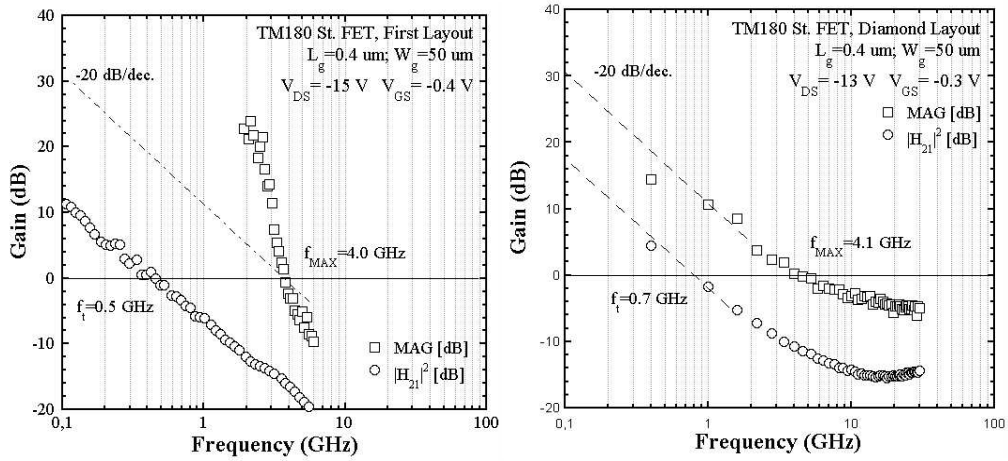


Figure 104 – Frequency dependence of maximum oscillation frequency (MAG) and current gain ($|H_{21}|^2$) for 0.4 μm standard gate length FETs fabricated with first (a, left) and RF optimized layout (b, right)

Figure 104a and 104b show frequency dependence of Maximum Available Gain (MAG) current gain $|H_{21}|^2$ for two 0.4 μm gate length FETs fabricated on TM180 by Element Six with previously realized layout and diamond based structure, respectively, both based on the standard gate technique. Gate periphery is the same for both devices

and bias conditions are comparable. Maximum oscillation frequency f_{MAX} is completely comparable.

The improvement achieved by means of the diamond based layout is the higher current gain cut-off frequency f_T of 0.7 GHz instead of 0.5 GHz: the better impedance matching allows device to gain at higher frequencies.

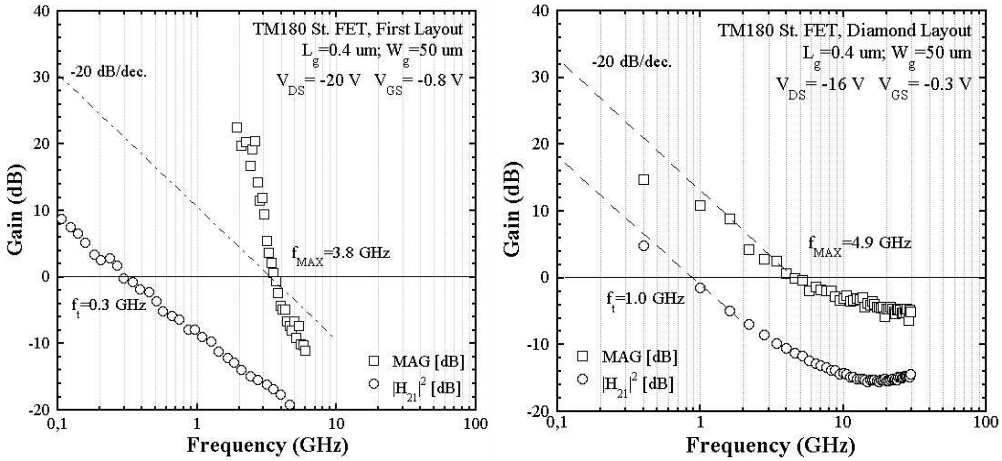


Figure 105 - Frequency dependence of maximum oscillation frequency (MAG) and current gain ($|H_{21}|^2$) for 0.4 µm standard gate length FETs fabricated with first (a, left) and RF optimized layout (b, right)

The improvement introduced by optimized layout is more evident in figure 105a and 105b, where the same previously shown FETs are presented for higher applied drain to source voltage V_{DS}: in this case, also f_{MAX} shows an evident improvement, from 3.8 GHz up to almost 4.9 GHz while f_T improves of 0.7 GHz. Increasing V_{DS}, the RF optimized layout creates the conditions for better performances.

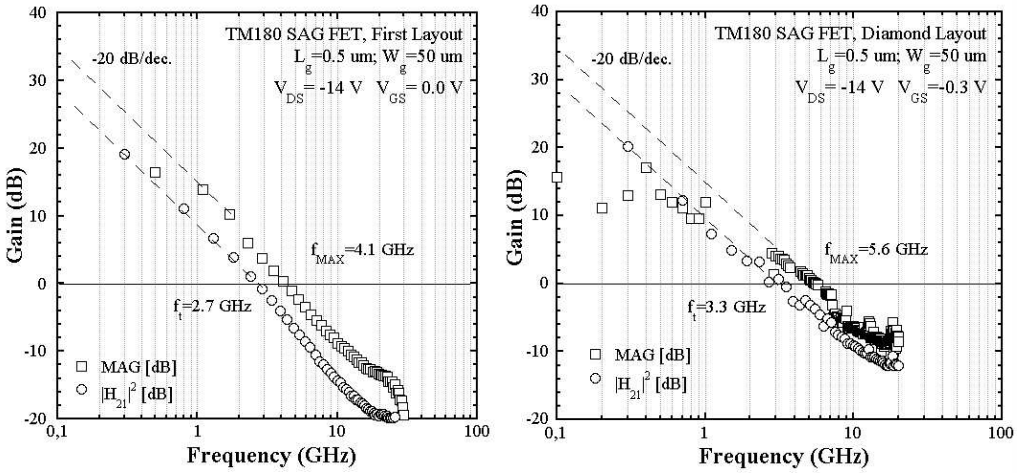


Figure 106 – Frequency dependence of maximum oscillation frequency (MAG) and current gain ($|H_{21}|^2$) for 0.5 µm self-aligned gate length FETs fabricated with first (a, left) and RF optimized layout (b, right)

Current gain presents the typical -20 dB/decade dependence on frequency while for MAG, this behavior is achieved only for high frequency values: K, the Rollet' stability factor, is less than 1 for low frequency so that device has to be considered unstable in that range. It is important to notice that devices fabricated with new layout also include the hydrogen terminated area reduction that seems to does not affect negatively FETs performances.

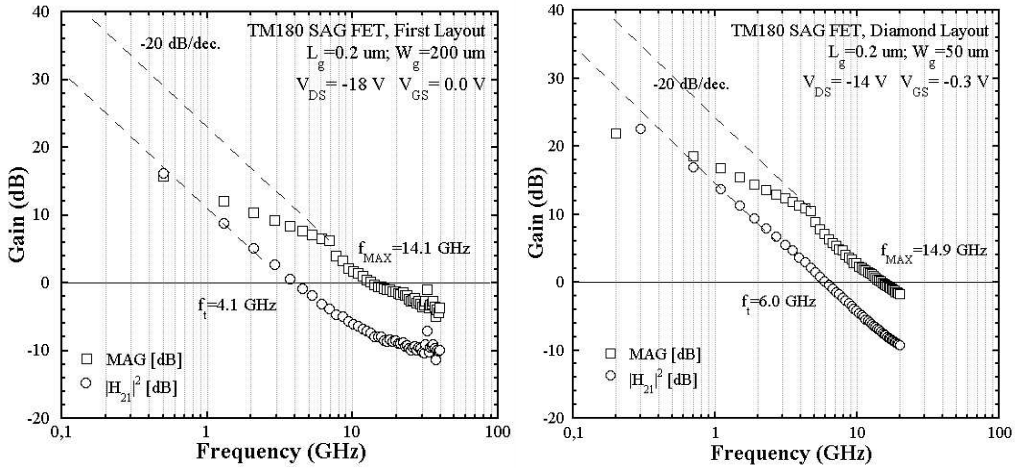


Figure 107 – Frequency dependence of maximum oscillation frequency (MAG) and current gain ($|H_{21}|^2$) for 0.2 µm self-aligned gate length FETs fabricated with first (a, left) and RF optimized layout (b, right)

Self-aligned gate FETs behavior in dependence of frequency is shown in figures 106a and 106b for devices with a 500 nm gate length and 50 µm gate width. Cut-off frequencies for current gain presents an improvement for similar bias conditions, from 2.7 GHz to 3.3 GHz while maximum oscillation frequency shifts form 4.1 GHz up to 5.6 GHz. The higher frequencies, compared with shortest gate length devices fabricated with standard technique, are due to the smallest drain to source distance. Also in this case, the new layout is associated with a hydrogen terminated area reduction with no evident negative effects. The stability of devices for low frequencies is still not reached. Smallest self-aligned gate devices fabricated on TM180 during this PhD thesis present a 200 nm gate length. RF performances of such FETs are shown in figure 106a and 106b for first and new layout, respectively. Gate reduction obviously leads to a higher cut-off frequencies, up to almost 15 GHz for maximum available gain. A current gain cut-off frequency f_T of 4 GHz has been achieved for first layout based FET (Fig. 107a), while it raises up to 6 GHz for the RF optimized structure (Fig. 107b). The bias condition in which the maximum f_{MAX} and f_T has been obtained is near the pinch-off region, which seems to be a unique characteristic of diamond FETs. Figure 108a shows a gate bias scan of these cut-off frequencies at a constant drain bias V_{DS} of 14 V for self-aligned gate FET with a 200 nm gate length.

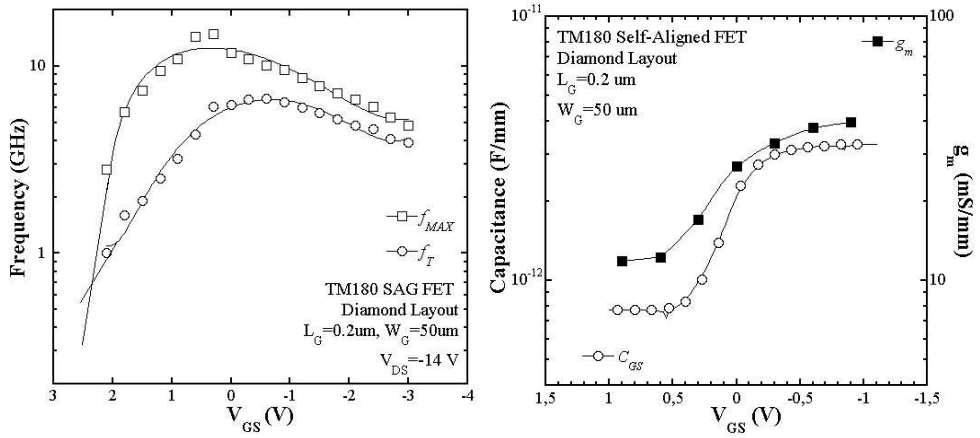


Figure 108 – Cut-off frequencies (a, left) and g_m and C_{GS} (b, right) dependence on gate bias

Form figure 108b it is possible to see that C_{GS} is rather constant across a wide gate bias range, indicating that the FET mode of operation is similar to that of a hetero-junction FET with constant gate barrier to channel separation. Near pinch-off C_{GS} decreases faster than g_m: the behavior of input capacitance (C_{GS}) and intrinsic trans-conductance (g_m), which are the essential part of f_T and f_{MAX}, are shown in figure 108b. It can be hypothesized that near pinch-off the hole channel charge is pushed into the substrate buffer layer down into a region of higher mobility. Residual DC current injection into this buffer layer and residual bypass conduction are indeed observed in DC characteristics, basically sub-threshold currents. Therefore, bulk conduction, as well as surface morphology, affects RF characteristics.

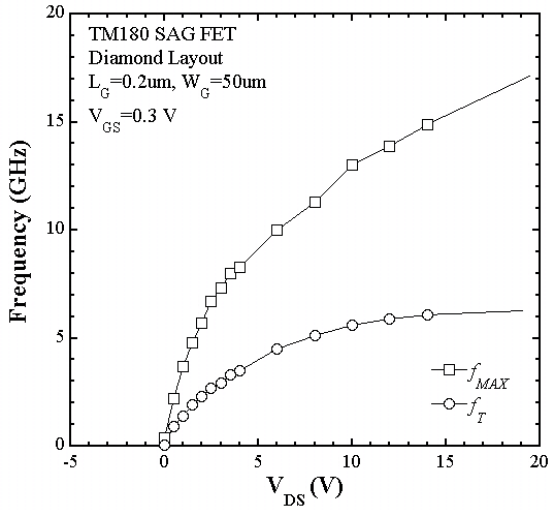


Figure 109 – Cut-off frequencies dependence on applied V_{DS}

RF small signal performances behavior of devices for a constant V_{GS} and scanning drain to source voltage V_{DS} is presented in figure 109. Cut-off frequencies increase

according to drain source applied electric field, suggesting that charge carriers saturation velocity is not reached yet.

Absolutely similar behavior have been found in this thesis for self-alinged gate FETs and for standard FETs fabricated on different diamond samples, both single crystal and polycrystalline, both high and low quality samples. As well as single crystal diamonds show a better DC behavior in terms of maximum achieved values, so that polycrystalline diamonds present higher RF performances in terms of cut-off frequencies. The reason of this strange trend is still not clear also in literature. It is possible that the presence of grain boundaries allows polycrystalline diamond to the bulk conduction, helped by surface scattering phenomena to higher mobility states.

Following figures 110a and 110b show the better results achieved in terms of cut-off frequencies during this three years work and already published in many papers[214,215,216].

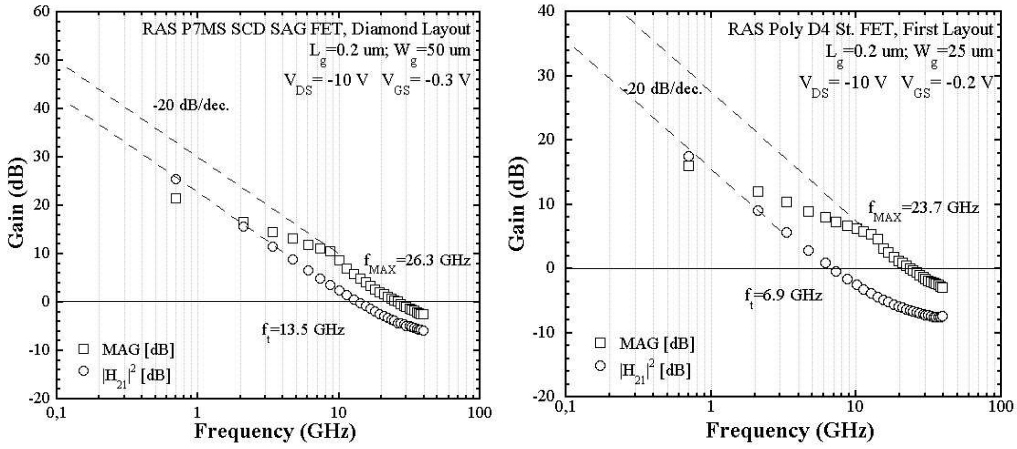


Figure 110 - Frequency dependence of maximum oscillation frequency (MAG) and current gain ($|H_{21}|^2$) for 0.2 µm gate length FETs fabricated on single crystal (a, left) and polycrystalline diamond (b, right)

Figure 110a presents the frequency performances of a self-aligned 200 nm gate length FET fabricated on a high quality homoepitaxial layer by Russian Academy of Sciences. Device is bias with a V_{GS}=-0.3 V and V_{DS}=-10 V resulting in a drain-source current of 1.5 mA (gate width is 50 µm). Maximum oscillation frequency f_{MAX} achieved with an RF optimized layout is 26.3 GHz while current gain cut-off frequency f_T is 13.5 GHz.

A 200 nm gate length standard FET (with asymmetrical gate, effectively comparable with a self-aligned gate FET) fabricated on a high quality large-grain size polycrystalline diamond by Russian Academy of Sciences achieves an f_{MAX} of 23.7 GHz and a f_T of 6.9 GHz (Fig. 110b). Bias conditions are basically the same as figure 109a, V_{GS}=-0.2V and V_{DS}=-10 V, resulting in a current of 0.8 mA (gate width is 25 µm instead of 50 µm). Same devices are presented for higher drain to source voltage V_{DS}=-

15 V while V_{GS} is -0.2 V in figure 111a and 111b, respectively. In this case, maximum oscillation frequency for single crystal diamond is 26.7 GHz while polycrystalline plate results exceed 30 GHz, according with literature results that give to polycrystalline diamonds the RF performances primacy. It is worth to notice that the same polycrystalline diamond based FET achieved an f_{MAX}=35 GHz when V_{GS}=0.0 V and V_{DS}=-35 V.

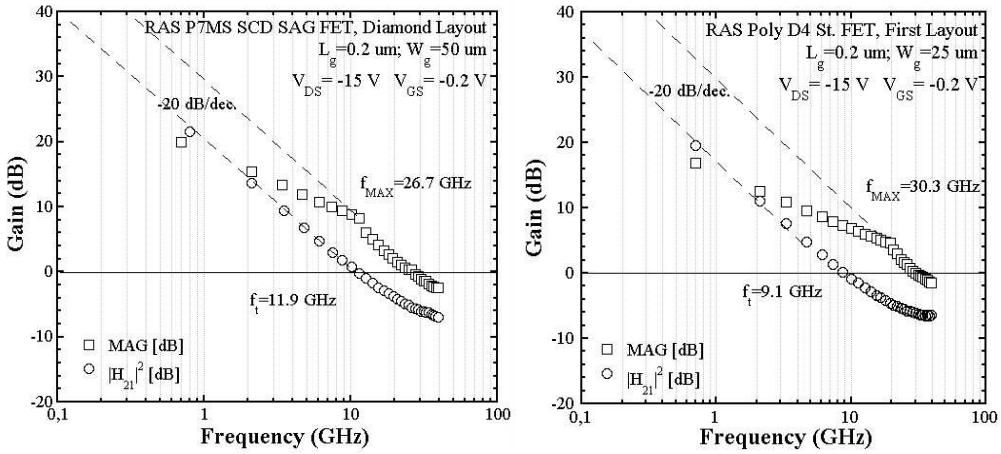


Figure 111 - Frequency dependence of maximum oscillation frequency (MAG) and current gain ($|H_{21}|^2$) for 0.2 µm gate length FETs fabricated on single crystal (a, left) and polycrystalline diamond (b, right)

Current gain cut-off frequencies obtained are 11.9 GHz and 9.1 GHz for single crystal and polycrystalline diamond, respectively.

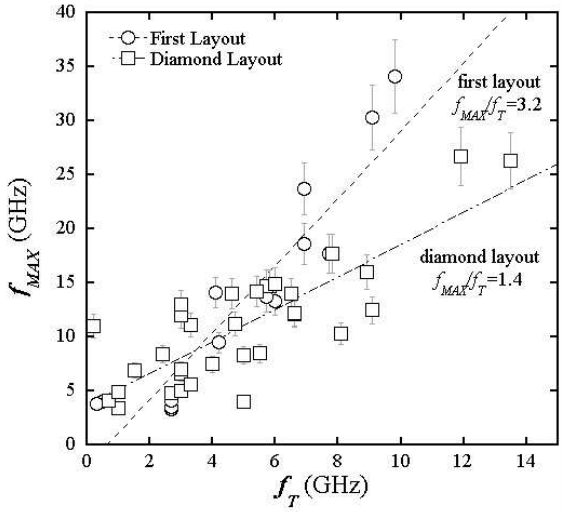


Figure 112 – f_{MAX} dependence on f_T for FETs based on first and on RF optimized layouts

The higher cut-off frequency achieved for single crystal diamond are due to the optimized layout (polycrystalline sample based device has been fabricated with the

previous structure) and to the absence of surface scattering induced by grain boundaries.

Anyway, in figure 112, it is clearly possible to see how the RF optimized layout introduction results in a lowering of the f_{MAX}/f_T medium ratio from 3.2 down to 1.4, leading to a more ideal and controllable FET behavior.

5.2. RF equivalent circuit

Also RF equivalent circuit has been extracted in order to get a better understanding of devices behavior. Such a modeling procedure has been applied to a self-aligned 1 µm gate length FET fabricated on an Optical Grade polycrystalline diamond by Element Six[217]. Gate width is 100 µm.

Figure 113 shows the S-parameters of analyzed device in Smith chart. S_{11} of the device, which represents the sum of the intrinsic resistance, the gate metal resistance and the source parasitic resistance, follows a constant resistance circle of 90 Ω. This resistance is mainly due to the high source parasitic resistance caused by the source–gate spacing. Other factors such as the intrinsic channel resistance and the gate metal resistance are ruled out, because the former is inversely proportional to the gate length and the latter hardly contributes to the total resistance due to the low-resistance material used (Al).

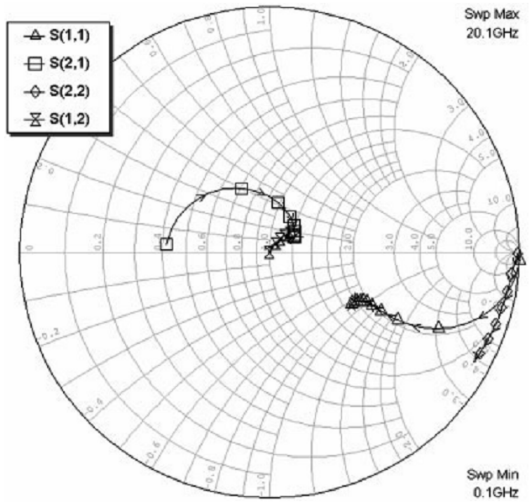


Figure 113 – S-parameters represented on Smith chart of a 1 µm gate length FET fabricated on an Optical Grade polycrystalline diamond by Element Six

Assuming a sheet resistance of 25 $k\Omega_{\square}$, the source–gate parasitic resistance is calculated to be 55 at a source–gate spacing of roughly 1 µm and a gate width of 100 µm. The high source–gate parasitic resistance stabilizes the operation of the MESFET over the range of measurement frequencies in spite of the narrow source–gate spacing.

The gate-source capacitance C_{GS} is calculated to be 0.5 pF from S_{11}. The depth of the depletion region under the Schottky gate is calculated to be 10 nm from C_{GS}. S_{22} shows low power loss at the device output due to the low dielectric constant of diamond, which is useful for microwave applications of diamond FETs. Because of the low dielectric constant of diamond, both reactances of S_{11} and S_{22} are low, which is advantageous in RF foreground as well. Because of high input and output device mismatch, S_{21} parameter magnitude is less than unity, but this not means that the device had no gain.

Table 5 - Intrinsic Elements

V_{GS}= -0.8V V_{DS}= -10V	V_{GS}= -2V V_{DS}= -10V	V_{GS}= 0.8V V_{DS}= -10V
C_{GS} (fF) =483.9831	C_{GS} (fF) =501.7142	C_{GS} (fF) = 12.0383
R_i (Ω) =88.0367	R_i (Ω) =66.0317	R_i (Ω) =1021.4
C_{GD} (fF) =9.1509	C_{GD} (fF) =21.2115	C_{GD} (fF) =6.1285
R_{GD} (Ω) =2850.2	R_{GD} (Ω) =1373.9	R_{GD} (Ω) =757.2259
g_m (mS)=3.7651	g_m (mS)=6.7179	g_m (mS)=0.005
Tau (ps)=19.367	Tau (ps)=11.041	Tau (ps) =8.8863
C_{DS} (fF) =1.7419	C_{DS} (fF) =2.2304	C_{DS} (fF) =0.5
G_{DS} (mS) =0.0807	G_{DS} (mS) =0.2363	G_{DS} (mS) =0

The starting small-signal equivalent circuit topology adapted was based on Dambrine model. This kind of equivalent circuit generally fits with FET physical structure and behavior. In this case we adopted a 16 elements small signal equivalent circuit where R_{GD} has been useful to represent device symmetry and improve experimental data fitting in low frequency and during transition from symmetric (low biasing) conditions to saturation region. However it has been necessary to introduce a current leakage representative resistance between gate and drain.

Table 6 – Parasitic Elements

C_{PG} (fF) = 24	R_G (Ohm) = 10	L_G (pH) = 60
C_{PD} (fF) = 26	R_D (Ohm) = 36	L_D (pH) = 25
C_{PGD} (fF) = 10	R_S (Ohm) = 45	L_S (pH) = 7

This element, usually describe surface trapping effect in HEMT device and in our case it, probably regards the same kind of effect or leakage effect induced by strong gate inverse polarization tunnel phenomenon. Starting from the achieved results a simple equivalent circuit model of diamond based MESFETs has been formulated keeping into account the basic parasitic elements of a FET, source (R_S), drain (R_D) and

gate resistances (R_G). Source and drain resistances are related to carrier density and mobility of the surface hole channel, hence to the hydrogenation conditions. Device geometry (source to gate and drain to gate distance) also determine resistance values. Best fit values for each component of the equivalent circuit are listed in table 5. MESFET extrinsic elements complete equivalent circuit definition (table 6). The proposed equivalent reproduce fairly well the frequency dependence of the measured S-parameters in all measurement frequency range. Figure 114 shows the RF equivalent model.

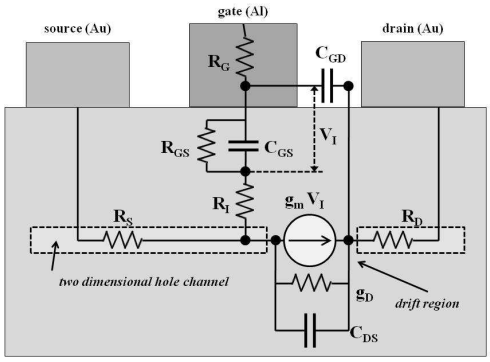


Figure 114 - Small-signal equivalent circuit of a 1 µm gate length FET fabricated on an hydrogen terminated Optical Grade polycrystalline diamond by Element Six

5.3. RF Large Signal performances

Large signal characteristics have been measured in collaboration with politecnico di Torino group of Department of Electronics. Generally, to evaluate RF power devices, power gain, efficiency, output power, and power density are measured using load-pull measurement as performance values. The load-pull measurement means varying or "pulling" the load impedance while measuring the performance of a device-under-test (DUT).

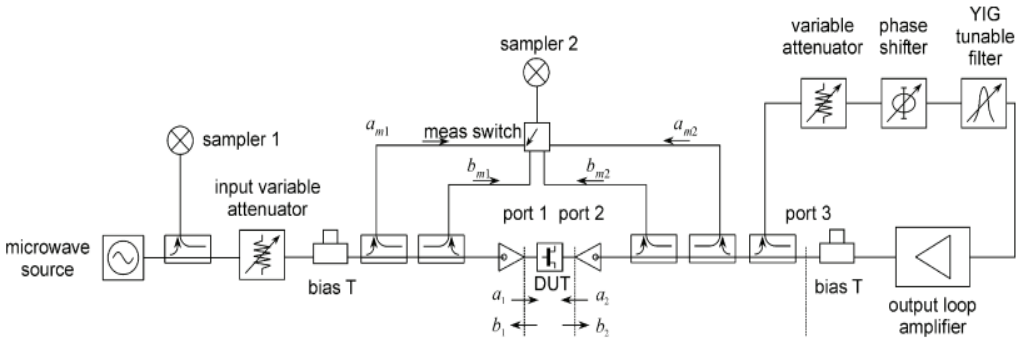


Figure 115 - Simplified scheme of the load/source-pull system with time-domain waveform capabilities of Politecnico di Torino.

In the load-pull measurement, the load impedance where the highest or lowest performance values can be obtained is directly determined by varying the load impedance over a wide range on the impedance plane on a Smith chart. This method is important for large-signal, nonlinear devices where the operating point may change with power level or tuning. The performance limitations can be evaluated using this method, and it has been used for designing peripheral circuits for discrete devices and monolithic microwave IC (MMIC).

The RF waveforms are measured in real-time at the DUT reference planes by means of a Vector Network Analyzer (VNA). The output loading conditions are changed at the fundamental frequency by means of the active loop, see figure 115. The active technique allows for reflection coefficients up to, or even above unity. This is a fundamental feature in the characterization of diamond based devices of small periphery, since their optimum loads typically exhibit a reflection coefficient with magnitude close to unity, that cannot be synthesized, due to losses, with conventional passive tuners.

A self-aligned gate FET with L_G=200 nm and W_G=50 µm fabricated on a TM180 by Element Six according to the RF diamond based optimized layout, has been tested for RF power performances, achieving the best result up to now present in literature for a polycrystalline diamond sample.

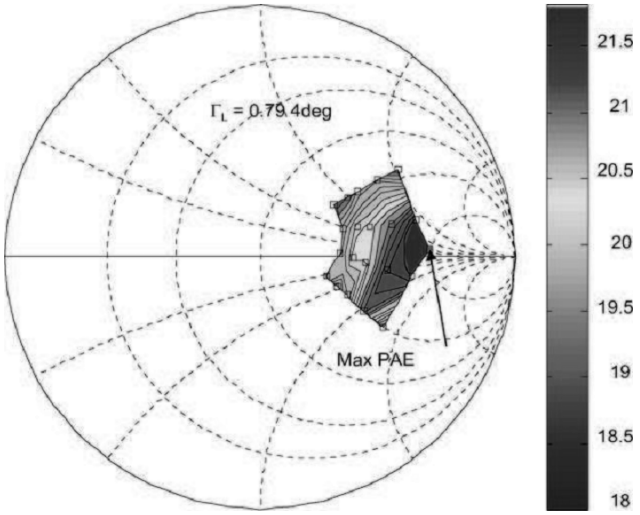


Figure 116 - Load-pull map of the 50 µm device operating at 2 GHz, and biased in class A (V_{DS}=-14 V and V_{GS}=-1 V). The marker shows the location of the optimum load for maximizing the PAE.

According to the load-pull approach, the optimum load can be investigated for several performances, typically the maximum power, the maximum power added efficiency (PAE), the minimum distortion (under a two-tone test). In this work optimum PAE has been considered the goal, taking into account that the power can be also increased by pushing the drain bias towards larger absolute values than 14 V. An

example of PAE load pull map is shown in figure 116; we found an optimal load for maximum PAE of Γ_L=0.79, phase 4°. As expected the optimum load has a small inductive reactive part compensating the output capacitance; due to the comparatively low frequency, however, the resistive part is dominant.

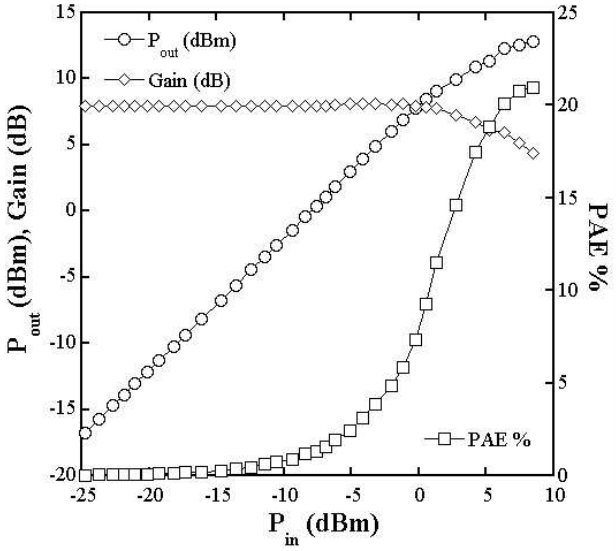


Figure 117 - Power sweep on the PAE optimum load (Γ_L = 0.79, 4°) in class A at 2 GHz. Power gain, output power normalized to 1 mm total gate periphery and PAE for V_{GS}=-1 V and V_{DS}=-14 V.

Fig. 117 shows the results of a power sweep for a 100 µm device, with the device terminated on the optimum load. The maximum output power density is 0.2 W/mm with 22% PAE, and linear power gain of 8 dB. Assuming a maximum drain current around 11 mA, the maximum output power value is compatible with a peak RF voltage around 9 V (consistent with the given bias and with a knee or saturation drain voltage of -5 V), which amounts to a maximum instantaneous drain voltage of -23 V. The theoretical value of the drain efficiency obtained with such values is around 30%, which further decreases to the PAE due to finite gain. Larger efficiencies could be reached by increasing the drain bias, but, as already mentioned, this could ultimately lead to irreversible device damage. During the large-signal load-pull characterization the tested devices underwent several RF power weeps (20–30) without any appreciable DC or RF performance degradation. DC degradation following RF test was reported for devices on single-crystal diamond[178] due to surface problems. Kasu and coworkers[218] observed a drain current degradation induced by increase of gate leakage during pulsed-DC tests. However, for the present device, any increase of gate current has been observed (which remained always lower than about 1 µA up to the maximum applied DC gate bias of -4 V) either under DC and RF measurements. Extensive reliability tests in single-crystal or polycrystalline diamond devices have not been reported yet as far as we know and were anyhow beyond the scope of the present work,

also considering that the contact technology exploited does not allow repeated measurements on the same device for probe scratching (for adhesion problems) and, as a consequence, any significant aging test.

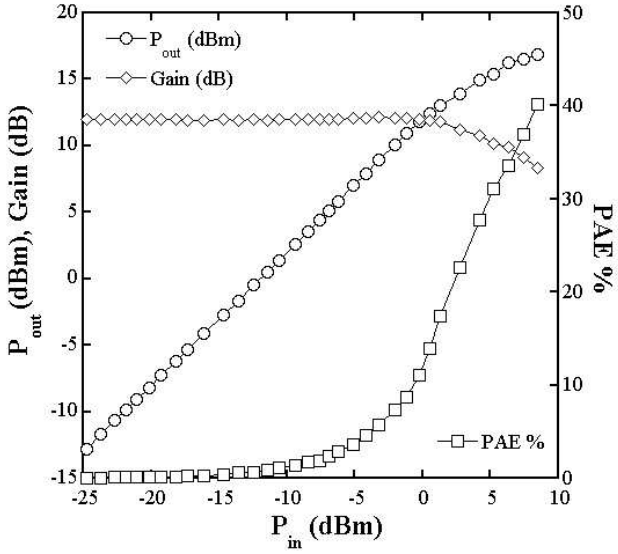


Figure 118 - Power sweep on the PAE optimum load (Γ_L = 0.79, 4°) in class A at 1 GHz. Power gain, output power normalized to 1 mm total gate periphery and PAE for V_{GS}=-1 V and V_{DS}=-14 V.

From the reported RF power characterization, the extrapolated output power density at 1 GHz is about 0.8 W/mm (Fig. 118); such value, though still much lower than the expected material limit, points out the potential of this technology on polycrystalline diamond when compared to the record performance of 2 W/mm on single crystal diamond[200] at 1 GHz.

Even if it was not possible up to now to perform temperature dependent measurements on fabricated FETs, literature states that the increase in temperature during power measurements on a single crystal diamond based FET with P_{out}=0.84 W/mm is only 0.64 °C. In the case of a GaAs MESFET with a similar output power of 0.6 W and a similar size and configuration, the increase in temperature of ~60 °C was reported. Compared with GaAs, the increase in temperature for diamond is extremely low. However, this is reasonable from physics principles. The increase in temperature is inversely proportional to the thermal conductivity. Since the thermal conductivity of diamond is 22 W/(cm K), ~50 times higher than GaAs (0.46 W/cmK), the increase in temperature for diamond should be ~1/50 that for GaAs. Actually, the upper limit of output power for GaAs and GaN devices is almost saturated due to heat spreading. However, for diamond devices, thermal management is not a serious factor limiting the output power.

Conclusions

Metal-Semiconductor Field Effect Transistors (MESFETs) based have been fabricated on Hydrogen terminated single crystal and polycrystalline diamond, supplied by Russian Academy of Sciences and purchased by Elements Six Ltd.

Sub-micron gate length transistors have been developed according to butterfly shaped layout, typical of RF oriented devices, that has been optimized keeping into account diamond physical and electronic parameters in order to achieve better performances. Improvements introduced by such a layout have been pointed out from devices characterization. Aluminum self-aligned and fixed drain-source distance ("*standard*") gates and gold ohmic contacts have been fabricated. Aluminum assures low ideality factor gate-source diodes, high rectification ratio and low leakage currents (anyway higher for polycrystalline diamond samples). The small L_T resulting from transfer length method (TLM) analysis, allowed the supposition of a completely lateral charge transfer so that the hydrogen terminated area dimension reduction close to gate junction results in a lowering of leakage currents and better gold adhesion to substrate without negative effects on device performances. Gold contacts, after a hard work of development and improvement, resulted in good mechanical strength as well as contact resistivity, lower enough to allow an excellent device operation.

Hydrogen terminated layer has been deeply investigated by means of Hall bars, TLMs and gate junctions characterization: hydrogen induced conductive layer results in sheet resistances essentially stable and repeatable, only dependent on substrate quality. From experimental evidences, such a conductive layer can be associated to a quasi-two dimensional hole gas (2DHG). Analysis carried out for many fabricated MESFETs, pointed out a different behavior of this 2DHG for DC and AC, respectively: it could be hypothesized an effective two-dimensional transport for in DC conditions, and other transport mechanism triggered on with oscillation. An effective increase of mobility is highlighted when devices are subject to frequency dependent signals that could be due to interaction between h-terminated layer and bulk diamond with higher holes mobility, giving raise a three dimensional transport. Anyway, it could be also explained as a priming of second quantum level of the 2DHG.

Results achieved for self-aligned and standard FETs fabricated on nominally identical large-grain size, low quality, polycrystalline diamonds TM180 by Element

Six have been presented and investigated in order to obtain a better understanding of hydrogen terminated diamond transistors. DC characteristics pointed out the presence of the 2DHG as well as an operation typical of hetero-junction FETs. Anyway, achieved results seem to highlight the presence of an effective insulating layer at the aluminum-diamond interface. Such a characterization show the primacy of the self-aligned gate structure: 200 nm gate length FETs show current density and transcondutance values of 100 mA/mm and 40 mS/mm, respectively. Higher values have been obtained on high quality single crystal plates by Russian Academy of Sciences, with an I_{DSmax} of 120 mA/mm, stable up to a V_{DS} = -80 V (corresponding to an applied electric field E_A = 2 MV/cm, still far from diamond nominal breakdown electric field) and a maximum transconductance exceeding 70 mS/mm. The absence of grain boundaries and surface scattering phenomena, in this case, limits sub-threshold and leakage currents; besides, hydrogen termination of single crystal plates results in lower sheet resistances (8-10 $k\Omega_{\square}$) and higher mobility (up to 130 cm^2/Vs at room temperature): 2DHG formation and surface transport are strictly dependent on the surface roughness and grains orientation. All devices fabricated in this thesis are not affected by self-heating effect, obviously because of the very high thermal conductivity of diamond.

RF small signal performances of fabricated FETs have been investigated for both self-aligned and standard devices fabricated on Element Six TM180 diamond plates. Established technology allows the fabrication of transistors with operation frequencies always in the X and C band of the radio spectrum, even if based on low quality substrates.

Self-aligned 200 nm gate length FETs fabricated on TM180 achieved a maximum oscillation frequency f_{MAX} = 15 GHz and a current gain cut-off frequency f_T = 6 GHz resulting in a power output at 1 GHz of 800 mW/mm that is, up to now, the best result in literature for polycrystalline diamond based transistors. Such a result is anyway comparable with well-established technologies like GaAs based transistors. From S-parameters analysis, it has been possible to extract a FET small signal model.

Best results in terms of operation frequencies have been obtained, also in this case, for single crystal and polycrystalline diamond plates supplied by Russian Academy of Sciences. Higher RF performances have been typically obtained close to the pinch.off region where the hole channel charge seem to be pushed into the substrate buffer layer down to a region of higher mobility. Single crystal plate achieved a f_{MAX} = 27 GHz and a f_T = 14 GHz when V_{DS} = -15 V and V_{GS} = -0.2 V and polycrystalline diamond exceed 30 GHz for maximum oscillation frequency while 9 GHz have been achieved for f_T. Completely satisfying reasons for polycrystalline diamond better performances, in terms of f_{MAX}, have not been found: probably such a trend is due, as already stated, to a sort of mobility increase owing to grain boundaries and bulk interface (bulk mobility in

diamond is 1600 cm^2/Vs). Results achieved in this thesis have pointed out the supremacy of the self-aligned gate structure and the development of an RF optimized layout specifically for diamond results in a DC characteristics improvement and a f_{MAX}/f_T ratio reduction that will lead to better RF performances.

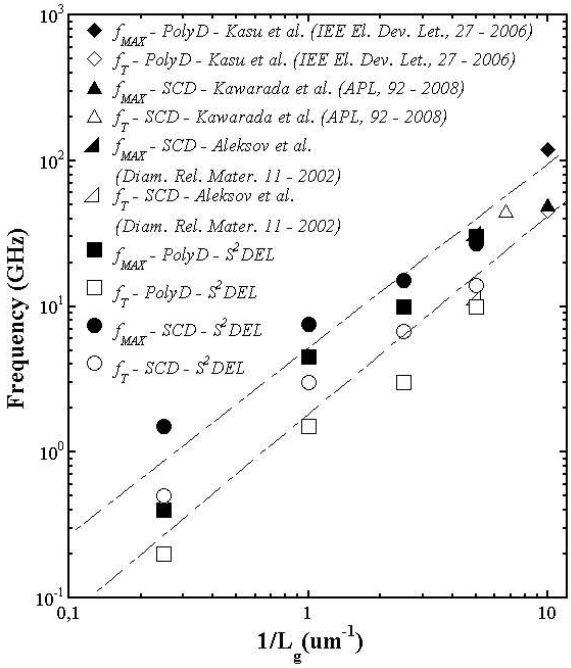


Figure 119 – f_{MAX} and f_T dependence on gate length inverse of literature data compared with results achieved from S^2DEL

Quality of substrate clearly influence the hydrogen termination: Russian Academy of Sciences samples shown higher quality in terms of FETs operation if compared with Element Six Ltd. Results achieved are absolutely comparable with literature ones in terms of cut-off frequencies, as shown in figure 119. Up to now, it seems that our limitation is the gate length, and, in other words, surface roughness: it is important to remark that other groups involved in diamond based FETs, grown their own diamond substrate and so they can work also on crystallographic orientation of substrate (that allow higher hole density and so carriers mobility) and operating a surface roughness lowering that allows higher technology resolution.

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List of publications

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Engineering, Vol. 54, 3, pp. 137-142 (Springer, ISBN: 978-90-481-3605) (2010)

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- ✓ M.C. Rossi, P. Calvani, S. Carta, G. Conte, "UV Photodetection in Surface Channel Diamond MESFETs" - MRS-NDNC (New Diamond and Nano Carbons) 2009

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- ✓ 5th NDIP (New Development in Photodetection), Aix-les-Bains, France (2008)
- ✓ SPIE Optics + Photonics, San Diego, California (2008)
- ✓ 19th Diamond European Conference, Sitges, Spain (2008)
- ✓ Nuclear Science Symposium, Medical Imaging Conference and 16th Room Temperature Semiconductor Detector Workshop, Dresden, Germany (2008)
- ✓ 15th MECSA National Symposium, Naples, Italy (2008) – oral presentation14th AISEM, Pavia, Italy (2009)
- ✓ 2009 NANOTEC, Rome, Italy (2009)
- ✓ 4th German Microwave Conference, Munich, Germany (2009) – *oral presentation*
- ✓ 10th Ultimate Integration on Silicon Conference, Aachen, Germany (2009)
- ✓ IEEE Nanotechnology Materials and Devices Conference, Traverse City, Michigan (2009) – *oral presentation*
- ✓ MRS NDNC (New Diamond and Nano Carbons), Traverse City, Michigan (2009) - *oral presentation*
- ✓ IEEE MTT-S International Microwave Symposium (IMS) RFIC, Boston, Massachusset, USA (2009) – *oral presentation*
- ✓ 4th European Microwave Integrated Circuits Conference (EuMIC), Rome, Italy (2009) – *oral presentation*
- ✓ MRS 2009 Fall Meeting, Boston, Massachusset (2009) – *2 oral presentations*
- ✓ International Semiconductor Device Research Symposium (ISDRS), University of Maryland, USA (2009)
- ✓ E-MRS 2010 Spring Meeting, Strasbourg, France (June 7-11, 2010) – *oral presentation*
- ✓ Prime 2010, Berlin, Germany (July 18-21, 2010) – *oral presentation*
- ✓ 5th European Microwave Integrated Circuits Conference (EuMIC), Paris, France (September 27-28, 2010) – *oral presentation*
- ✓ SPIE Microtechnologies, Prague, Czech Republic, (18-20 April 2011) – *oral presentation*

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