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3-Phase 5-Level E-Type Converter Topologies for Industrial Power Supply Applications

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LIST OF ACRONYMS AND SYMBOLS

BTB	Back to Back
SCR	Silicon Controlled Rectifier
TRIAC	Triode for alternating current
GTO	Gate Turn-off Thyristor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
BJT	Bipolar Junction Transistor
IGBT	Insulated Gate Bipolar Transistor
WBG	Wide-Band Gap
Si	Silicon
SiC	Silicon Carbide
GaN	Gallium Nitride
THD	Total Harmonic Distortion
UPS	Uninterruptible Power Supply
EMF	ElectroMotive Force
AC	Alternative Current
DC	Direct Current
NPC	Neutral Point Clamped
ANPC	Active Neutral Point Clamped
NNPC	Nested Neutral Point Clamped
FC	Flying Capacitor
CHB	Cascaded H-Bridge
MCC	Multi-Cell converter
PV	PhotoVoltaic
5LDCR	Five-Level Diode-Clamped Rectifier
5LDCI	Five-Level Diode-Clamped Inverter
MSSC	Multi-State Switching Cell
MC	Matrix Converter
P2 cell	Pyramid of the Basic Cell
PMSG	Permanent Magnet Synchronous Generator
EMI	ElectroMagnetic Interference
N	Number of Levels
f_{sw}	Switching Frequency
Δi_0	Current Ripple
PFC	Power Factor Correction
PWM	Pulse Width Modulation
N_S	Series Connected Capacitors
m_0	Modulation Index Offset
M_0	Modulation Depth
DCM	Discontinuous Conduction Mode
CCM	Continuous Conduction Mode

$SRBC$	Series Resonant Balancing Circuit
L_{ξ}	Total Commutation Inductance
L_{σ}	Connections Inductance
ESL	DC-bus Capacitors Inductance
L_{SW}	Die and Wire Bond Inductance
di_{sw}/dt	Device Current Slope
dv/dt	voltage derivatives
V_{BUS}	DC-bus Voltage
Δv_{BUS}	DC-bus voltage unbalance
V_{IN}	RMS Input Voltage
P	Phases: a, b, c
u_P	Input Phase-to-Neutral Voltages
$u_{P(sw)}$	Input-to-Neutral Switching Voltage
I_{IN}	RMS Input Current
i_P	Input Phase Current
S_{RPx}	Rectifier Switching Function
$\theta(i_P)$	Threshold Function
ZCS	Zero Current Switching
SSA	Steady-Space Averaging
L_P	Input Filter Inductors
$G_{vc}(s)$	Transfer Function of the DC-bus Voltage Controller
$G_{cc,d}(s)$	Transfer Function of the d-axis Current Loop
$G_{id}(s)$	System Transfer Function defined as i_d/d_d
$G_{vi}(s)$	System Transfer Function defined as V_{BUS}/i_d
$G_{lf}(s)$	Transfer Function of the Feedback Low-pass Filter
$G_{cc,q}(s)$	Transfer Function of the q-axis Current Loop
$G_{iq}(s)$	System Transfer Function defined as i_q/d_q
$G_{\Delta vc}(s)$	Transfer Function of the Voltage Controller
$G_{\Delta vd0}(s)$	System Transfer Function defined as $\Delta v_{BUS}/d_0$
u_{NM}	Middle Point Voltage
i_+	Currents through the Plus DC-bus Connections
i_-	Currents through the Minus DC-bus Connections
i_1	Currents through the Bottom-middle Leg
i_3	Currents through the Top-middle Leg
d_{RP}	Rectifier switches duty cycle
K	Park's transformation
TF	Transfer Function
S_{IN}	Input Apparent Power
PF_{IN}	Input Power Factor
f_{IN}	Input Frequency
ω_{IN}	Input Angular Frequency
THD_i	Input Current THD
S_{OUT}	Output Apparent Power
PF_{OUT}	Output Power Factor

f_{OUT}	Output Frequency
THD_v	Output Voltage THD
V_{OUT}	RMS Output Voltage
I_{OUT}	Output Current
φ_{OUT}	Output Phase Displacement
ω_{OUT}	Output Angular Frequency
$M_{0,R}$	Rectifier Modulation Depth
$M_{0,I}$	Inverter Modulation Depth
Q	Phases: u, v, w
u_Q	Output Phase-to-Neutral Voltages
$u_{Q(sw)}$	Output-to-Neutral Switching Voltage
I_{OUT}	RMS Output Current
i_Q	Output Phase Current
S_{IQy}	Inverter Switching Function
$V_{BL(max)}$	Maximum Blocking Voltage
Δv	Commutation Over-Voltage
PSM	Passive Switch Mode
ASM	Active Switch Mode
V_{FR}	Forward Recovery Voltage
$A_{n,car}$	Amplitude of the Carriers
$m_{n,car}$	Offset of the Carriers
c_{t1}, c_{t2}, c_{t3}, c_{t4}	Carrier Signals
$m_{P,R}(t)$	Rectifier Modulating Signal
$m_{Q,I}(t)$	Inverter Modulating Signal
ψ	Input to Output Voltage Displacement
d_{IQ}	Inverter Switches Duty Cycle
AVG	Average
RMS	Root Mean Square
T_{sw}	Switching Period
T_0	Fundamental Period
$i_{RMS,i}$	RMS Rectifier Devices Current
$i_{AVG,i}$	AVG Rectifier Devices Current
$i_{RMS,j}$	RMS Inverter Devices Current
$i_{AVG,j}$	AVG Inverter Devices Current
v_{sw}	Voltage Across the Switch
i_{sw}	Current Flow the Switch
P_{switch}	Total Losses Switch
$V_{sw(0)}$	Forward Voltage Drop
r_{sw}	Power Semiconductor Ohmic Resistance
P_c	Conduction Losses
T_j	Junction Temperatures
E_{AVG}	Average Switching Energy
P_{sw}	Switching Losses
E_{on}	Turn-on Energy

E_{off}	Turn-off Energy
$E_{rr,AVG}$	Average Reverse Recovery Energy
P_{off}	Blocking Losses
$I_{sw(\zeta)}$	Switch Leakage Current
N_C	Number of the Interleaved Cells
ICT	Inter-Cell Transformer
L_{IN}	Input Inductance
C_{IN}	Input Capacitance
L_{OUT}	Output Inductance
C_{OUT}	Output Capacitance
i_{LP}	Input Inductor Current
Δi_{LP}	Input High Frequency Current Ripple
$\Delta i_{LP,max}$	Input Maximum Peak-to-Peak Current Ripple
Z_{Grid}	Grid Equivalent Impedance
i_{LQ}	Output Inductor Current
Δi_{LQ}	Output High Frequency Current Ripple
$\Delta i_{LQ,max}$	Output Maximum Peak-to-Peak Current Ripple
$\Delta u_{Q,pp}$	Output Voltage Peak-to-Peak Ripple
AP	Area-Product Factor
A_E	Core Effective Cross-Section Area
A_W	Core Winding Window Area
B_{peak}	Peak Flux Density
n	Number of Turns
J	Current Density
k_{FL}	Winding Coefficient
A_{cu}	Cross-Section Winding Wire
$P_{ICT,C}$	ICT Core Losses
P_{ICT}	ICT Total Losses
m_C	Core Mass
$R_{0(DC)}$	Winding Resistance at Low Frequency
P	Resistivity
L_W	Winding Wire Length
P_{CU}	Windings Losses
R_{CC}	Thermal Resistance Core to Ambient
R_{W1W1}	Thermal Resistance First Winding to Ambient
R_{W2W2}	Thermal Resistance Second Winding to Ambient
R_{W2W1}	Mutual Thermal Impedances
i_{BUS}	DC-bus Instantaneous Current
$i_{BUS,LF}$	Low Frequency DC-bus current
$i_{BUS,LF}$	High Frequency DC-bus current
$i_{CBUS,LF}$	DC-bus Capacitor Current
ΔV_{BUS}	Peak to Peak Voltage Ripple
R_{ESR}	Capacitor ESR
$I_{C1,BUS(RMS)}$	Requirement Current per Single Capacitor

P_{BUS}	DC-bus capacitor losses
T_c	Case Temperature
T_a	Ambient Temperature
$R_{th,c\text{-}a}$	Case to Ambient Thermal Resistance
λ_T	Life Time
$R_{th(c\text{-}s)}$	Thermal Resistance Case to Heat Sink
$R_{th(j\text{-}c)}$	Thermal Resistance Junction to Case
f_{swE}	Equivalent Switching Frequency
h_{PS}	Efficiency Power Supply
GD	Gate Driver
Q_G	Gate Charge
P_{IC}	GD IC consumption
$\rho_{density}$	Power Density
Vol	Total Volume
G	Total Weight
$\rho_{specific}$	Specific Power Density
MRC	Multi-Resonant Controller
PLL	Phase-Locked Loop
OSG	Orthogonal Signal Generator
$G_{RC(n)}(s)$	Multi-Resonant Controller Transfer Function
$\hat{\theta}_{grid}$	Estimated Grid Angle
$G_{Rep}(z)$	Repetitive Controller Transfer Function
$G_{PI}(s)$	PI controller Transfer Function
GUI	Graphical User Interface
$FPGA$	Field Programmable Gate Array
RT	Real-Time
DT	Dead-Time

THE DISSERTATION OBJECTIVES

The target of this dissertation is to investigate, to analyze and implement an innovative multi-level converter configuration topology solution to obtain high efficiency and high power density to be used in industrial power supply applications. To this purpose, a wide analysis of the existing multi-level converter topologies has been carried out. Accordingly, it has been found out that the multi-level T-Type topology can be considered as an important topology to be used for high speed generation (i.e. generation units composed by gas turbines, aerospace, etc.) and UPS applications. After that, the investigation focused on the three-phase unidirectional AC/DC multi-level rectifier (3Φ5L E-Type Rectifier). The theoretical study and preliminary simulation has been addressed with reference to 3Φ5L E-Type Rectifier. Afterwards, the laboratory prototype 3Φ5L E-Type Rectifier has been built in order to validate theoretical analysis. As a result of the amazing performances of the rectifier in terms of weight, volume and efficiency, the final delivery project on the AC/AC double conversion system has been realized with reference to industrial applications like Uninterruptible Power Supply (UPS). The AC/AC converter is composed of two multi-level topologies: the AC/DC multi-level rectifier (5L E-Type Rectifier) and DC/AC multi-level inverter (5L E-Type Inverter). This connection is called Back to Back E-Type (BTB) multi-level converter. The multi-level rectifier topology can be easily extended, from the hardware point of view, to the double conversion configuration, which is typical of UPS applications. The main difference between drive system and UPS multi-level double conversion is the operating point. On one hand, a drive system usually works with a frequency which depends on the rotational speed of the electric drive. On the other hand, a double conversion UPS works at almost constant voltage and fixed frequency. In both the considered applications, all the power semiconductors need to be selected to optimize the overall performance of the multi-level converter topology. Finally,

a 20 kVA Back to Back E-Type multi-level Converter has been analyzed in order to ensure the following targets:

- AC/AC peak efficiency equal to 98.25% including filter, driver, control and fan, with a resistive load;
- a power density greater than 3.5 kW/L including filter;
- input current total harmonic distortion (THD_i) less than 3%;
- output voltage total harmonic distortion (THD_v) less than 1%;
- a short circuit capability equal to 3 times nominal current for 60 ms.

THE DISSERTATION ORGANIZATION

The dissertation is organized in five parts: 1) State of the art of Multi-level Converters, 2) 5 Level E-Type Unidirectional Rectifier, 3) 5 Level E-Type Back-To-Back Converter, 4) Proof of concept design proposal topology, 5) Modeling Aspects and Control Scheme.

1. **State of the art of Multi-Level Converters**

   The first part of the dissertation shows the needs and the motivation for the multi-level conversion. The main three-phases Back-To-Back Converter configurations based on multi-level topologies are discussed, moreover the voltage balancing and total commutation inductance issues are presented. Special attention has been given to patents and established technology already found in industry. Patent review is important as it offers the possibility to analyze, in this way, existing solutions in industrial environment, to identify what has been already protected. Consequently, from the existing systems description, further investigations will be carried out to develop and protect new solutions.

2. **5 Level E-Type Unidirectional Rectifier**

   In the second part of this dissertation, the 5 level E-Type Unidirectional Rectifier is introduced for electrical drives applications. The theoretical investigation, simulation results and losses analysis are achieved with reference to the suitable power semiconductors. A laboratory prototype was built with a rated power equal to 17 kW. The control strategy has been implemented using the National Instruments LabVIEW environment. The tuning of the control strategy is based on the rectifier Bode transfer function which has been obtained starting from the rectifier mathematical model. The experimental tests have been performed in order to confirm the achieved theoretical analysis.

3. **5 Level E-Type Back-To-Back Converter**

   The basic power converter topology and its improvement, called New 5L E-Type Back-To-Back Converter (N5L BTB Converter) is investigated in the third part of this dissertation. Two different multilevel topologies in Back-To-Back configuration are identified: N5L E Type Inverter and N5L E-Type Rectifier. A brief introduction to the characteristics of the 5L BTB Converter is presented. The general analysis, the switches realization, switches voltage ratings, modulation scheme and analytical approach to calculate the current stress in the 5L BTB Converter are discussed.

4. **Concept design of the proposed topology**

   The analytical approach to calculate the conduction and switching losses in the 3ΦN5L E-Type BTB Converter is presented in the fourth part of the dissertation. The power losses are used to investigate converter performance and efficiency as a function both of the converter output power and of the switching frequency. The final part deals with the analytical method to select the capacitors and the inductors of the input and output filter and with the analytical technique for selecting DC-bus capacitor of the 3ΦN5L E-Type BTB Converter. The active and passive components stresses have been obtained and verified through preliminary simulation performed in the Matlab/Simulink and Plexim/Plecs environment.

5. **Modeling Aspects and Control Scheme**

   In the fifth part, the control strategy both of the rectifier and of the inverter is presented and discussed. The control algorithm has been implemented in LabVIEW and the resulting program is made up of two different targets: FPGA and Real-time, which are run on dedicated hardware. The circuit of the 3ΦN5L E-Type BTB Converter has been built in NI Multisim environment. Afterwards, the control loop algorithm has been tested using the co-simulation capabilities between Multisim and LabVIEW

environments in order to evaluate its performances.

PART ONE

- STATE OF THE ART -

1 INTRODUCTION

1.1 Power Electronics Yesterday, Today and Tomorrow

Power electronics began with the invention of the mercury-arc rectifier of Peter Cooper Hewitt in 1902 [1]. Afterwards, the ignitron and the thyratron or hot-cathode glass bulb gas tube rectifier were introduced in 1930s. The diode version of the thyratron was known as the phanotron. The ignitron, thyratron and phanotron devices were used until the 1950s. The invention of transistors in 1948 by Bardeen, Brattain, and Shockley of Bell Telephone Laboratories transformed the power electronics world. Thus, the second electronics revolution started with the invention of the p-n-p-n Silicon (Si) transistor in 1956 by Moll, Tanenbaum, Goldey, and Holonyak at Bell Laboratories, and General Electric Company introduced the thyristor (Silicon-Controlled Rectifier - SCR) to the commercial market in 1958. The modern thyristor or SCR derives its name from the thyratron. Progressively other power devices emerged:

- integrated antiparallel thyristor (TRIAC) was invented by General Electric in 1958 for AC power control,
- gate turn-off thyristor (GTO) was invented by General Electric Company in 1958,
- high-power GTOs were introduced by several Japanese companies in the 1980s.

The thyristors were used exclusively for power control in industrial applications until 1970. Then, different power semiconductor devices such as power MOSFETs (VMOS field effect transistors or FETs and viable silicon MOSFET, HEXFET) and bipolar junction transistors (BJTs, used as bipolar power transistors, BPTs) appeared on the market in the late 1970s, Fig. 1. In those days, it was not possible to run high power at high voltage and high switching frequency. The reason was the poor switching characteristic of the BPT and SCR

devices and high on-state resistance at high voltage related to the power MOSFETs (they were used for low-voltage high-frequency applications). The power electronics was born a second time when Jayant Baliga invented insulated-gate bipolar transistor (IGBT) at the end of 1970 and begin of 1980s. The IGBT solved all problems of BJT and MOSFET. To solve the high on-state resistance of high-voltage MOSFET, Super Junction-CoolMOS devices were developed by Infineon in 1990s. Considering the same package, CoolMOS device has lower on-state resistance than other MOSFET.

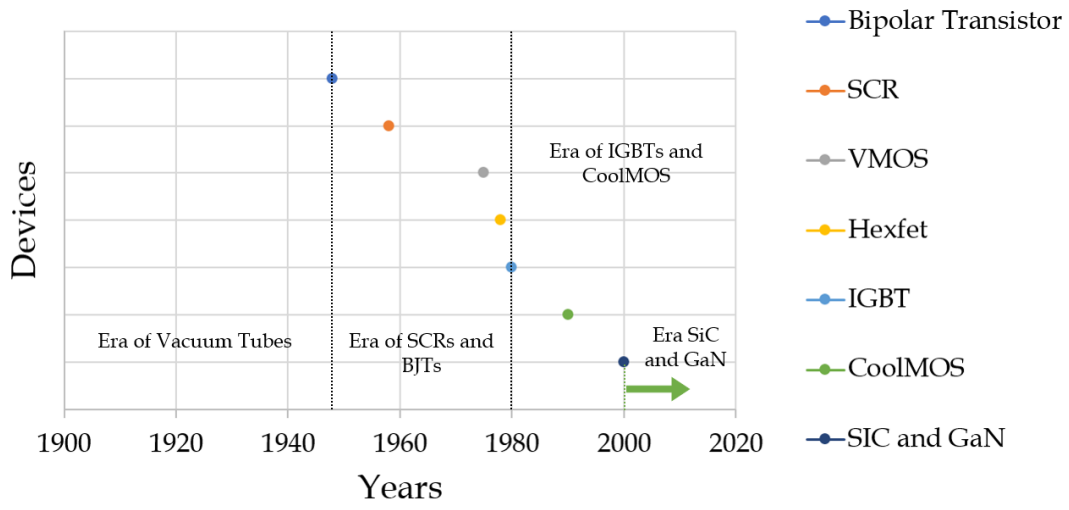


Fig. 1. Power device technology reaches maturation.

Today, the IGBT is the most important device for medium and high power applications and MOSFET is used for low and medium voltage applications. Over the years, silicon has been the basic raw material for power devices. Today, there are many challenges in researching large-bandgap power devices. Wide-band gap (WBG) materials, such as SiC, GaN, and ultimately diamond (in synthetic thin-film form), are showing great promise.

What is the situation like in power electronics today? Power electronics is part of every segment of our life, Fig. 2. Any piece of electric equipment we see today is somehow based on power electronics and static converters: in-home appliances, industrial equipment, renewable energy, automotive, avionic, etc., etc. Power electronics allows to improve the performance, power density, reliability, energy efficiency, and cost effectiveness of electrical power systems. New power devices

and new power systems development contributed to these improvements.

What is going to happen in the near future? The power electronics target is to reduce as much as possible the costs, size, weight and losses of the conversion systems. To reach this purpose it will be necessary to use new material processing and fabrication techniques, packaging, device characterization, modeling, and simulation techniques. They will help the evolution of advanced power devices, higher voltage and current ratings, and the improvement of performance characteristics.

Fig. 2. Power electronics today.

As the Si-technology is reaching the theoretical limits, new WBG devices are becoming the new choice for power electronics applications.

What kind of semiconductors technology can be used? Si, SiC or GaN? Of course, it depends on the applications! Naturally, power semiconductor, whatever it is, without "support system" is nothing. Thus, next to semiconductor technology we must also consider packaging and gate driver circuit.

WBG devices are very promising, as they allow power electronic components to be smaller, faster, more reliable, and more efficient than their silicon-based counterparts. On the other hand, alternative packaging materials or designs are also needed to withstand the high temperatures and to minimize stray inductance and capacitance. Furthermore, WBG devices require an active gate

driver to limit the overvoltage. Thus, among the optimism surrounding WBG semiconductors there are still open challenges. First of all, there is the cost reduction and the need to optimize packaging to allow the full realization of the potential of WBG materials. Keeping in mind that silicon has taken more than half a century to get to where it is today, it is reasonable to predict that it will take some time for WBG and other emerging technologies to gain full maturity to replace silicon. Given the high potentiality, we can expect to see more WBG semiconductors in our future. In parallel with the power semiconductor evolution, new converter topologies and new control platform technology will play an important role in continuous efficiency improvement, power density and cost reduction.

1.2 Research Motivation

A power converter is a system consisting of four main elements: 1) a set of power semiconductor switches, 2) a network of passive devices (inductors, transformers and capacitors), 3) digital control circuitry and 4) control algorithm, Fig. 3.

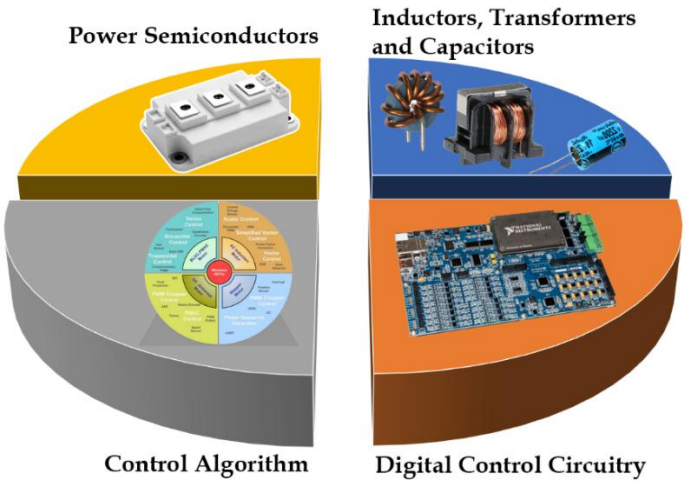
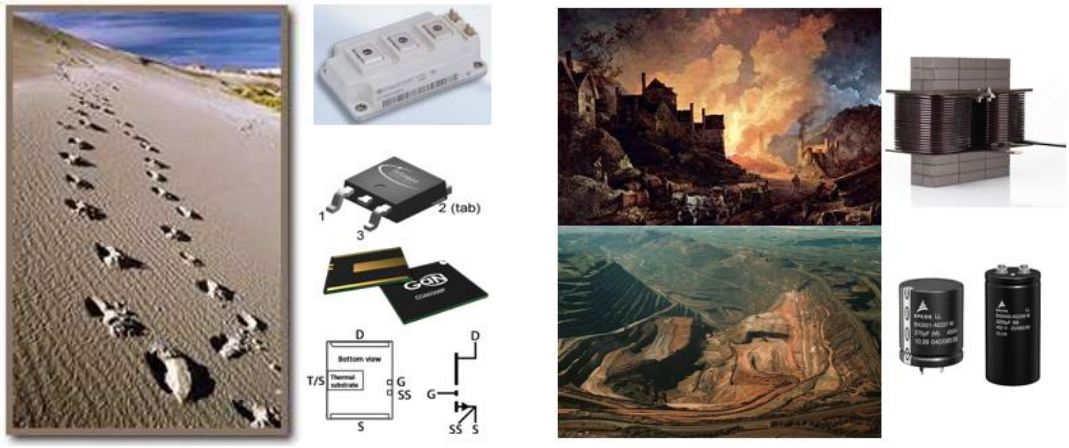


Fig. 3. Power converter System.

From a material point of view, the power semiconductors are nothing else than a piece of "roosted sand". Raw material is basically sand and it is 27% of the planet, Fig. 4a; this means that we have a lot of material although inductor,

transformers and capacitors are very dirty technology due to the use of iron, copper and aluminum which are considered raw material, Fig. 4b. Having all this in mind, it is obvious that the only solution for future development is to use more and more semiconductors (Si, SiC, GaN) and less iron and copper. In fact, applications linked to the power semiconductors have had a cost reduction in the recent years. Furthermore, iron and copper, which are the basic materials for the manufacture of inductors and transformers, are not cheap at all. Thus, from a cost point of view, if the number of semiconductor devices increases in a power converter, it does not mean that the cost of the overall system becomes higher.



(a) (b)

Fig. 4. Motivation and must of the future Power Electronics. (a) Use more "Nice" Power Semiconductors, (b) and Less "Not-Nice" iron and copper.

Efficient energy conversion and power density for low and medium voltage applications have gained more and more attention in recent years. Applications such as photovoltaic and wind inverters [1], [3], [4], PFC rectifiers, electric and hybrid vehicles, power quality and active filters [5], aerospace and large ship propulsion [4],[6], [7], [8], [9], [10], [11], [12], [13], [14], Uninterruptible Power Supply (UPS) [15] and automotive inverter systems demand for high efficiency at low costs. Furthermore, the integration and acoustic noise problem are some of the main concerns in applications due to the established international Standards. For these reasons, the switching frequency is often increased (higher than 20 kHz). This leads to small and cheap passive components on one side, and high switching losses and low system efficiency on the other side. Additionally,

the trend in high-speed drives and in aircraft applications is to increase the fundamental output frequencies up to 1 kHz and even more to improve the power density. As a consequence, the switching frequency is increased in order to obtain acceptable voltage waveforms. Once again, the performance of the power conversion systems is limited by the power semiconductors, whose limitations are imposed by the physical characteristics of the semiconductor materials. Thus, the interests of the researchers are moving towards the development of new power semiconductors with lower switching losses and higher voltage withstand capabilities. Is it enough to improve the power devices? Obviously, the answer is no! We need to find new solutions which can accommodate power semiconductors with limited voltage and current rating. Is there any new topology? It is unlikely: all new topologies were introduced years and years ago. What is necessary to do is to consider all the existing topology converters and use them in a different way.

One way to achieve higher efficiency and lower cost/size/weight is to deploy multi-level and/or multi-cell power converter topologies [1], [3], [4], [7], [8], [10], [11], [12], [13], [14], [16], [17], [18], [19], [20]. Almost four decades have passed since the first introduction of multilevel inverters. Their important role in industry and academia is well known. Multilevel converters have been introduced to extend the power range and to ensure the use of low voltage rating power semiconductors. Having low voltage across the device when switching, multilevel topologies allow to reduce the switching times. Consequently, the multilevel converters enable to improve the switching losses when they are compared to the classical two-level topology at the same switching frequency. Furthermore, multilevel converters also have interesting additional features when they are compared to the classical two-level topologies, such as the reduction of the harmonic content of the synthesized voltage waveform.

As the working number of voltage levels of the converters increases, multilevel converters greatly increase the number of power devices and the number of

capacitors in the DC-bus. As a result, gate driver circuits required to drive each switch increase in number and the DC-bus voltage across the capacitors in series connection is unbalanced. Additionally, when using discrete components to build the power board, as the number of semiconductors increases, the layout of the board must be carefully designed in order to avoid the increasing of stray inductances and possible malfunctions. This may cause the overall system to be more expensive and complex. One point that should not be underestimated is the control algorithm which is used to regulate the multilevel converters in order to achieve the multiple constraints of number of switches of redundant states, power density, unbalanced losses, reliability, etc. All this represents a wide field of research in the study of existing multilevel topologies and new circuit topologies and their control algorithms in a wide range of applications.

1.3 Background

Multilevel inverters are widely used as static power converters for alternating current applications which include variable speed industrial electric drives, UPS and interfacing of renewable energy sources, photovoltaic and fuel cell, with the utility grids. Additionally, these applications require either unidirectional or bidirectional power flow capability [21]. Depending on the number of independent DC sources used in their structure, the multilevel inverters can be classified in two main groups, as shown in Fig. 5. The most known topologies are the Neutral Point Clamped (NPC) or diode clamped, the Flying Capacitor (FC) or capacitor clamped, and the cascaded H-bridge (CHB) [22]. Due to their modular and simple structure composed of several smaller power converters called power cells, the multilevel converters, as FC and CHB inverters, can be stacked up to an almost unlimited number of levels. These multilevel inverters are also referred to as multi-cell converters (MCCs) [23], [24], [25]. In order to satisfy particular application requirements and to improve the operational features, nowadays numerous variations and combinations of these

topologies have been presented in literature [25], [26], [27], [28], [29]. The utilization of these multilevel converters leads to designs with higher power ratings, improves the power quality and the dynamic stability for utility systems, assures high efficiency (even higher than 98%). In PVs systems, multilevel inverters can become relevant, since PV strings can be used as DC sources for multilevel topologies. As there is no need for a rectifier stage, the multilevel power circuit is greatly reduced.

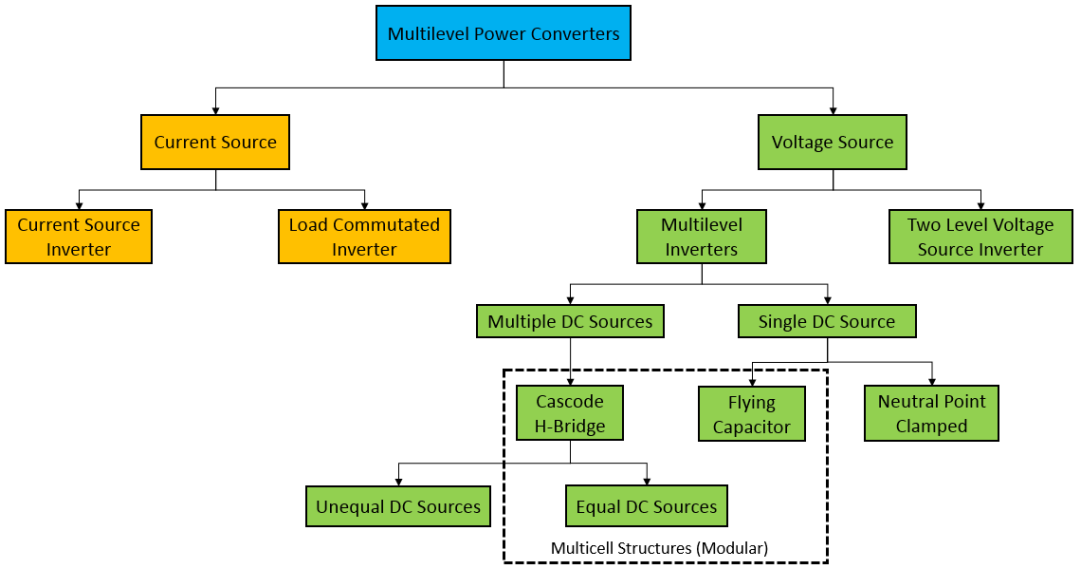


Fig. 5. Multilevel inverter classification.

The multilevel converter can provide control for both maximum power tracking and output power factor reducing the filter weight and volume. Furthermore, it can improve efficiency (lower switching frequencies can be applied) and eliminate the need for step-up transformers, or it can boost circuits if enough PV sources are connected in series. CHB converters used for PV power conversion have been reported in [30], [31]. Multilevel converters can also be used as a DC-AC power conversion in the UPS units. The connection between a multilevel rectifier and a multilevel inverter for AC-DC/DC-AC conversion is known as Back-To-Back Configuration (BTB), Fig. 6.

Some multilevel inverters topologies, such as NPC inverter or FC inverter, require low or medium voltage DC source, whereas in other multilevel inverters topologies, as CHB inverters, several isolated DC sources are needed.

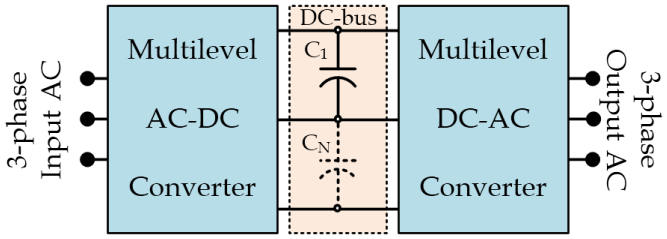


Fig. 6. Multilevel Back-To-Back Configuration.

In order to provide these DC voltages, different rectifier topologies can be used which can be classified on the basis of the number of phases and the power flow capability [32], Fig. 7. As it can be seen in Fig. 7, there are two categories: the first one consists of single-phase and three-phase non-regenerative power rectifiers; the second one consists of single-phase and three-phase regenerative power rectifiers. The standard diode rectifiers at the input side have serious problems of low input power factor, high THD (Total Harmonic Distortion) in input currents and harmonic pollution on the grid. According to these problems, several topologies of converters have been proposed in literature [33], [34].

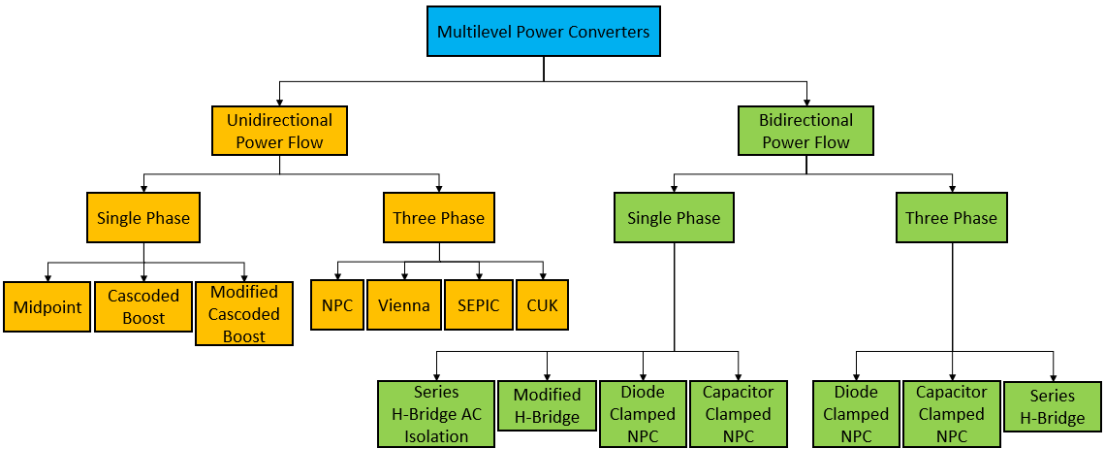


Fig. 7. Rectifier classification of improved power quality converters.

A classification of unidirectional three-phase rectifier circuits has been achieved considering three different groups: passive systems, hybrid and active systems, as shown in [33], [34]. Three-phase PFC rectifier topologies are even more used in various applications as input power stage, such as variable speed drives, UPS, data centers and telecom power supplies, DC motor drives, battery charging, etc. [35]. In the last few decades, new interface topologies have evolved

from unidirectional two-level to three-level rectifiers [35], [36]. In [37], the three-level neutral point clamped rectifier has been compared with two-level conventional rectifier. The study shows that multilevel rectifier for proposed control scheme is far superior to its counterpart two-level rectifier. On one hand, it provides better performance in terms of unity input power factor, negligible input current THD, reduced rippled regulated DC load voltage at a lower switching frequency and reduced voltage stress of the power semiconducting devices. On the other hand, the large number of power switches significantly increases cost and control complexity [38]. Anyway, applications such as variable speed drives, UPS and telecom power supplies, where both power density and specific weight are of the greatest importance, have become potential users of unidirectional three-level rectifiers. Among active PFC systems, the Vienna rectifier [33] is often used as multilevel rectifier stage for its reduced power losses, low number of active devices, sinusoidal input currents with Power Factor close to one and THD less than 5%, high efficiency and low switch/diode voltage stresses, which make it suitable from medium to high power applications. In order to improve the number of voltage levels and, at the same time, retaining the advantages offered by the Vienna rectifier, a new type of three-phase converter called Five-Level Unidirectional T-Rectifier has been proposed in [39], [40]. With the reference to unidirectional applications, the benefits of having a multilevel rectifier over conventional rectifier make the multilevel rectifier a favorite choice as a DC source for multilevel inverters.

2 MULTI-LEVEL THREE-PHASE BACK TO BACK CONVERTERS

2.1 Multi-Level Converter in Low Voltage High Current Applications

Multi-level Converters have been initially introduced for DC to AC conversion applications. In recent years, even in AC to DC conversion system the multi-level converter received increase interest of both academia and industry. Nowadays, many industrial applications have begun to require high power. Some appliances in the industries, however, require medium or low power for their operations. In fact, the use of a high-power source can be useful to some industrial loads but it can damage other ones. The increased demand for electrical power is experienced in both the automotive sector as well in the distributed generation and it occurred also in aerospace applications. As the electric power is increased also the size of the electrical systems is increased. In limited spaces, i.e. in automotive and aerospace applications, the size increasing of the electrical system is considered a main disadvantage. This has motivated research into finding new technologies that allow the use of power generation systems with high efficiency and reduced volumes. With reference to generating units being fed through high speed prime movers, a typical power conversion system for low voltage and high-power applications is shown in Fig. 8. In general, the gen-set system presents a high-speed turbine, a three-phase permanent magnet synchronous generator (PMSG) and a rectifier. The main idea of using high-speed generators is to couple directly an energy conversion unit to a given fast rotating mechanical system, (e.g. gas turbines, aircraft turbine turbo-expander) without the use of gear boxes. The high-speed generators are used in order to reduce the system volume and maintenance costs and to increase efficiency. Permanent magnet machines have the most advantages, including higher efficiency and smaller size when compared with other types of motors

and/or generators of the same power rating [9], [10], [41]. The conversion of direct drive from turbines to permanent magnet systems has led to the increase of the machines speed. As a result, the higher the machines speed is the higher the output fundamental frequency (up to 1-2 kHz) of the motors will be.

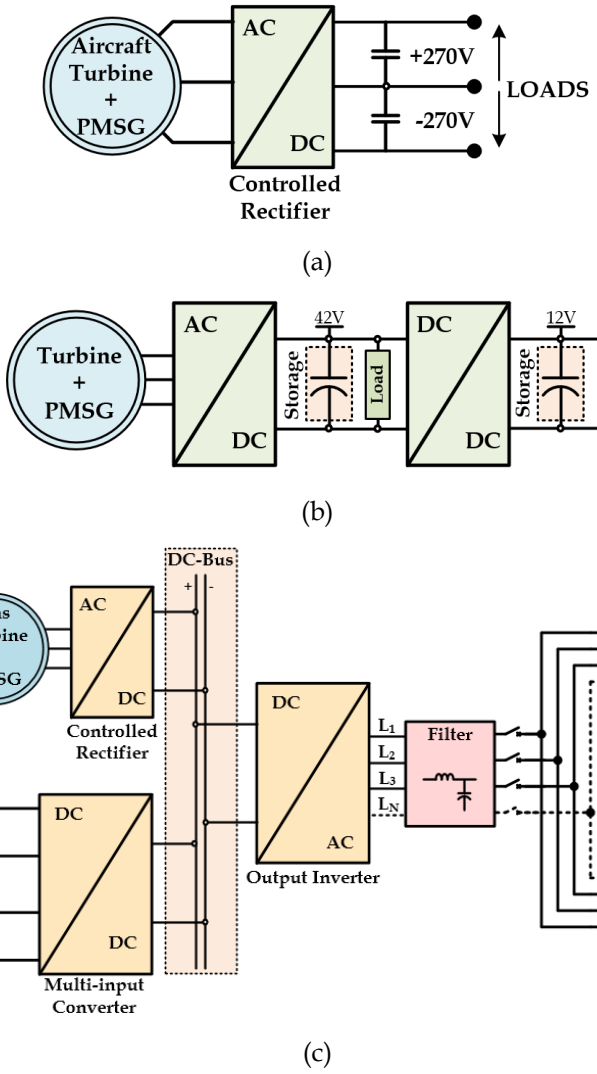


Fig. 8. Block scheme of high speed gen-set applications; a) aircraft, b) automotive, c) Micro-grid.

Because of the resulting high fundamental frequency of the machine, the synchronous inductance is reduced in value to limit the reactive voltage drop. On the other hand, having low inductance value, the phase current at the input of the rectifier presents high level of the current ripple. A method to reduce the current ripple to an acceptable value is to increase the switching frequency. Does it make sense to increase the switching frequency? As explained more in detail

in the following section, multilevel converters are considered an attractive option due to their ability to reduce the ripple current without increasing the switching frequency.

2.1 Multi-Level Converter in the UPS Applications

Multilevel converters are currently considered as one of the most promising industrial solutions for high dynamic performance and power-quality demanding applications, covering a power range from 1 kW to 30 MW [18], [44], [45], [46], [47], [48]. Among the reasons, their success can be highlighted as the higher voltage operating capability, lower common-mode voltages, reduced voltage derivatives (*dv/dt*), voltages with reduced harmonic contents, near sinusoidal currents, smaller input and output filters, increased efficiency, and, in some cases, possible fault-tolerant operation [49], [50], [51]. Recently, they have been proposed to enable new possibilities for several important applications like UPS, wind energy conversion, electric and hybrid vehicles, aerospace, photovoltaic energy conversion, reactive power compensation, and regenerative applications [3], [52], [53], [54], [55], [56], [57].

The UPS system plays an important role in the modern power electronic conversion, because of its simplicity in transferring electric power from the input to the output. In order to limit the harmonic influence on the grid or load, standards, guidelines and regulations are often required [58]. To this purpose, the UPS systems should have the ability to control the input and output power. In applications where the power quality of the power grid can be a problem, standard architecture for double conversion UPS systems are typically used, Fig. 9. The load, in the double conversion UPS systems, is completely isolated from the power grid and the whole electricity flows through the UPS. During normal operation, the input voltage is rectified into DC; this power is converted back to AC through an inverter and used to power the critical loads. The advantages of this system are: the load is protected from all types of power disturbances present

in the power grid, the voltage and frequency of the AC output can be adjusted in the UPS and in case of power grid failure the battery will supply the loads.

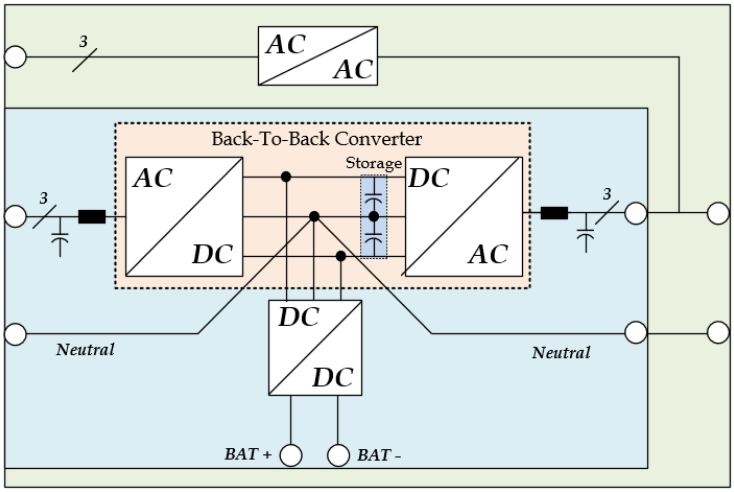


Fig. 9. Block scheme for double conversion UPS.

Additionally, the double conversion UPS has an internal bypass, ensuring that if your UPS experiences a catastrophic failure or requires maintenance, you may be able to keep your critical loads online. The multi-functionality provided by this system is the reason why this type of UPS is the most common for data centers and digital offices. With the availability of the multilevel converter topologies, the UPS systems can be further explored with the potential of increasing the number of levels. Furthermore, the recent interest in renewable energy generation, especially in grid-connected photovoltaic systems, is imposing challenges in the realization of new topologies of multilevel converters.

2.2 Motivation for Multi-Level Power Electronic Conversion

The target of multi-level converter topologies is to have the losses reduction and, consequently, improving the efficiency without sacrificing both the system's power quality and costs. In fact, the increasing of the number of voltage levels produces better voltage waveform and reduced THD. Furthermore, reducing *dv/dt* stress leads to the reduction of Electromagnetic Interference (EMI). In the multi-level converter, the switches are stressed by a fraction of the total DC-bus voltage. This allows us to use lower voltage rated switches that have better

switching and conduction performance if compared to the switches rated on the full blocking voltage. Additionally, using multi-level converter means having short switching times of the devices. Keeping constant the device's losses, a classic two-level converter is required to use two times the switching frequency of a three-level converter in order to achieve the same ripple in the output current. Thus, the input/output filter components in a multi-level converter will be smaller in both value and size than the filter components in a two-level converter. In other words, it can be shown that the peak-to-peak current ripple of an N-level converter that has to be filtered by an input and/or output filter strongly depends on the total inductance L_T, switching frequency f_{sw} and number of the levels N. A generalized current ripple equation is given by (1), where V_{BUS} is the total DC-bus voltage and m is the modulation index.

$$\Delta i_0 = \frac{V_{BUS}}{L_T (N-1) f_{sw}} \left\{ (N-1)m - floor\left((N-1)m\right) - \left[(N-1)m - floor\left((N-1)m\right) \right]^2 \right\} \quad (1)$$

In order to reduce the current ripple, we can play with the switching frequency f_{sw} and the number of levels N. The frequency is not an option since higher is the switching frequency then higher will be the conversion losses.

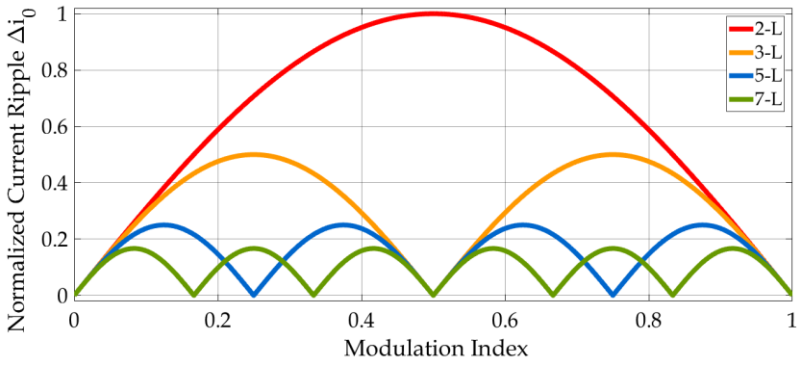


Fig. 10. Normalized current ripple versus modulation index m and number of levels N.

The inductance value L_T is neither an option; higher is the inductance then bigger, heavier and more expensive will be the system. Thus, the only option is to increase the number of levels N. The normalized current ripple versus the number N of levels and the modulation index m is shown in Fig. 10. It can be notated the advantages of an N-Level converter compared to an ordinary 2-Level converter.

In view of the above, it can be concluded that the only way to increase the efficiency as well to reduce size/weigh/cost is to increase the number *N* of levels. However, as intensively discussed in [12], number *N* of levels cannot be arbitrary selected. Higher is better is not always the case. The system parameters such as the DC-bus voltage, current rating, the device switching speed, the commutation inductance, etc., etc., have to be analyzed to select an optimal number *N* of levels. In some applications, another important aim is to optimize the power density. To do this, besides reduction of the size passive filter the key player is the size of the heat-sink. Obviously, the heat-sink's size is a function on the power semiconductor's losses; the power losses saving depends on the different degrees of freedom such as topology, operating point of converters and choice of devices. As will be described later, the T-Type and/or I-Type topology multi-level converter exhibits a different behavior depending on the modulation index; changing the modulation index changes the converter's operating point. When the modulation index is low in the multi-level converters can be present few voltage levels and the conversion losses can be much higher than a classic two-level converter, considering the same power semiconductor's technology. On the contrary, having high modulation index allows a better performance of the multi-level converters compared to a classic two-level converter. Additionally, for high modulation index the current path in some multi-level topologies can involve more devices than in other multi-level topologies; thus, different multi-level converters topologies present different power conversion losses. Multi-level converters always work with high modulation index in some applications (i.e. UPS), therefore, power device's technology being equal, the goal is to choose the most suitable multilevel topology that enables to reduce the conversion losses and, consequently, reduce the size of the heat sink.

2.3 Multi-Level Converter Topologies: *Review*

Back to Back power electronic conversion can be realized by using multi-stage AC–DC/DC–AC converter, Fig. 11. Considering a three-phase input voltage source provided by PMSG at high fundamental frequency or supplied by the grid at fixed frequency and voltage, the features of the AC-DC converter are to provide sinusoidal input currents and a regulated DC voltage. Afterwards, DC-AC converter has the task of feeding a critical load or a grid with a voltage and current sinusoidal starting from a DC voltage. Moreover, in order to supply a constant DC output voltage even at low mechanical speeds or at low voltage values at the input from mains, boost functionality is often required.

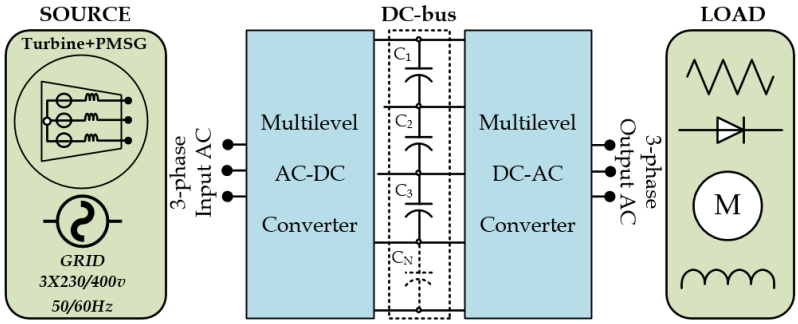


Fig. 11. Back-To-Back connected multilevel converters for variable-speed drive and UPS applications.

The AC-DC three-phase converters are gaining more and more attention to provide high efficiency, small size, reliability and low component counts with a high input power factor, low line current distortion and the ability to provide a regulated output voltage, regardless of the input voltage and the load [21], [42]. Several types of active and hybrid rectifiers' topologies, from the simplest to the most complex, can perform the described tasks. In the simplest case, the rectifier could be an ordinary 2-Level Voltage Source (VS) rectifier [12] with capacitive dc bus filter. The low complexity due to no control, sensors, auxiliary supplies or EMI filtering and high robustness of this concept must, however, be weighed against the disadvantages of relatively high effects on the mains and the unregulated output voltage directly dependent on the mains voltage level [33].

Many topology of converters, from the simplest to the most complex (e.g. active PFC systems, hybrid systems, etc.) have been introduced in literature trying to improve the bad features previously mentioned [33], [34], [43]. Later, two levels and three-levels rectification have been widely used as the front-end converter due to its attractive benefits of provide a high input power factor, a regulated output voltage, regardless of the input voltage and the load, low line current distortion, high efficiency, small size and low system costs over a passive system. In order to reduce the switching losses caused by switching od power semiconductors at both the input and the output stages of multilevel configurations, to assure low distortions in the output voltages and to achieve sinusoidal input currents, many BTB topologies have been investigated. An overview of the voltage and current DC-link converter topologies used to implement a three-phase PWM AC–AC converter system is presented in [59]. As described in more details in [60], [61], the methodology and the results of a comprehensive comparison of a direct matrix converter (MC), an indirect MC, and a voltage DC-link BTB converter for a 15-kW permanent magnet synchronous motor drive have been investigated. Most of the three-level BTB converters, nowadays, are based on the three-level NPC inverter as shown in Fig. 12.

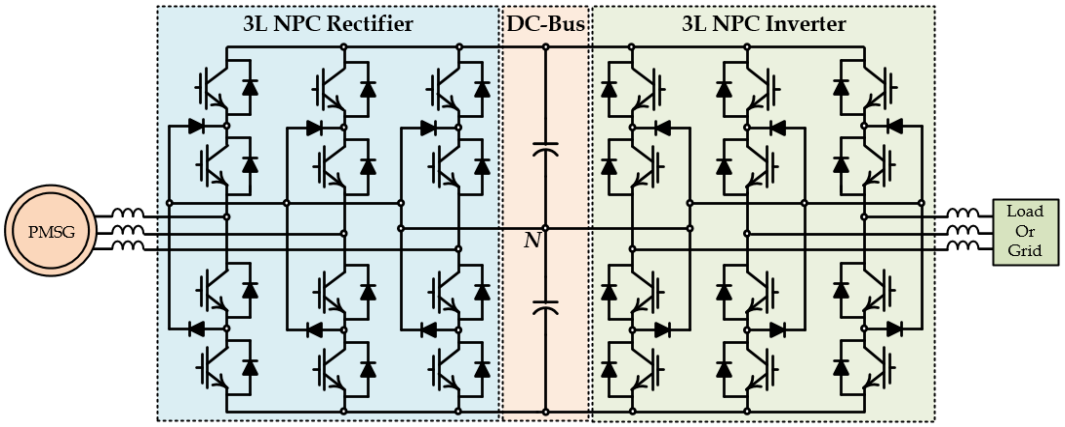


Fig. 12. Back-To-Back NPC configuration.

For unidirectional power flow applications, the unidirectional three-level BTB converter (U3L-BTB) proposed in [62] can be used. This type of converter has

been obtained using the Vienna rectifier, as depicted in Fig. 13.

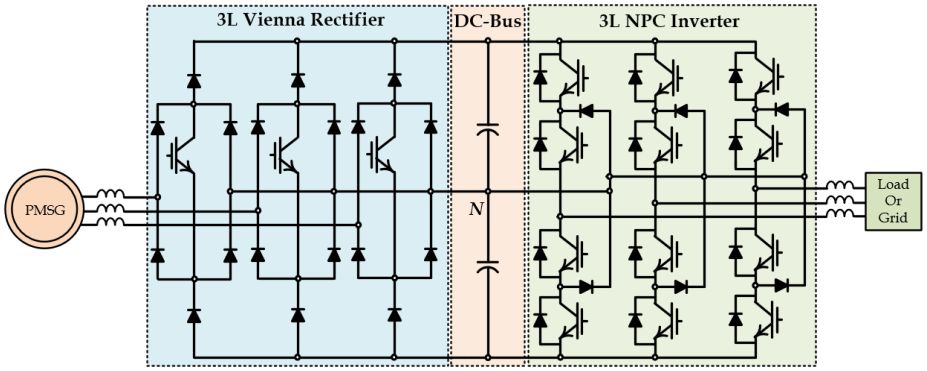


Fig. 13. Unidirectional 3L BTB (U3L-BTB) converter.

The BTB converters based on the FC inverter, as shown in Fig. 14, can achieve the same tasks of the previous configuration. The main advantage of the topologies shown in Fig. 12 and Fig. 14, besides their regenerative operation, is that the same hardware is required for both rectifier and inverter side; however, different control strategies are required. The rectifier control is achieved to control the input current, obtaining lower distortions than configurations based on diode rectifier and multi-pulse transformer.

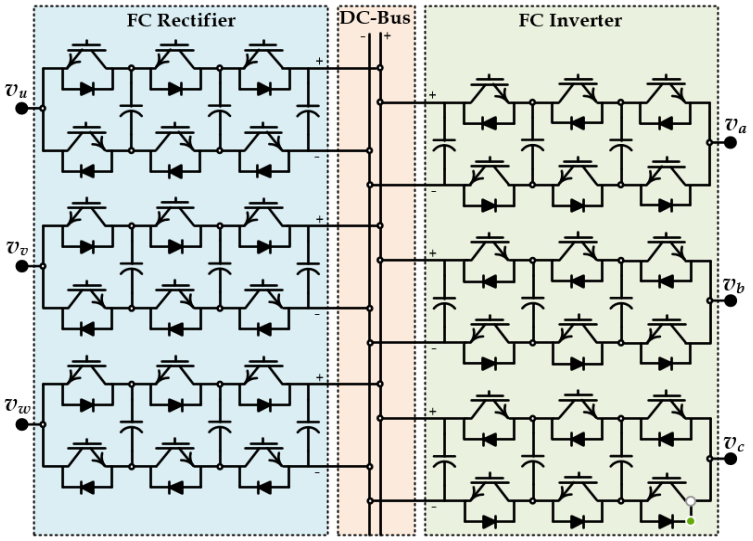


Fig. 14. Back-To-Back FC configuration.

With reference to Cascaded H-bridge converters, replacing the diode rectifier with the three-phase voltage source rectifier or active front-end rectifier, for each power cell, the three-phase active front-end rectifier-based power cell is obtained, as shown in Fig. 15. However, the input transformer that feeds the rectifier cannot be eliminated, because it is needed in order to provide the required

isolated DC sources.

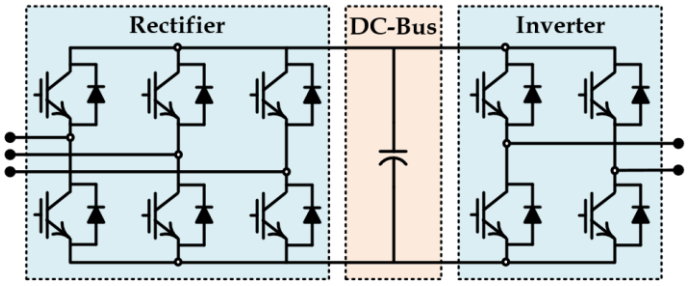


Fig. 15. Three-phase active front-end rectifier-based power cell.

Afterwards, in order to improve the efficiency and the effectiveness of the power conversion systems, new BTB topologies with an extension to the multilevel converters based on the five-level diode clamped topology have been introduced.

2.3.1 Five-Level Converter Topology

In [63] a BTB multilevel converter topology has been presented. This power generating system can be either interfaced with a utility or used as an autonomous backup UPS system. The backup UPS system has been implemented with a five-level diode-clamped rectifier (5LDCR) and a five-level diode-clamped inverter (5LDCI) in BTB configuration, as depicted in Fig. 16.

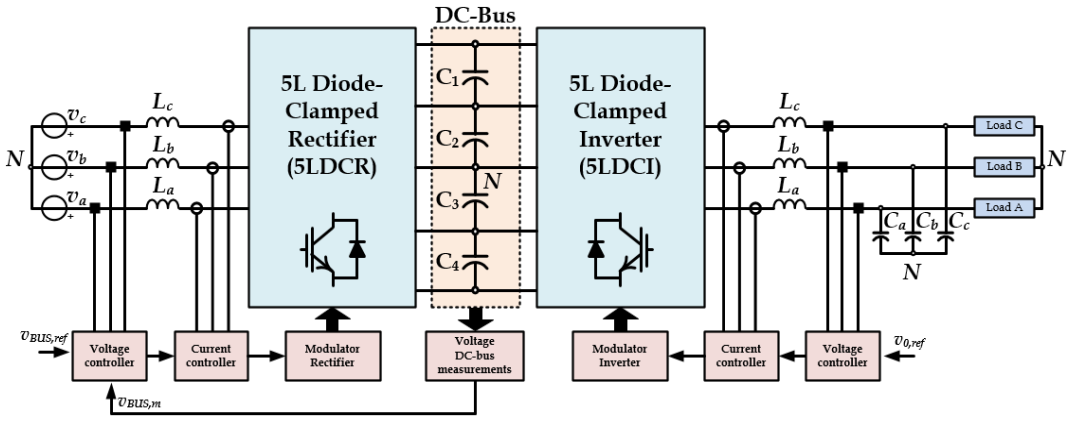


Fig. 16. Grid-connected system with multilevel converters.

The 5LDCI, or also called 5L I-type inverter, used in this configuration is shown in Fig. 17. The 5LDCI is capable to operate with balanced loads (symmetrical phases) or with fully unbalanced loads (asymmetrical phases) in each phase individually, whereas an unbalance loading should not affect the output voltage

regulation.

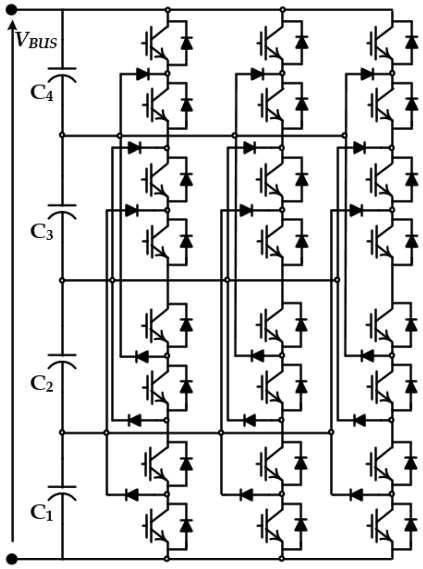


Fig. 17. Conventional three-phase 5LDCI (or 5L I-type) inverter.

An improved capacitor voltage balancing method for five-level diode-clamped converter has been presented in [64]. This converter consists of 36 diodes, 12 diodes for each phase. Voltage balancing of the DC-link capacitors is another issue with this topology which has been studied comprehensively in [64]. A generalized approach of the backup system for the design of n-level generic BTB system with the generic n-level diode-clamped rectifier and inverter has been explained in [65]. When the number of voltage levels increases, the number of the power semiconductor or flying capacitors increases greatly. CHB topology can be easily extended to higher-level applications due to its modular design. Unfortunately, each H-bridge cell requires an isolated DC supply, which generally is obtained by the multi-pulse diode rectifier. The high complexity and cost of the phase shifting transformers are the main drawbacks when higher voltage levels are required. Moreover, the high number of series connected devices can cause the same high conduction loss as in the I-type 5L-NPC. In order to derive high performance converters five or more levels with simplified structure converters have been introduced and developed based on the combination of the basic multilevel topologies. In [66] is shown the five-level converter with reduced number of clamping diodes. This topology is the

combination of the two-level and the three-level converter cells and can be easily extended to the multilevel converter with higher number of levels. A three-phase five-level 10 kW converter/inverter system based on this topology is depicted in Fig. 18, [66].

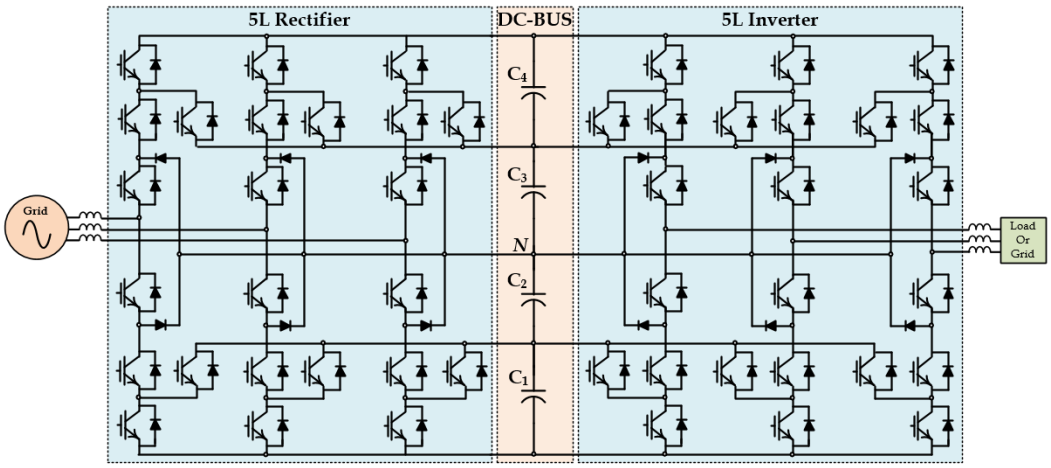


Fig. 18. Schematic of the 5L Rectifier/Inverter system.

Recent surveys show that the T-type topology has been proposed as valid alternative to the NPC topology [67], [68], [69]. A five-level inverter based on multi-state switching cell applied to the T-type converter called 5L T-Type-MSSC [19] has several advantages compared with the 5L NPC-MSSC topology [70]. The 5L T-Type-MSSC presents fewer semiconductors, because it does not need clamping-diodes, reducing the cost of the converter; during the operating intervals, the number of conducting semiconductors is smaller, representing a reduction in total losses and, consequently, a higher efficiency. Also in photovoltaic and fuel cell applications the T-type topology has been proposed in order to achieve better performance than the 5L I-type inverter [71], [72], [73]. A variant of the 5L-NPC inverter based on the equivalent matrix structure is then developed in [74]. The equivalent matrix structure is applied to high power induction machine electric drives and the general structure of the three-phase five-level NPC voltage inverter is shown in Fig. 19. The extension of this topology of inverter to generic n-level voltages has been investigated in [75]. As will be described in more detail in the next section, DC-link capacitors increase with the

number of levels; thus, due to the rectifier and inverter inject currents into DC-bus capacitors, the voltage unbalancing across the capacitors is the main issue of this topology.

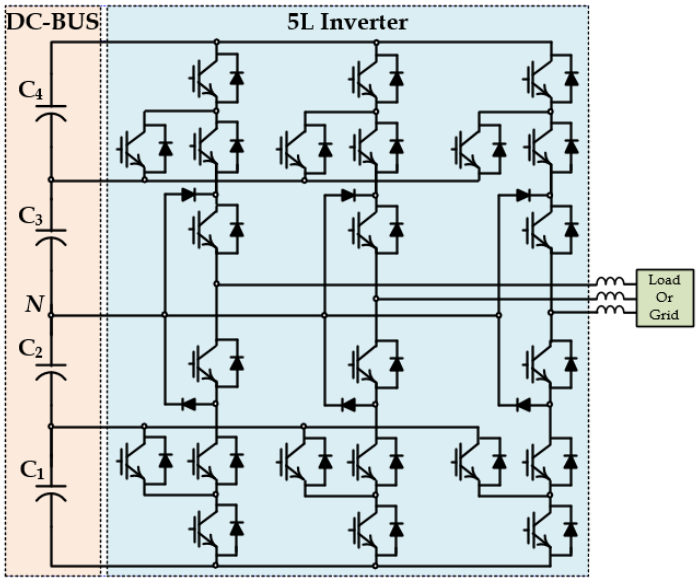


Fig. 19. General structure of the three-phase 5L NPC Inverter.

In other words, the average currents injected by the rectifier and inverter are zero only in an ideal case, namely when the modulation depths and the switching delays of both converters are identical. These conditions never occur in real applications. Accordingly, a careful control of converters and an additional circuit should be used in order to balance the DC-bus voltages across the capacitors. Fig. 20 shows the generalized multilevel inverter topology per phase-leg [76]. The existing multilevel inverters such as diode-clamped and capacitor-clamped multilevel inverters can be derived from this generalized inverter topology. The generalized N-level phase-leg is a horizontal pyramid of the basic cells (P2 cell). Since the basic cell is a two-level phase-leg, this generalized multilevel inverter is also called the P2 multilevel inverter. The advantage of this topology is its ability to balance each voltage level by itself regardless of the inverter control and load characteristics. For DC-AC energy conversion systems, the emerging multilevel inverter topologies for higher levels can be the best candidates as the second conversion stage in BTB configurations.

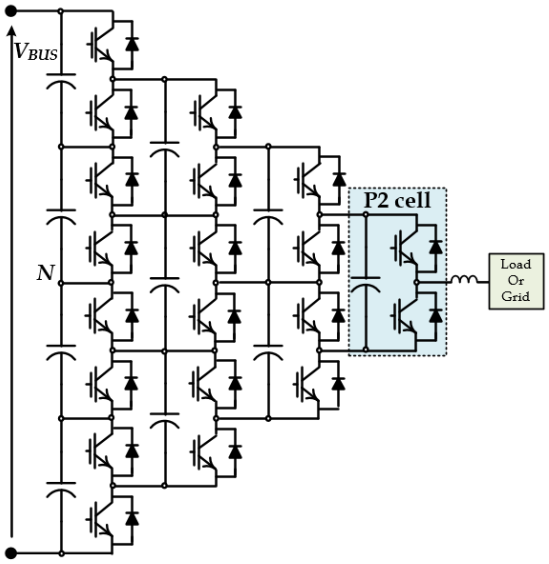


Fig. 20. A five-level Generalized Multilevel Inverter or P2 multilevel inverter.

In recent years, several topologies with five-level structure have found practical applications which are commercialized by manufacturers. ABB introduced and employed in the market the product ACS 2000 system, a new 5-level active neutral-point clamped topology composed of active NPC and FC configuration (5L-ANPC) [77], [78], as shown in Fig. 21. The main drawback of the 5L-ANPC is that the voltage ratings of the power semiconductors are different; the outer switches are subjected to half of the DC-link voltage, whereas the inner devices have only one-fourth of the dc-link voltage.

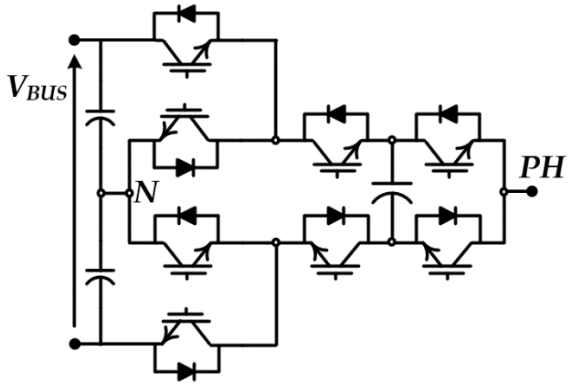


Fig. 21. Three-phase 5L-ANPC inverter.

This limits the voltage rate of the converter for higher voltage applications [79]. In [20], [80], [81] a five-level H-bridge NPC (5L-HNPC) inverter, where the H-bridge cells are composed of two classic three-level NPC phase legs, is proposed

and applied in the industry. This topology, depicted in Fig. 22, requires three isolated DC sources fed by a phase shifting transformer and a number of diode bridges. The bulky phase shifting transformer increases also cost and complexity of the converter. Another inverter that has attracted a great deal of practical interest in industry due to a number of advantageous features is called five-level flying capacitor (FC) converter [82], [83].

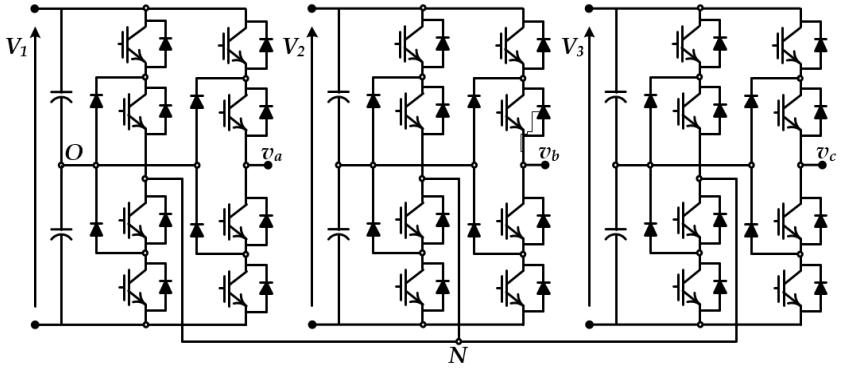


Fig. 22. Three-phase 5L-HNPC inverter.

In this converter, shown in Fig. 23, there are two main issues: the number of flying capacitor and the regulating voltages of the flying capacitors. In practical applications, the manufacturers try to reduce the number of capacitors.

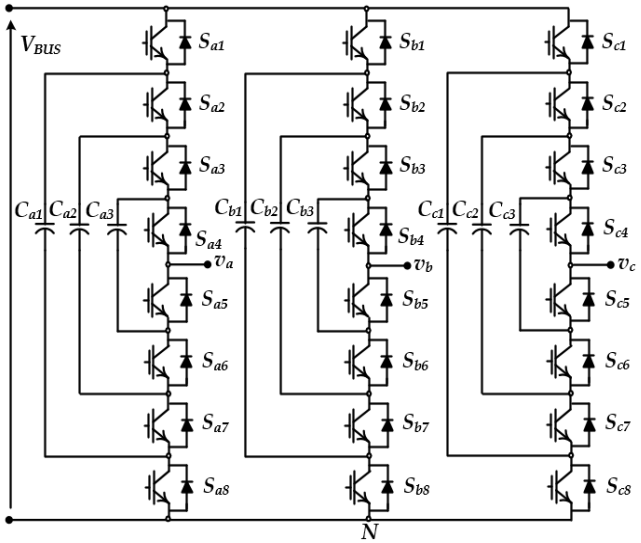


Fig. 23. Three-phase five-level flying capacitor (FC) inverter.

A novel four-level-nested neutral point clamped (NNPC) converter has been proposed in [84]. The NNPC inverter is a newly developed four-level voltage source inverter for medium-voltage applications with properties such as

operating over a wide range of voltages (2.4–7.2 kV) without the need for connecting power semiconductors in series and high-quality output voltage [85].

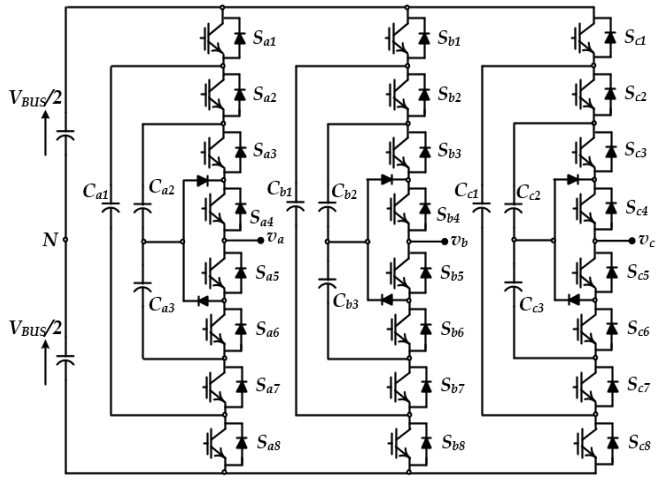


Fig. 24. New three-phase five-level neutral-point clamped (NNPC) inverter.

Recently, the new five-level voltage source converter shown in Fig. 24, that is based on the upgrade of a four-level NNPC converter, has been proposed in [86].

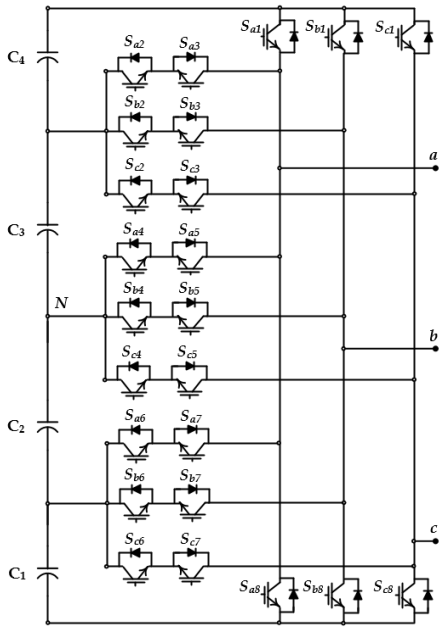


Fig. 25. Three-phase Five-Level E-Type Converter.

As describes in more details [86], this inverter can operate over a wide range of voltages without the need for connecting power semiconductors in series, it has high-quality output voltage and fewer components compared to other more conventional five-level topologies. Finally, a power converter topology, called Five-Level E Type Inverter, is presented and analyzed in [14] regarding the BTB

configuration with a multi-level rectifier. The circuit diagram of the converter is shown in Fig. 25.

2.4 Some Disadvantages and Drawbacks of Multi-Level Converters

2.4.1 Voltage Balancing Issue

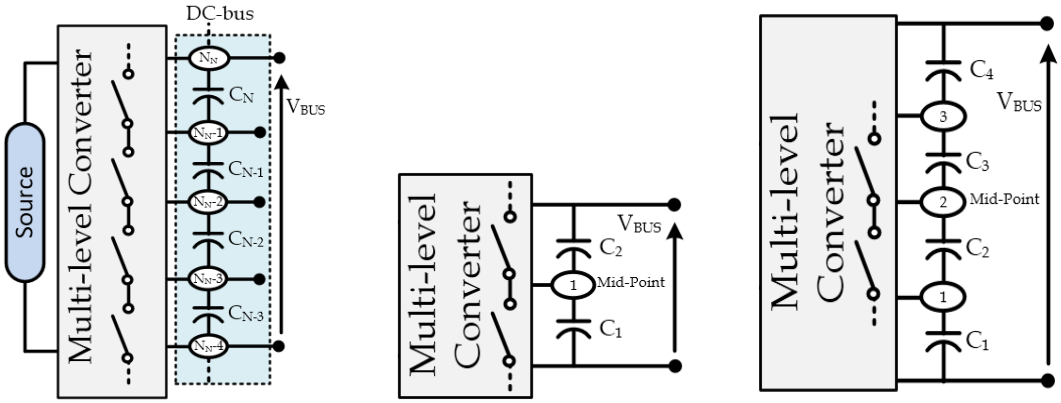
When the number of levels is increasing the number of series connected DC-bus capacitors is increasing too. According to the equation (2), for I-Type and T-Type multi-level topologies the number of series connected capacitors, N_S, depends on number of levels, N. As it is shown in Fig. 26a, the number of DC-bus nodes, N_N, is given by equation (3).

$$N_S = N\text{-}1 \tag{2}$$

Using the first Kirchhoff's law at the DC-bus nodes of the circuit, it is easy to understand as the currents that flow into DC-bus capacitors, C_N , C_{N-1}…, are not the same.

$$N_N = N\text{-}2 \tag{3}$$

Thus, the DC-bus voltages across the series capacitors are not equal.



(a) (b) (c)

Fig. 26. a) Multi-level Converter plus DC-bus capacitors, b) DC-bus capacitor for 3-Level converter, c) DC-bus capacitors for 5-Level converter.

The main issue of the I-Type and T-Type multilevel topologies and their variants is the unequal voltage sharing among the series connected capacitors that results

in DC-bus capacitors unbalancing. When the number of levels is set to 3, we have only one node (Mid-point), Fig. 26b. If the converter is controlled with pulse width modulation (PWM) techniques [87], the converter modulation index is given by the equation (4), where m_0 is the offset of the modulation index, M_0 is the modulation depth and ξ=0,1,2. It can be proven that the average current into the mid-point depends on the modulation index offset m_0. Therefore, controlling the modulation index offset m_0 it is possible to achieve an equal voltage distribution among the series capacitors.

$$m_{A,B,C}(t) = m_0 + \frac{1}{2}\left[1 + M_0 \sin\left(\omega_0 t - \xi\frac{2\pi}{3}\right)\right] \quad (4)$$

Equation (4) is valid only for 3-phase 3-wire converters. In case of 3-phase four-wire converters, the modulation index offset m_0 is zero due to the short circuit between neutral and common star point. Mid-point voltage balancing problem of three-level NPC topology has been widely addressed in literature. Many control strategies to fix this problem have been presented in the last years [54], [63], [87]. Several methods were introduced for the DC-bus neutral point voltage balancing, some of them make use of the equivalent states (redundant state-space vectors), some other use feedback voltage control and other few use the feedback DC current sign detection [18], [88], [89]. Additionally, some of the proposed algorithms avoid the narrow pulse problems, minimize the losses by avoiding the switching of the highest internal current, or share the balancing task with the active front-end inverters [82], [90], [91], [92].

Considering the 5-Level Converter, we have three nodes, Fig. 26c. As mentioned above, the current injected into mid-point can be controlled using appropriate control strategies. The currents injected into node 1 and node 3 are not controllable variables. Thus, when the voltage balancing through the modulation is not achievable, available or for other reasons not implemented, additional circuits can be used to balance the capacitors' voltages. These balancing circuits aim to charge or discharge the capacitors so that they keep balanced the voltage.

There are many ways to implement balancing circuits; a Back-to-Back converter [93], a buck-boost converter, a multilevel boost converter [42], [94]. However, these methods may increase the volume of the converter and have a disadvantage in realization of converters with high output power density. To solve these problems, Series Resonant Balancing Circuit (SRBC) has been introduced. One example for the balancing circuit of the multi-level converter has been implemented in [39], [40], [95].

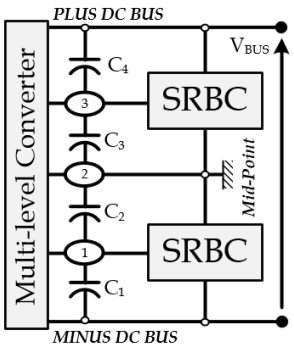


Fig. 27. Equivalent circuit diagram of a SRBC.

A generalized block diagram of a Series Resonant Balancing Circuit (SRBC) is depicted in Fig. 27. The first SRBC is connected between MINUS DC BUS, MID POINT and node 1; the second SRBC is connected between PLUS DC BUS, MID POINT and node 3. As extensively discussed in [42], [95], the balancing converter is a variant of the switched capacitor converter. The balancing converter works in discontinuous conduction mode (DCM), type 1 [42].

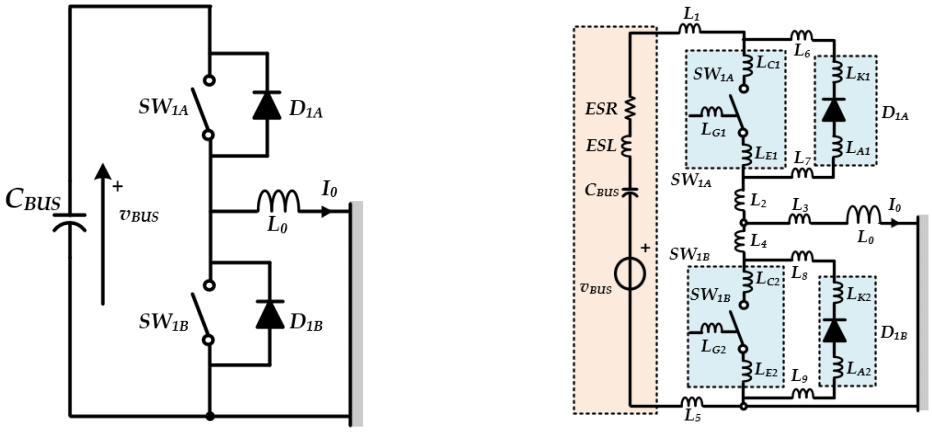
2.4.2 Total Commutation Inductance Issue and Commutation Path

Any network, passive components and power semiconductors introduces a stray inductance due to their physical and geometric characteristics. As the current path length increases, connection and devices stray inductances are also increasing. Why is it so important the stray inductance? Is really very important for many reasons. With high switching speeds, high power handling requirements and finite size, the stray inductance becomes a crucial factor in design of power converters, especially in the power converters hosting the

discrete switching devices. The presence of the stray inductance leads to over-voltages

$$\Delta v = L_{\xi} \frac{di_{sw}}{dt}, \tag{5}$$

where L_{ξ} is the total commutation inductance and di_{sw}/dt the device current slope. Having a power board layout with low stray inductance allows reducing the switching losses due to the lower switching time and to choose devices with a lower voltage rating. Devices with a lower voltage rating enable to reduce the conduction losses caused by semiconductor resistance. It is obvious that higher efficiency leads to smaller amount of heat produced by power converters, which means smaller heat sinks and cooling efforts. Consequently, we are going to have smaller and cheaper power converters. For these reasons, designers of power converters try to minimize stray inductance as much as possible. To do this, the commutation paths in the power converters' circuits should be as short as possible.



(a) (b)

Fig. 28. a) Basic switching cell converter, b) Equivalent circuit diagram of the Basic switching cell converter.

To explain the dynamics related to the commutation path, let us start considering the basic switching cell of power electronics, Fig. 28a. Many converter topologies have been proposed and analyzed to perform different types of power conversion. Actually, most of the existing power electronics converters are composed by the basic switching cell repeated over and over again.

The basic switching cell is composed by two switching devices, IGBTs and/or MOSFETs, with anti-parallel freewheeling diodes and DC source. Fig. 28b shows explicitly the stray inductances in the various parts of the circuit.

$$L_{\xi} = L_{\sigma} + ESL + L_{SW} \tag{6}$$

According to the equation (6), the total commutation inductance L_{ξ} is given by three parameters: 1) inductance introduced by connections L_{σ}, 2) inductance related to the DC-bus capacitors ESL, and 3) inductance associated with the die and wire bond of the power semiconductors, L_{SW}. For example, if the current path includes the device SW_{1a} and the diode D_{1B} the inductance $L_{\sigma}=L_1+L_2+L_4+L_5+L_8+L_9$ and the inductance $L_{SW}= L_{C1} +L_{E1}+L_{K2} +L_{A2}$. If the current path involves the device SW_{1B} and the diode D_{1A} the inductance $L_{\sigma}=L_1+L_2+L_4+L_5+L_6+L_7$ and the inductance $L_{SW}=L_{C2}+L_{E2}+L_{K1} +L_{A1}$. ESL is related to the capacitor technology, L_{σ} depends on the components placement and the arrangement of the circuit and L_{SW} is linked to packaging and the PCB arrangement [12], [96], [97].

When a semiconductor is turned off during normal operation the current has been flowing through that device. The previous current path is no longer existent due to the device turn-off. This process of passing the current from one to another path is called commutation. The commutation path depends on the power converter topology (rectifier or inverter) and the operating power factor. The commutation path will change depending on the direction of the output current, particularly whether it has the same or opposite polarity with respect to the voltage. The name "short/long" commutation path also indicates the geometric length of the commutations. It is obvious that the "long" commutation path results in high value of the total commutation inductance.

2.4.2.1 Three-level Converters

When we have the inductive load, the output voltage and current waveform are shown in Fig. 29a. For any value of power factor between ±1 the phase shift changes and the converter operation can be divided in two operating areas: 1)

$V_0>0$, $I_0>0$; 2) $V_0<0$, $I_0<0$. The instantaneous power is positive in area 1; the output voltage and output current are of opposite signs in area 2, thus, the instantaneous power is negative. Let us starting to analyze the basic switching cell converter. According to the operating areas, the commutation loop (highlighted in yellow) of the basic switching cell converter is depicted in Fig. 29b. The switching cell converter exhibits different current paths, Fig. 30.

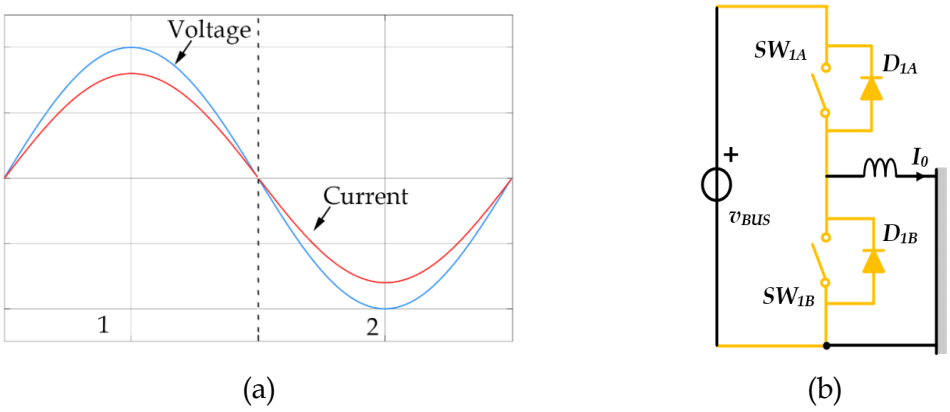


Fig. 29. a) Basic switching cell in operating areas; b) commutation loop.

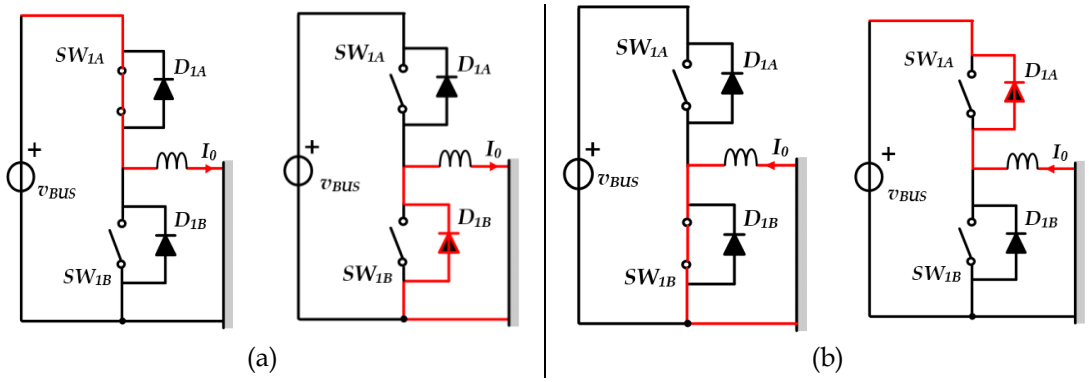


Fig. 30. Basic switching cell in operating areas: a) area 1, b) area 2.

In this case, there are no short or long commutation paths in the basic cell converter; all paths are of the same geometric length. What happens when the number of the converters voltage levels increase? According to the multilevel converters topology, the commutation paths can be either long or short depending on the modulation index. Furthermore, the current path involves more power devices, which means high commutation inductance and high conduction losses. Let us consider a single-phase three-level NPC Inverter and its variant T-Type NPC Inverter (T-NPC Inverter). Considering Fig. 31, the

commutation loops of operating areas are depicted in Fig. 32, Fig. 33, Fig. 34 and Fig. 35. In operating area 1 and 3, the commutation loop involves two power devices for the NPC Inverter and three power devices for the T-NPC Inverter; in these areas, T-NPC Inverter shows longer commutation loop compared to the classic NPC Inverter. In operating area 2 and 4, commutation loop includes four power devices for the NPC Inverter and three power devices for the T-NPC Inverter; in these areas, T-NPC topology exhibit shorter commutation loop compared to the classic NPC Inverter.

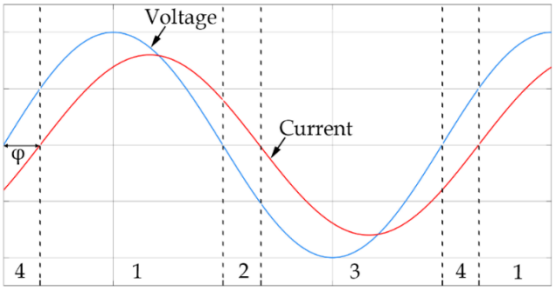


Fig. 31. Operating areas.

Practically, in the T-NPC Inverter there are no short or long commutation paths; all paths are of the same geometric length and the commutation occurs between one outer switch (SW_1 or SW_4) and two inner switches (SW_2, SW_3). On the other hand, the NPC Inverter presents short commutation paths (e.g. area 1 and 3) and long commutation paths (e.g. area 2 and 3). Consequently, T-NPC Inverter shows on the whole a better commutation loop, which means lower stray inductance and lower overvoltage.

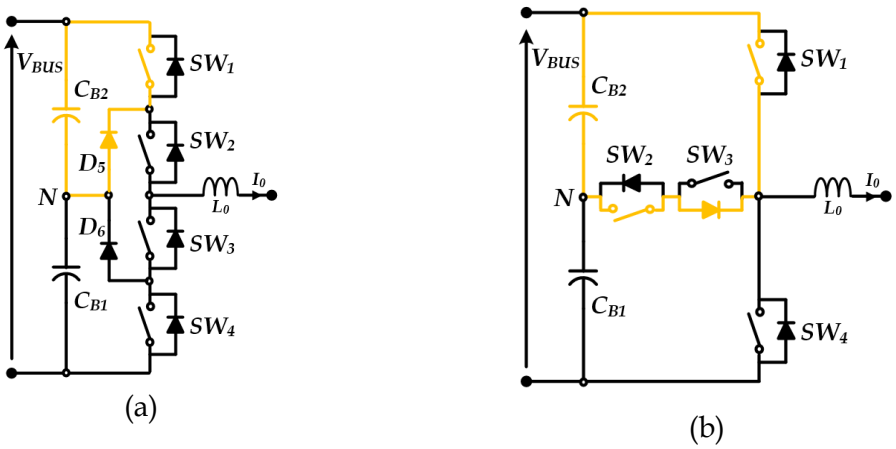
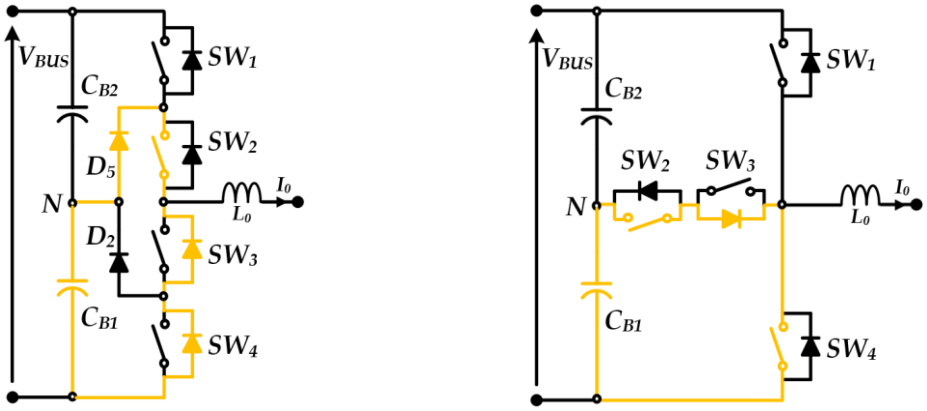
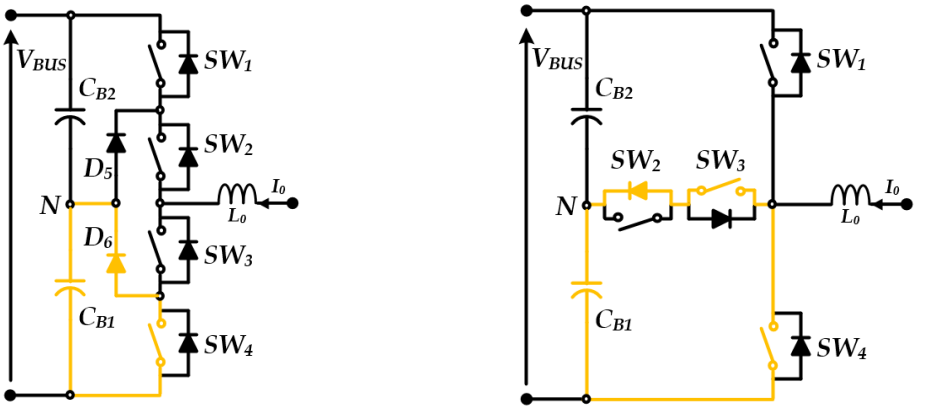


Fig. 32. Commutation loop for operating area 1: a) NPC, b) T-NPC.



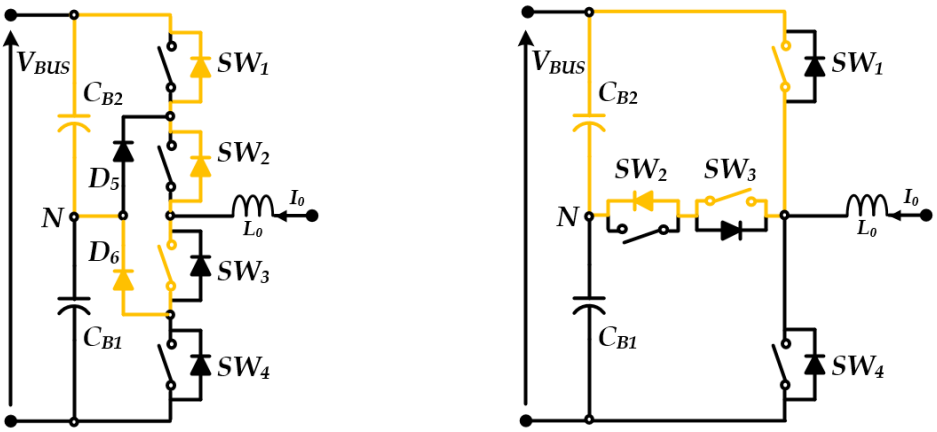
(a) (b)

Fig. 33. Commutation loop for operating area 2: a) NPC, b) T-Type.



(a) (b)

Fig. 34. Commutation loop for operating area 3: a) NPC, b) ANPC, c) T-Type.



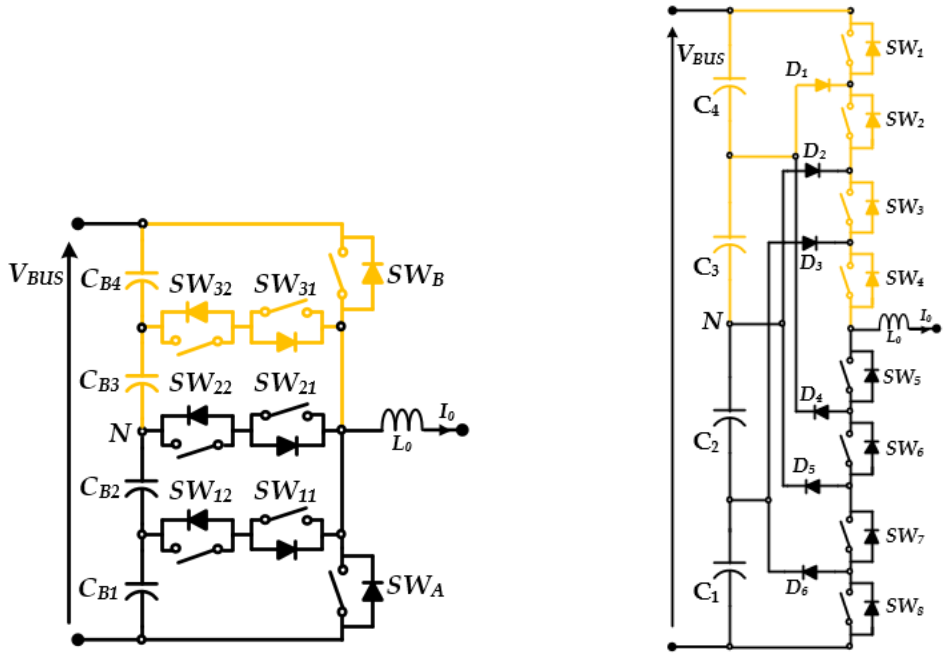
(a) (b)

Fig. 35. Commutation loop for operating area 4: a) NPC, b) T-Type.

2.4.2.2 Five-level Converters

The 5L E-Type Converter shows in Fig. 25 is an improvement of Three-level T-Type Converter. Adding two DC-bus capacitors and two bidirectional power semiconductors in the top-middle and bottom-middle circuit of Three-level T-

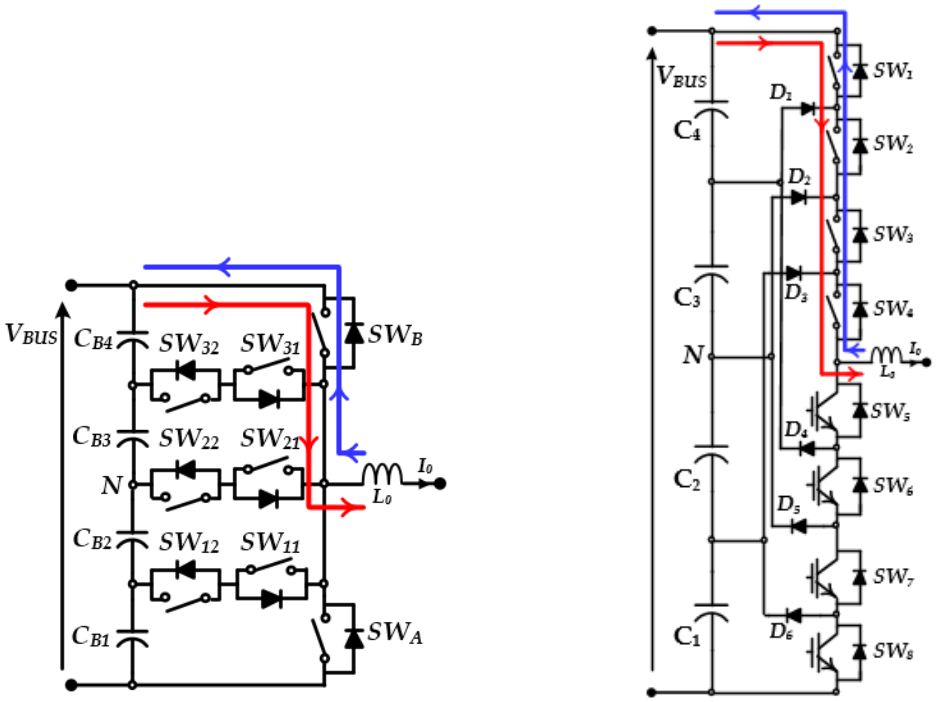
Type Converter, we can obtain a 5L E-Type Inverter used as AC-DC power conversion in the proposed three-phase 5L E-Type Back-To-Back Converter [14].



(a) (b)

Fig. 36. Commutation loop for high modulation depth: a) 5L E-Type Inverter, b) 5L I-Type Inverter.

When the modulation depth is high the 5L E-Type Inverter and the 5L I-Type Inverter (see Fig. 17) operate with five voltage levels. As shown in Fig. 36, it easy to understand that the 5L E-Type Inverter shows a better commutation loop compared with 5L NPC Inverter and 5L I-Type Inverter. Fig. 37 shows the current path in the 5L E-Type Inverter and the 5L I-Type Inverter during the peak of the positive modulation index. In the 5L E-Type Inverter, the current flows through only one power device, SWB, Fig. 37a. As depicted in Fig. 37b, current path in the 5L I-Type Inverter includes four power devices. The longer current path in the 5L I-Type Inverter causes higher overvoltage due to the high commutation inductance. Consequently, the voltage rating of the power semiconductors is increasing. Thus, the 5L E-Type inverter shows better conduction losses compared to the 5L I-Type Inverter.



(a) (b)

Fig. 37. Current path during the peak of modulation index: a) 5L E-Type Inverter, b) 5L I-Type Inverter.

3 PATENTS REVIEW

3.1 Patent review on three-phase multi-level topologies

The objective of this section is to provide a comprehensive review of relevant patents to find out the solutions being proposed by industries. It is of high relevance to identify which kinds of multilevel converters are used in UPS and PV applications, as it is useful for the further investigations in order to find new solutions that can create opportunity for growth within the industry. BTB systems and multilevel converters protected by patents are listed as follows.

Patent References	Description
[98]	A power flow controller with a fractionally rated BTB converter is provided. The power flow controller provides dynamic control of both active and reactive power of a power system. The fractionally rated BTB converter comprises a transformer side converter (TSC), a direct-current (DC) link, and a line side converter (LSC). By controlling the switches of the BTB converter, the effective phase angle between the two AC source voltages may be regulated, and the amplitude of the voltage inserted by the power flow controller may be adjusted with respect to the AC source voltages.
[99]	An AC-AC converter system includes transformers and converter units on primary and secondary sides of the system, respectively. The converter system is connected to first and second AC networks and the converter units are interconnected by means of a DC link. By integrating at least part of two transformers connected to the first and second network respectively into one transformer unit, a cost-efficient

	transformer configuration can be achieved.
[100]	A multilevel converter-based, intelligent, universal transformer includes back-to-back, interconnected, multi-level converters coupled to a switched inverter circuit via a high-frequency transformer. The input of the universal transformer can be coupled to a high-voltage distribution system and the output of the universal transformer can be coupled to low-voltage applications. The universal transformer is smaller in size than conventional copper-and-iron based transformers, yet provides enhanced power quality performance and increased functionality.
[101]	The present invention relates to an uninterruptible power supply, more specifically, to an uninterruptible power supply for the backup of AC-power supply which includes an electric double layer capacitor as an energy storage device. The uninterruptible power supply according to the present invention comprises an AC power source, a AC-DC converter, an energy storage device and a DC-AC inverter. The uninterruptible power supply has highly enhanced energy efficiency and power backup time, compared even to the conventional DC power backup system such that efficient power backup can be achieved.
[102]	Pre-charging and dynamic braking circuits are presented for multilevel inverter power stages of a power converter with a shared resistor connected to charge a DC bus capacitor with current from the rectifier circuit in a first operating mode and connected in parallel with the capacitor to dissipate power in a dynamic braking mode.
[103]	Aspects of the invention provide methods and apparatus for

	providing uninterruptible power. The uninterruptible power supply includes a first input to receive input power from an input power source, an output to provide output power, a bypass input to receive bypass power from a bypass power source. The uninterruptible power supply is constructed and arranged in a bypass mode of operation to control the inverter circuit to convert AC power from the bypass power source at the output of the inverter circuit to DC power at the input of the inverter circuit.
[104]	A method for parallel non-redundancy operation of uninterruptible power supply equipment having a bypass circuit without using an additional common circuit. In the method of operating in parallel uninterruptible power supply equipment, each apparatus has two operational modes, a bypass feeding mode and an inverter feeding mode. An off-instruction for an AC switch that is turned on in the bypass feeding mode of one of the uninterruptible power supply apparatuses is produced in the respective uninterruptible power supply apparatuses when operated in the inverter feeding mode. The off-instruction is produced based on detection of coincidence of a bypass feeding signal which is active during the bypass feeding mode and a ready signal which becomes active when the inverter feeding mode is ready.
[105]	A three-phase 5L T-type MSSC inverter presents three input terminals (P, MP, N) and three output terminals. The inverter further comprises a first multi-state switching cell (MSSC), comprising three input terminals, respectively connected to the input terminals P, MP, N of the inverter, and a first output terminal.

[106]	The new three-phase NNPC inverter with a controller that operates the switches of the inverter and switched capacitor circuit to provide a multilevel output voltage has been implemented. The switches of the NPC core and the switched capacitor circuit being gated using selected redundant switching states to control the voltage of the switched capacitors to achieve a multilevel output voltage having equally spaced voltage step values.
[107]	A five-level power converter and a control method for the same are provided. The five-level power converter includes an inverter and at least a rectifier. The rectifier includes at least one rectifier control circuit and four capacitors which are divided into two groups, each with two capacitors connected in parallel, where a first end of a first capacitor to a fourth capacitor is grounded. The inverter includes a discharge control circuit, and a first inductor unit and a first load connected in series. A five-level power converter and a control method provided in embodiments of the present invention may implement operations in five-levels and may be applied to a UPS system.
[108]	A five-level hybrid inverter include a first boost apparatus, a second boost apparatus, a first half-cycle switching network coupled to the first boost apparatus. The first half-cycle switching network is configured such that a first three-level conductive path is formed when a voltage at a dc source is greater than an instantaneous value of a voltage at an output of the inverter. A first five-level conductive path is formed when the instantaneous value of the voltage at the output of inverter is greater than the voltage at the dc source.
[109]	A high voltage inverter cascades a plurality of multiple voltage

	level inverter modules each fed by an isolated dc energy unit to reduce the number of stages of the inverter required to generate a desired ac voltage has been invented. Thus, where the dc energy unit includes the secondary winding of an AC transformer, the number of each winding needed is reduced. By using active rectifiers operated in a boost mode to convert the transformer secondary voltage to dc for powering the inverter modules, regenerative operation can be achieved.
[110]	A five-level topology unit non-isolated is used with a first DC power supply and a second DC power supply. The five-level topology unit include a floating capacitor that is charged by the first DC power supply or the second DC power supply and a half-bridge inverter module that outputs five mutually different voltage levels including zero.
[111]	A multilevel inverter with flying capacitor topology, either single phase or three phase is realized. Additionally, the control system allows the use of low-voltage MOSFETs (e.g. 80V) in order to form an equivalent switch of higher voltage (e.g. using six 80V MOSFETs resulting in an equivalent 480V switch). The conduction and switching characteristics of the low voltage switching multi-level inverter are substantially and unexpectedly improved over other multi-level inverter implementations.
[112]	The present invention discloses the multilevel-clamped multilevel converter (MLC2). In this invention, the multilevel clamping concept is devised, whereby one manages a DC bus voltage, comprised of multiple DC bus voltage nodes, or more multilevel clamping units (MCUs) to convey a higher number of levels for synthesizing the output waveforms of a DC-AC

	multipoint clamped (MPC) power conversion structure. Thus, the resulting converter has the number of levels increased when compared with conventional MPC multilevel solutions, which is very important for improving power quality, while the overall structure is kept simple, wherein the number of components can be considerably reduced.
[113]	Cascade H-Bridge inverters and carrier-based level shift pulse width modulation techniques are presented for generating inverter stage switching control signals, in which carrier waveform levels are selectively shifted to control THD and to mitigate power distribution imbalances within multilevel inverter elements.
[114]	A high-power motor drive converter includes a five-level hybrid NPC output power conversion stage including three NPC phase bridges. Each NPC phase bridge receives power on a respective direct current bus. This invention also includes three isolated split series-connected DC capacitor banks each coupled in parallel to a respective one of the three NPC phase bridges and a controller for selecting switch positions with active control of neutral voltages. The controller is adapted to select switch positions using feedforward sine-triangle modulation with third harmonic injection, zero sequence injection, and/or discontinuous modulation injection.
[115]	An adjustable frequency multiphase power supply provides low harmonics to the line and the loads. The power supply having a plurality of power cells in each phase output thereof, each cell having an input side, and an output side. The input side is capable of converting single-phase AC into DC and for converting DC into AC to said source. The output side is capable

	of converting DC into a controlled AC output and for converting AC from said load to feed said DC bus. The respective outputs and respective inputs of the cells are series connected. Each cell can have a single-phase transformer connected either to the input side or the output side. The output side of each cell can be controlled to limit the harmonic content of the output AC to the load, and the input side of each cell can be controllable to limit harmonic content of the AC power feed to the source. The input and/or output sides can be interdigitated to limit harmonic components to the source and/or to reduce the harmonic content of the AC supplied to the load.
[116]	An embodiment of the present invention comprises a multi-level PWM inverter that is constructed by cascading multi-level H-bridge inverters and providing different voltage inputs to the multi-level H-bridges. The values of the voltages, or the ratios of the voltages, are selected in order to provide an increased number of output levels. In the cascaded arrangement, at least one of the multi-level H-bridge inverters has more than three levels. Preferably, at least one of the multi-level H-bridge inverters is a 5-level inverter. According to one aspect of the invention, the cascaded arrangement may use a primary 5-level H-bridge with at least one 3-level H-bridge (referred to as a "5/3H" arrangement). This arrangement can provide up to fifteen output levels if regenerative voltage sources are used, and up to eleven output levels if a non-regenerative voltage sources are used.
[117]	A single unit, four switching devices and two diodes configure each phase of a three-level power converting apparatus. In each unit are arranged along a flow direction of cooling air on a heat

	sink of a cooling device with long sides of the switching devices and the diodes oriented perpendicular to the flow direction of the cooling air. The first and second diodes are arranged in a central area of the heat sink, whereas the second switching device and the third switching device with high heat generation loss are arranged in a distributed fashion to sandwich a group of diodes in the central area in between.
[118]	A novel topology of multilevel external point piloted converters has been designated. A voltage inverter has been characterized in that the N−1 generators comprise 3N−5 series connected elementary direct voltage generators, the two terminal generators of the N−1 generators connected directly to one of the two input voltage terminals comprising two elementary direct voltage generators and the other generators of the N−1 generators comprising three elementary generators.
[119]	The NPC power converter fault protection system is provided, and include a DC bus, a switching network, a control module and method of controlling a NPC.
[120]	A method of controlling a three-phase three-level NPC inverter is realized. The method includes regulating the electrical potential of the mid-point when the inverter operates at full voltage, that is to say in over-modulation.
[121]	A multi-level medium-voltage inverter that receives three-phase power and outputs a three-phase voltage to a three-phase motor has been invented. The multi-level inverter includes a rectifying unit to rectify received a three-phase voltage, a smoothing unit to receive the rectified voltage and provide the rectified voltage as voltages having different levels to first to third different nodes and a unit power cell including a plurality

	of switch units to transfer the voltages having three levels provided from the smoothing unit. Two units power cells are provided per phase of the motor operated as a load, and the number of unit power cells may be increased as needed. A unit power cell is configured as a cascaded T-type NPC inverter to reduce conduction loss.
[122]	A full-bridge neutral point clamped (NPC) inverter having an input and an output converts a direct current voltage at the inverter input to an alternating current voltage at the inverter output acceptable for connection to a utility has been invented. The inverter further includes a pulse width modulator control unit having a predetermined carrier frequency. The control unit using for each carrier period either positive or negative values of a reference voltage to generate a predetermined number of signals to control the switching on and off of each of the eight switching elements.
[123]	The present invention relates to a multilevel inverter comprising a converter unit, a film capacitor rectifying the DC power source converted by the converter unit and an inverter unit converting the rectified DC power source to a three-phase current in response to a pulse width modulation (PWM) control signal. Moreover, the system includes a current detector detecting a current outputted from the inverter unit, a power cell main controller generating a voltage instruction and a voltage instruction using the detected current, and a PWM controller generating the pulse width modulation (PWM) control signal using the voltage instruction and frequency instruction.
[124]	A multi-level inverter having at least two banks, each bank containing a plurality of low voltage MOSFET transistors. A

	processor configured to switch the plurality of low voltage MOSFET transistors in each bank to switch at multiple times during each cycle.
[125]	A method for balancing a voltage of an inverter determines an expected voltage of a capacitor based on a voltage of the capacitor at a start of a switching cycle and determines a duty cycle minimizing a value of an objective function representing a difference between the expected voltage of the capacitor and a desired voltage of the capacitor. A switching sequence controlling the inverter is selected based on the duty cycle.
[126]	The present invention provides a three-level ac generating circuit and the control method thereof. The three-level ac generating circuit includes a three-level boosting circuit connected to an input source and a positive boosting portion and a negative boosting portion. A three-level inverting circuit connected to the three-level boosting circuit and including a positive inverting portion and a negative inverting portion, wherein while the input source is a relative low voltage, the relatively low voltage is boosted via the three-level boosting circuit, inverted and output via the three-level inverting circuit.
[127]	A solar module device with a back plane integrated inverter device includes a substrate member having a front side and a backside. The device has a plurality of solar cells, which includes a first group of solar cells connected in a first serial configuration and a second group of solar cells connected in a second serial configuration, and a tab wire configuration formed overlying the front side of the substrate member. The tab wire includes a first interconnection coupled to the first set of solar cells in the first serial configuration and a second

	interconnection coupled to the second set of solar cells in the second serial configuration. The device has an inverter device coupled to a backside of the substrate member. The inverter device includes a first set of connections coupled to the first interconnection and a second set of connections coupled to the second interconnection.
[128]	The multi-level DC/AC converter includes an input connectable to a direct voltage source, a half-bridge with a first controlled switch and a second controlled switch between which is positioned an output of the converter. A first connecting branch between the first controlled switch and the first connection and a second connecting branch between the second controlled switch and the second connection are present. A third controlled switch associated to the first controlled switch, connectable in series to the first controlled switch to generate an output voltage exceeding a first limit value, a fourth controlled switch associated to the second controlled switch, connectable in series to say second controlled switch to generate an output voltage below a second limit value are included.
[129]	A control system for a multilevel converter includes a differential mode current regulator, a neutral point (NP) controller and a PWM controller for generating switching pulses for the multilevel converter. The differential mode current regulator generates reference voltage command signals based on a difference between reference current command signals and actual current command signals, and the NP controller determines a modified neutral point current signal in response to a DC link voltage unbalance. The NP controller utilizes the modified neutral point current signal to generate a common

	mode reference voltage signal. The PWM controller based on the reference voltage command signals and the common mode reference voltage signal generates the switching pulses.
[130]	A method for controlling a switching device of a multilevel converter includes dynamically selecting a carrier and generating a switching signal to affect a switching event of the switching device based on a comparison of the dynamically selected carrier with a reference signal. The carrier is dynamically selected from a multiple carrier; each corresponding to one of multiple contiguous bands into which range of a waveform of the reference signal is divided. The carriers corresponding to different bands have differing waveform shapes. The dynamically selected carrier corresponds to the band instantaneously occupied by the reference signal. The dynamic selection is executed whereby whenever there is a transition of the reference signal from a first band to a second band, the carriers for the first and second bands are selected dependent on a slope of the reference signal waveform at the transition.

PART TWO

5 LEVEL E-TYPE UNIDIRECTIONAL RECTIFIER

4 INTRODUCTION

4.1 Power Conversion System for Variable Speed Drive Applications

The main attractions in the variable speed drive applications are the weight and size reduction and the increased efficiency with a restricted system costs. In the field of power generation units, in order to avoid the use of gearbox and ensure a higher power density, the interest towards the high-speed gen-set units is increased. In fact, high speed electrical generators are often directly coupled to aircraft turbines to provide, through the controlled three-phase rectifier, power to the on board electrical distribution system (for example power supply to 270V or 540V DC-bus), Fig. 38.

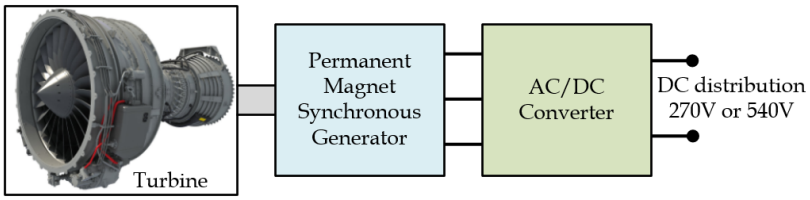


Fig. 38. Circuit diagram of the electrical generation based on DC-bus distribution system.

Future trend in variable speed drive applications is to consider the permanent magnet synchronous generator (PMSG) to be directly as a part of the engine; as a result, very high frequency of the EMF fundamental harmonic is expected. The main advantage of the direct-drive generation systems is the reduction of dimensions and energy dissipation, ensuring, at the same time, easy maintenance and high reliability. Nowadays, the aim is to identify a particular kind of rectifier able to satisfy, in the best way, the requirements of the electrical generation systems. Three-phase AC-DC power converters have been improved in order to provide high efficiency, small size, reliability, high input power factor and low line current distortion. Several types of active and hybrid rectifiers topologies, from the simplest to the most complex, pursue the described tasks [21],[33],[34].

4.2 Multi-level Converter for Variable Speed Drive Applications

In the mentioned applications, the electrical distribution system is usually composed by three elements (as it can be seen from Fig. 38): high-speed turbine, a three-phase PMSG and a rectifier. As previously mentioned, the high-speed generators are used in order to increase the efficiency and reduce the system volume and the maintenance costs. In order to limit the reactive voltage drop given the high fundamental electrical frequency, new technologies and designs within drives have been enabled to reduce the synchronous inductance.

To better explain the concept let's consider the equivalent circuit of the input converter, as shown in Fig. 39. As can be seen from Fig. 39, the *EMF* is the electromotive force, R_0 is the winding stator resistance and L_0 is the leakage stator inductance.

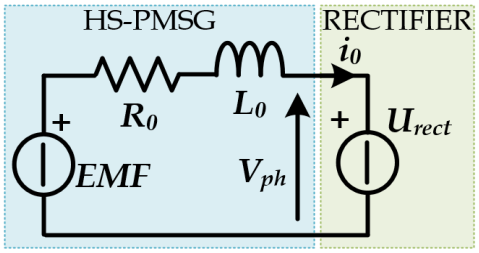


Fig. 39. Equivalent circuit of the input converter.

If the fundamental frequency increases the reactive voltage drop across the inductance L_0 is not negligible; as a consequence, the phase voltage, V_{ph}, supplied by the machine is reduced. For this reason, the aim of the machine design is to reduce the synchronous inductance to limit the reactive voltage drop. On the other hand, having small inductance per phase at the converter side leads to a high current ripple (as can be shown from the equation (1). Increasing of the switching frequency to keep the current ripple within bounds is not an option due to the losses and the devices speed limits. Thus, the multi-level converters have been introduced for variable speed drive applications with high fundamental frequency.

4.3 A Solution: 3Φ5L E-Type Rectifier

The circuit diagram of the three-phase 5-level unidirectional E-Type Rectifier (3Φ5L E-Type Rectifier) is depicted in Fig. 40.

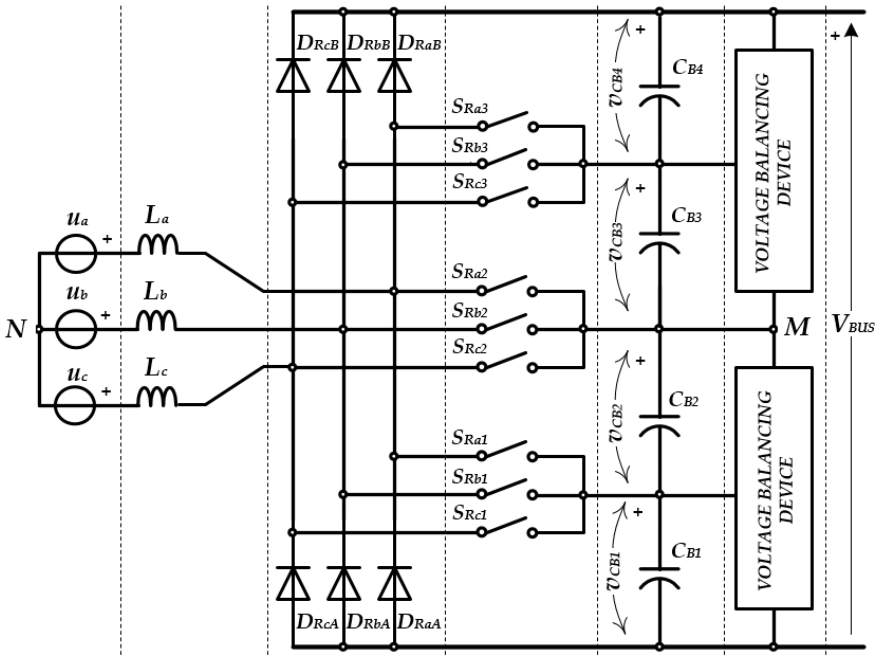


Fig. 40. Circuit diagram of the 3Φ5L E-Type Rectifier.

The 3Φ5L E-Type Rectifier consists of five functional blocks: input filter inductors L_a, L_b and L_c, three phase diode bridge, a set of the IGBTs connected between the diode bridge, the DC-bus capacitors, a set of four series connected DC-bus capacitors C_{B1}, C_{B2}, C_{B3}, C_{B4} and two voltage balancing devices. The power devices are controlled to ensure a sinusoidal waveform of the input current and a regulated DC-bus voltage at the output [39]. As discussed in the previous chapter, two voltage balancing are used in order to obtain four equal voltages among the series capacitors ($v_{CB1}=v_{CB2}=v_{CB3}=v_{CB4}=¼V_{BUS}$).

4.3.1 3Φ5L E-Type Rectifier Characteristics

The generator is a symmetrical three-phase PM generator having the phase-to-neutral voltages as in (7), where V_{IN} is the RMS input voltage.

$$\begin{cases} u_a(\mathrm{t}) = \sqrt{2}V_{IN}\sin\left(\omega_{IN}t\right) \\ u_b(\mathrm{t}) = \sqrt{2}V_{IN}\sin\left(\omega_{IN}t - \frac{2}{3}\pi\right) \\ u_c(\mathrm{t}) = \sqrt{2}V_{IN}\sin\left(\omega_{IN}t - \frac{4}{3}\pi\right) \end{cases} \quad (7)$$

The input current of each phase rectifier can be written as in (8), where I_{IN} is the RMS input current. Since the rectifier is unidirectional, the input phase displacement φ_{IN} must be equal 0, (φ_{IN} =0).

$$\begin{cases} i_a(\mathrm{t}) = \sqrt{2}I_{IN}\sin\left(\omega_{IN}t - \varphi_{IN}\right) \\ i_b(\mathrm{t}) = \sqrt{2}I_{IN}\sin\left(\omega_{IN}t - \frac{2}{3}\pi - \varphi_{IN}\right) \\ i_c(\mathrm{t}) = \sqrt{2}I_{IN}\sin\left(\omega_{IN}t - \frac{4}{3}\pi - \varphi_{IN}\right) \end{cases} \quad (8)$$

The converter modulation depth is given by the equation (9).

$$M_{0,R} = \frac{2\sqrt{2}V_{IN}}{V_{BUS}} \quad (9)$$

Let us assume the DC-bus capacitors large enough for its voltages to remain constant. The DC-bus partial voltages are assumed to be equal as in (10).

$$v_{CB1} = v_{CB2} = v_{CB3} = v_{CB4} = \frac{V_{BUS}}{4} \quad (10)$$

The voltage levels depend on the input-to-neutral switching voltage $u_{P(sw)}$, where $P \in \{a, b, c\}$. On one hand, if the 3Φ5L E-Type Rectifier operates in Continues Conduction Mode (CCM), the input-to-neutral switching voltage u_{Psw} is a function of the DC-bus voltage and the states of the switches [152]. On the other hand, when the 3Φ5L E-Type Rectifier works in Discontinuous Conduction Mode (DCM) the input-to-neutral switching voltage $u_{P(sw)}$ is also a function of the current.

$$S_{RPx} = \begin{cases} 0 & \text{switch off} \\ 1 & \text{switch on} \end{cases} \quad (11)$$

Let's consider that the 5L E-Type Rectifier works in CCM. The switching function S_{RPx}, with $x \in \{1, 2, 3\}$ is defined by (11). The 5L E-Type Rectifier is unidirectional whereby the current in the top-middle leg flows in one direction from AC-side

to DC-side, whereas the current in the bottom-middle leg the current flows in the opposite direction, Fig. 41.

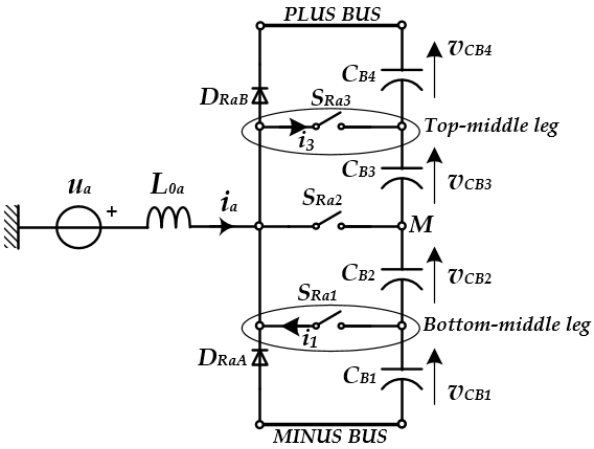


Fig. 41. Single-phase equivalent circuit diagram of the 5L E-Type Rectifier.

Therefore, the current direction in the top-middle and bottom-middle legs can be taken into account considering the threshold function $\theta(i_P)$ as in (12). It follows that $\theta(i_P)+\bar{\theta}(i_P)=1$ and $\theta(i_P)+\bar{\theta}(i_P)= sgn(i_P)$, where $\bar{\theta}(i_P)$ is logic complement of the $\theta(i_P)$.

$$\theta(i_P)=\begin{cases}1 & i_P \geq 0\\ 0 & i_P < 0\end{cases} \tag{12}$$

Thus, the input-to-neutral switching voltage $u_{P(sw)}$ can be derived as in (13), where $u_{BUS,Rh}$ and $u_{BUS,Rl}$ are the top-to-middle (or upper) and middle-to-bottom (lower) DC-bus voltages.

$$u_{P(sw)}=(1-S_{RP2})\left[v_{BUS,Rh}\theta(i_P)-v_{BUS,Rl}\bar{\theta}(i_P)\right] \tag{13}$$

The upper and lower DC-bus voltages can be derived as in (14). It can be noticed how $v_{BUS,Rh}$ and $v_{BUS,Rl}$ take into account the contribution of S_{RP1} and S_{RP3} switches.

$$\begin{aligned} u_{BUS,Rl}&=(1-S_{RP1})(v_{CB1}+v_{CB2})+S_{RP1}v_{CB2}\\ u_{BUS,Rh}&=(1-S_{RP3})(v_{CB3}+v_{CB4})+S_{RP3}v_{CB3}\end{aligned} \tag{14}$$

Substituting (10) and (14) in (13), the input-to-neutral switching voltage $u_{P(sw)}$ can be written as in (15), where S_{RP2} is switching function of the inner switch.

$$u_{P(sw)}=\frac{V_{BUS}}{4}(1-S_{RP2})\left[2sgn(i_P)-S_{RP3}\theta(i_P)+S_{RP1}\bar{\theta}(i_P)\right] \tag{15}$$

As can be seen by equation (15), when the S_{RP2} is "on" the input-to-neutral switching voltage, $u_{P(sw)}$, is clamped to the neutral point of the DC-bus (N).

Table 1. Input-to-neutral switching voltage versus switching function and phase current polarity

State R	i_P	S_{RP1}	S_{RP2}	S_{RP3}	$u_{P(sw)}$
1	+	0	0	0	+ $V_{BUS}/2$
2	+	1	0	0	+ $V_{BUS}/2$
3	+	0	1	0	0
4	+	1	1	0	0
5	+	0	0	1	$V_{BUS}/4$
6	+	1	0	1	$V_{BUS}/4$
7	+	0	1	1	0
8	+	1	1	1	0
9	-	0	0	0	- $V_{BUS}/2$
10	-	1	0	0	- $V_{BUS}/4$
11	-	0	1	0	0
12	-	1	1	0	0
13	-	0	0	1	- $V_{BUS}/2$
14	-	1	0	1	- $V_{BUS}/4$
15	-	0	1	1	0
16	-	1	1	1	0

When the S_{RP2} is "off" the input switching voltage $u_{P(sw)}$ can take one of the 4 values $\pm V_{BUS}/2$, $\pm V_{BUS}/4$ depending on the switching function S_{RP1} and S_{RP3}. To better explain how the voltage levels are produced, Table 1 shows the input-to-neutral switching voltage $u_{P(sw)}$ versus switching function and phase current polarity. Considering the voltage unbalance between the two partial v_{CB1}, v_{CB2} and v_{CB3}, v_{CB4}, the equation (10) can be written as in (16), where Δv_{BUS} is the DC-bus voltage unbalance. Consequently, the equation (15) can be rewritten as in (17).

$$v_{CB1} = v_{CB2} = \frac{V_{BUS}}{4} - \frac{\Delta v_{BUS}}{4},\ v_{CB3} = v_{CB4} = \frac{V_{BUS}}{4} + \frac{\Delta v_{BUS}}{4} \tag{16}$$

$$u_{P(sw)} = \frac{V_{BUS}}{4}\left(1 - S_{RP2}\right)\left[2sgn\left(i_P\right) + 2\Delta v_{BUS} - S_{RP3}\theta\left(i_P\right)\left(1 + \frac{\Delta v_{BUS}}{V_{BUS}}\right) + S_{RP1}\bar{\theta}\left(i_P\right)\left(1 - \frac{\Delta v_{BUS}}{V_{BUS}}\right)\right] \tag{17}$$

4.3.2 Operating Area

The input-to-neutral switching voltage $u_{a(sw)}$ and input phase-to-neutral voltage u_a is illustrated in Fig. 42.

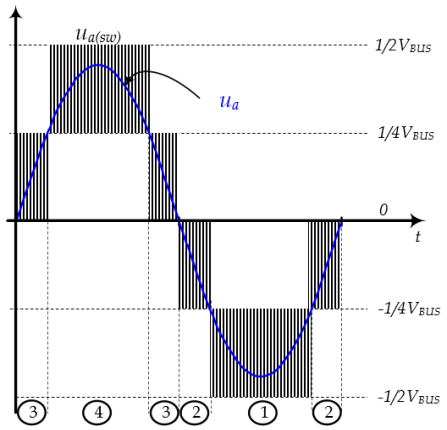
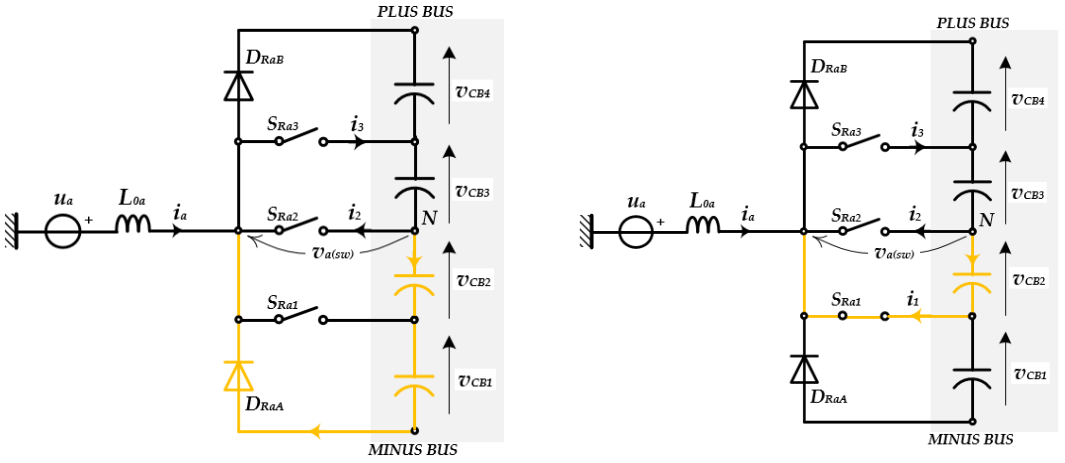
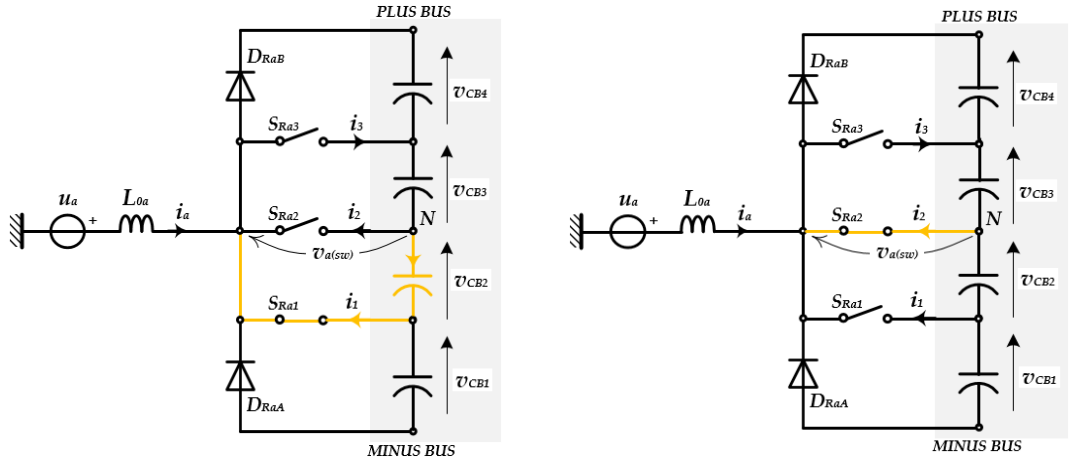


Fig. 42. Input phase-to-neutral voltage and switching voltage.



(a)



(b)

Fig. 43. Circuit diagram of the single-phase 5L E-Type Rectifier: a) area 1; b) area 2.

As it can be seen in Fig. 42, the 5L E-Type Rectifier can operates in four different areas. In area 1, the phase-to-neutral voltages u_a is negative and the input-to-neutral switching voltage $u_{a(sw)}$ can assume two discrete values $-½V_{BUS}$ and $-¼V_{BUS}$ depending on the states of the switches S_{Ra1} and S_{Ra2}, Fig. 43a. The input phase current i_a is negative (the direction is from the DC-side to AC-side). In the area 2, the phase-to-neutral voltages u_a is negative and the input-to-neutral switching voltage $u_{a(sw)}$ can assume two discrete values $-¼V_{BUS}$ and 0 depending on the status of the switches S_{Ra2}, Fig. 43b.

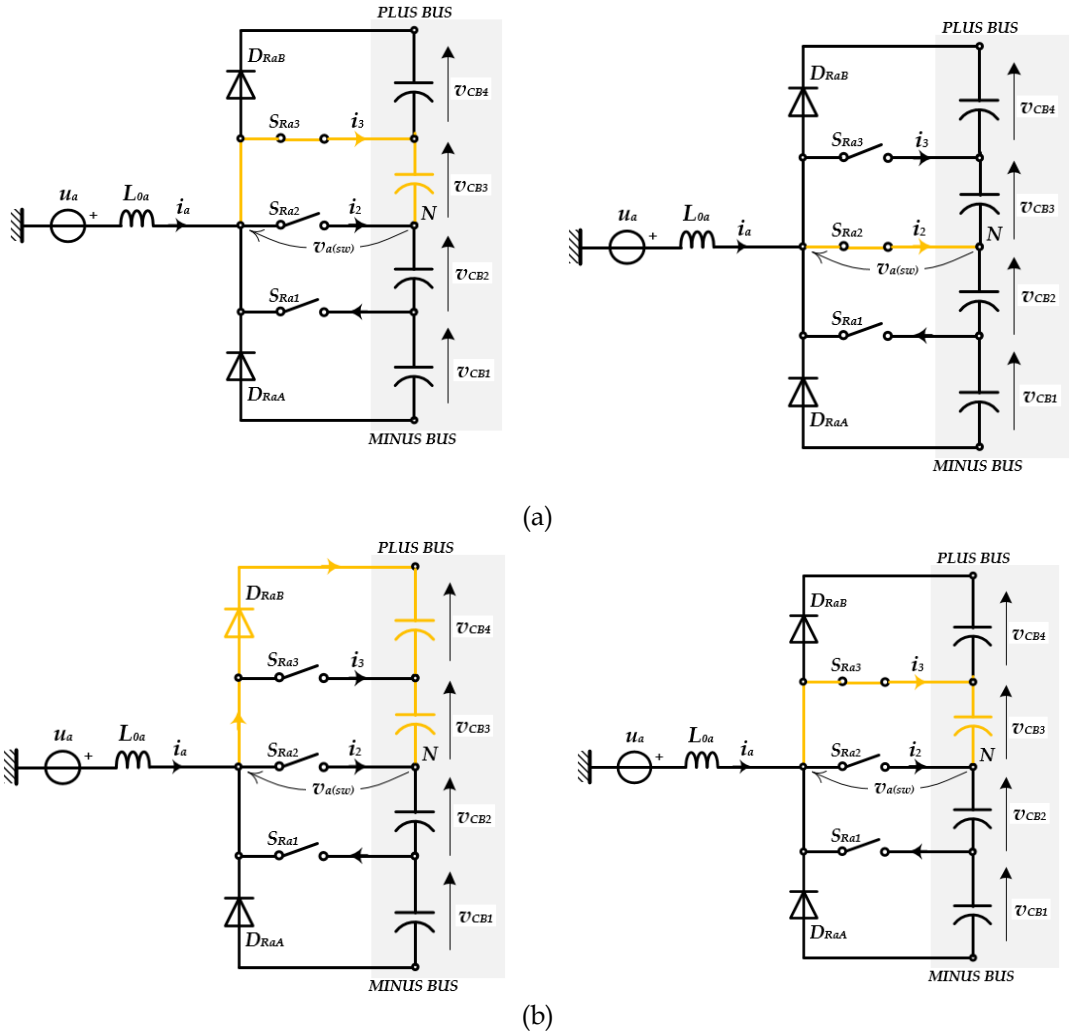


Fig. 44. Circuit diagram of the single-phase 5L E-Type Rectifier: a) area 3; b) area 4.

The input phase current i_a is negative. The phase-to-neutral voltages u_{aN} is positive and the input-to-neutral switching voltage $u_{a(sw)}$ in area 3, Fig. 44a. The input phase current i_a is positive and the input-to-neutral switching voltage can assume two discrete values 0 and $¼V_{BUS}$ depending on the status of the switches

S_{Ra2}. Finally, in area 4 the input phase current i_a is positive and the phase-to-neutral voltages u_a is positive, Fig. 44b. The input-to-neutral switching voltage $u_{a(sw)}$ can assume two discrete values ¼V_{BUS} and ½V_{BUS} depending on the status of the switches S_{Ra2} and S_{Ra3}.

4.4 3Φ5L E-Type Rectifier Performance

Let's consider the circuit of the 3Φ5L E-Type Rectifier in Fig. 45. Part number, voltage rating, current rating, technology and manufacturers of each device are listed in Table 2.

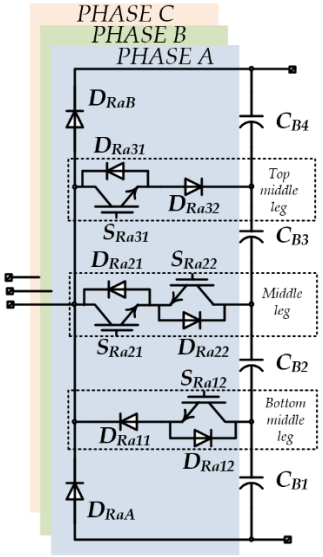


Fig. 45. 3Φ5L E-Type Rectifier Circuit.

The performance of the 3Φ5L E-Type Rectifier have been achieved with reference to the operating parameters shows in Table 3. Each DC-bus capacitor is composed by 3 film capacitors (3x15µF, part number: F611FY15614002, manufacturer: Kemet) and 2 electrolytic capacitors (2x560 µF, part number: EETUQ2V561D, manufacturer: Panasonic) in parallels. In this case, the rectifier is operated at constant DC-bus voltage, variable PMSG rotational speed and constant phase current. Simulation results are performed through PLECS tool in Matlab/Simulink environment. The thermal model of power semiconductors has been created in PLECS environment, producing multi-dimensional lookup tables based on the parameters provided by the manufactures.

Table 2. 3Φ5L E-Type Rectifier Configuration					
Device	**Part Number**	**Rated Voltage [V]**	**Rated Current [A]**	**Technology**	**Manufacturers**
D_{RPA}, D_{RPB}, D_{RP32}, D_{RP11}	IDC08S120	1200 V	60 A	SiC Diode	Infineon
S_{RP12}, S_{RP31}, S_{RP21}, S_{RP22}	IGC16T65U8Q	650 V	50 A	IGBT H5	Infineon
D_{RP12}, D_{RP31}, D_{RP21}, D_{RP22}	IDC08D65Q8	650 V	60 A	Si Diode	Infineon

The rectifier efficiency and losses are depicted in Fig. 46.

Table 3. Operating parameters for PMSG and 3Φ5L E-Type Rectifier.	
Rated mechanical input power [W]	17000
Rated speed [rev/min]	15000
Rated phase EMF [Vrms] @ rated speed	250
Rated phase current [Arms] @ rated torque	22
Fundamental frequency [Hz]	750
Switching frequency [kHz]	12
DC-bus voltage [V]	700
Synchronous inductance [μH]	100

Efficiency and losses results are achieved with switching frequency f_{sw}=12 kHz, junction temperatures T_j=100°C and phase peak current $I_{IN,p}$=30A.

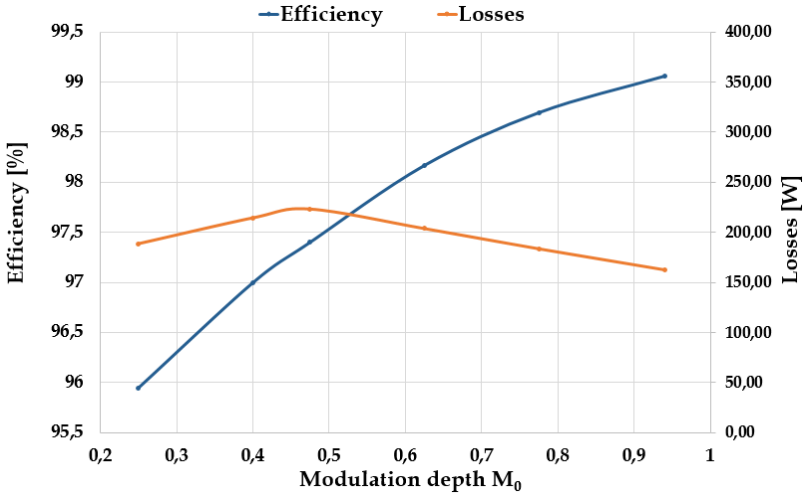


Fig. 46. Efficiency and losses of the 3Φ5L E-Type Rectifier versus modulation depth with fsw=12kHz, T_j=100°C, $I_{IN,p}$=30A.

It can be seen from Fig. 46 that the higher losses occur when the modulation depth $M_{R,0}$ is close to 0.5 because all the power is transferred from the central capacitors to the external capacitors. Meanwhile, the efficiency rectifier shows an increasing trend. The best performance occurs for high values of the modulation

depth. According to the selected DC-bus capacitors, the DC-bus capacitor losses versus modulation depth are shown in Fig. 47.

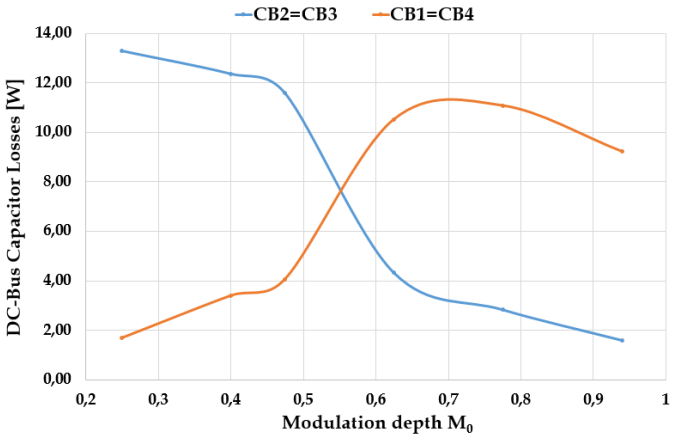


Fig. 47. DC-bus Capacitor losses versus modulation depth.

The capacitors losses have been estimated in PLECS tool in Matlab/Simulink using the equation (18), where R_{ESR} is the equivalent series resistance comes from the datasheet of the selected capacitors and I_{RMS} is the RMS current flow through the capacitors.

$$P_{cap} = R_{ESR} I_{RMS}^2 \tag{18}$$

Losses distribution between the top and the top-middle capacitors is highly dependent on the operating conditions. When the modulation depth $M_{R,0}$ is below 0.5, the power is transferred from the inner capacitors (C_{B2}, C_{B3}) to the external capacitors (C_{B1}, C_{B4}). When modulation depth $M_{R,0}$ is above 0.5, the losses in the external capacitors (C_{B1}, C_{B4}) increase. Fig. 48 shows the normalized power versus modulation depth.

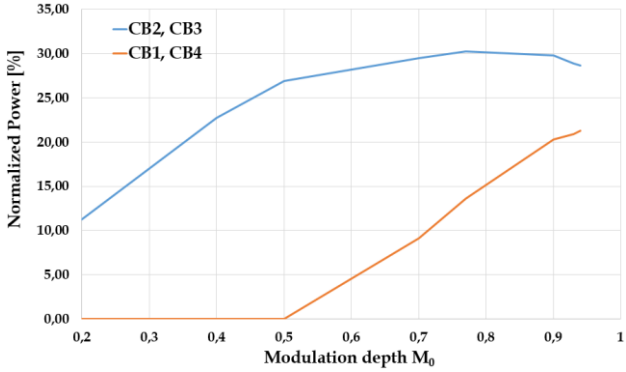


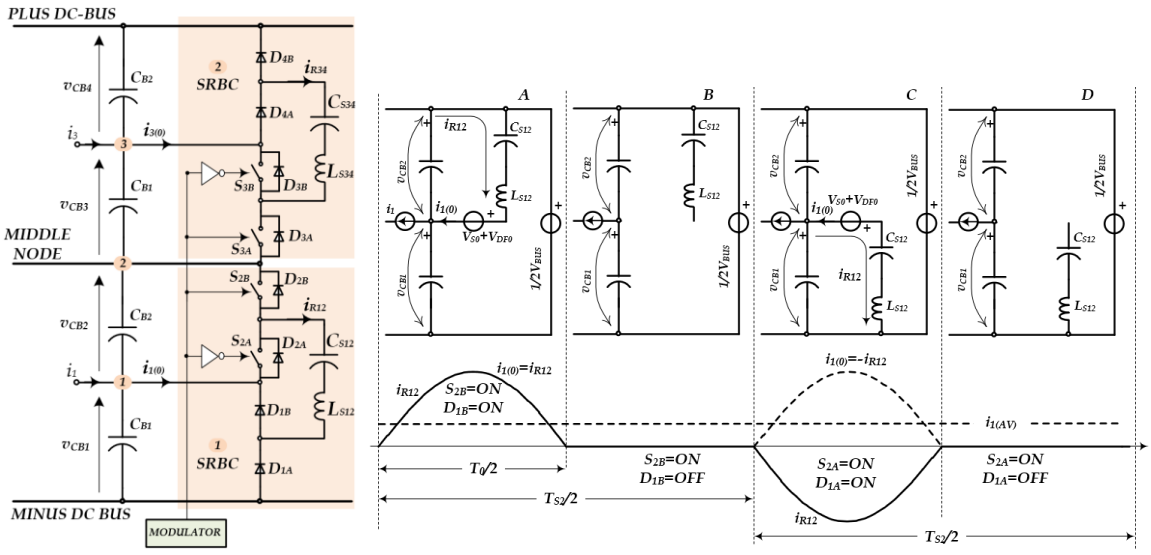
Fig. 48. 3Φ5L E-Type Rectifier Normalized Power versus modulation depth.

The maximum transfer power occurs when the modulation depth is close to 0.5.

Consequently, the power must be transferred from the central capacitors (C_{B2} and C_{B3}) to the external capacitors (C_{B1} and C_{B4}) using a proper additional balancing circuit or a useful control strategy [54]. The carried-out analysis provides a suitable information for improving the design and implementation of the 3Φ5L E-Type Rectifier.

4.5 Analysis of the Series Resonant Balancing Circuit (SRBC)

The circuit diagram of the two-balancing circuit is depicted in Fig. 49a. The balancing converter can be considered as a series resonant converter that operates in DCM, type 1 [63]. The first SRBC, composed by D_{1A}, D_{1B}, S_{2A} and S_{2B}, is connected across the capacitor C_{B1} and C_{B2}. The second SRBC, made up by D_{4A}, D_{4B}, S_{3A} and S_{3B}, is connected across the capacitor C_{B3} and C_{B4}. The capacitor C_{S12} (or C_{S34}) is the main capacitor that transfers energy between the bus capacitors C_{B2} to C_{B1} (or C_{B3} to C_{B4}). The inductor L_{S12} (or L_{S34}) is a resonant inductor used to reduce conduction losses and achieve zero current switching (ZCS) condition, [42]. The switches S_{2A} to S_{2B} (or S_{3A} and S_{3B}) are driven with complementary control signals at period T_{S2} and constant duty cycle (around 50%), see Fig. 49b.



(a) (b)

Fig. 49. a) Series Resonant Balancing Circuit (SRBC) as the DC-bus voltage balancing circuit; b) Basic operation of the SRBC: A) S_{2B}=ON, D_{1B}=ON; B) S_{2B}=ON, D_{1B}=OFF; C) S_{2A}=ON, D_{1A}=ON and D) S_{2A}=ON, D_{1A}=OFF.

Let's assume that v_{CB1} and v_{CB2} are constant over one switching cycle T_{S2} and the power semiconductors are modeled by constant voltage sources V_S and V_{DF}. Each period T_{S2} can be divided into four stages, namely stage A to stage D as shown in Fig. 49b.

Stage A - The switch S_{2B} is closed at the instant t=0. The capacitor C_{S12} is charged from v_{CB2} via the switch S_{2B}, diode D_{1B} and the inductor L_{S12}. The current i_{R12} increases toward the peak. Afterwards, the current starts decreasing towards zero following the resonance of the $L_{S12}C_{S12}$ circuit.

Stage B - The current i_{R12} reaches zero and diode D_{1B} is blocked at the moment $t=T_0/2$. The current remains zero until commutation of the switch S_{2A} is accomplished.

Stage C - The switch S_{2A} is closed at the moment $t=T_{S2}/2$. The capacitor C_{S12} is discharged into v_{CB1} via the switch S_{2A}, diode D_{1A} and the inductor L_{S12}. After reaching the maximum, the current starts decreasing towards zero following the resonance of the $L_{S12}C_{S12}$ circuit.

Stage D - The current i_{R12} reaches zero and diode D_{1A} is blocked at the moment $t=T_{S2}/2+T_0/2$. The current remains zero until the commutation of the switch S_{2B} is accomplished at the moment $t=T_{S2}$. At this point, one switching cycle is completed.

4.5.1 Estimated Losses of the SRBCs

The losses of the SRBCs have been carried-out using PLECS tool in Matlab/Simulink. Starting from the operating condition listed in Table 3 and datasheet provided by the Semikron (Semitop3 SK75GB066T), Fig. 50 illustrates the estimated SRBCs losses.

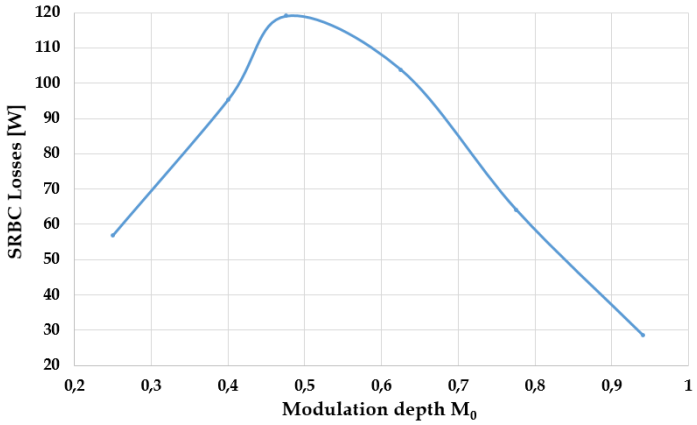
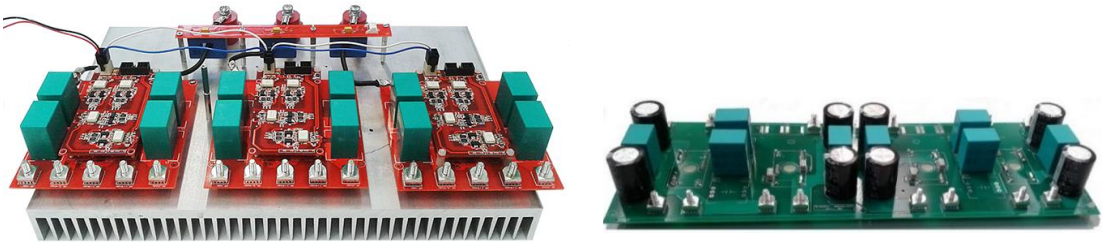


Fig. 50. SRBCs losses versus modulation depth.

It can be noticed that the worst condition occurs when the modulation depth is close to 0.5 due to the asymmetrical AC-to-DC power transfer.

4.1 Hardware Realization

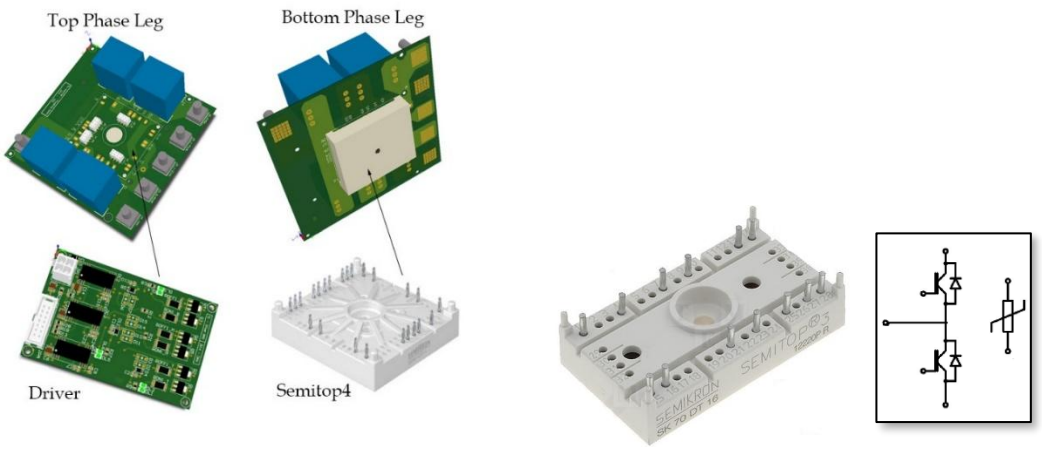
A prototype of the 3Φ5L E-Type Rectifier and the SRBC have been built. Properly designed PCBs have been used for both the rectifier and its balancing circuit in order to reduce the parasitic inductances [39], [40]. Fig. 51 shows the 3Φ5L E-Type Rectifier prototype and the SRBC prototype realization.



(a) (b)

Fig. 51. a) 3Φ5L E-Type Rectifier prototype; b) SRBC prototype.

It is possible to identify, from Fig. 51a, the three-phase leg circuit, the driver circuit, the current and voltage measure sensors and heat-sink. Each single-phase E-Type Rectifier accommodates a Semitop4 module (manufacturer Semikron®) located in the bottom side, the custom driver circuit in the top side and four DC-Bus film capacitors, as shown in Fig. 52a. The Semitop4 module employs the power devices listed in Table 2.



(a) (b)

Fig. 52. a) 3D Model of the Single-phase leg 5L Rectifier and driver circuit; b) Semitop3 SK75GB066T.

The SRBC circuit is instead achieved through the series connection of four Semitop3 SK75GB066T modules, rated 60A-600V (see Fig. 52b) and 4μH and 16μF as resonant total inductance and total capacitance respectively. Additionally, in the SRBC circuit are present one DC-bus film capacitor and two DC-bus electrolytic capacitors.

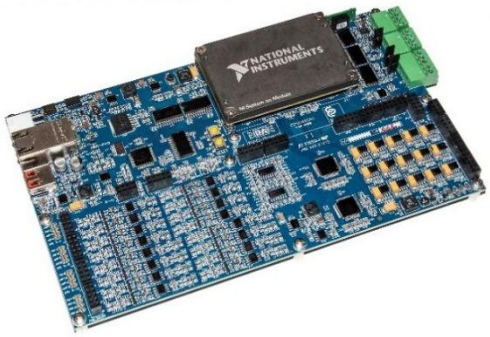


Fig. 53. 3Φ5L E-Type Rectifier Control board (PED-Board for sbRIO-9651); b) adapter for general inverter applications.

The rectifier is controlled by the National Instruments System-on-Module sbRIO-9651 with a dedicated board specifically designed for power electronics and drives applications (PED-Board), as shown in Fig. 53. The control algorithm has been implemented using the National Instruments LabVIEW environment. Being the sbRIO-9651 based on the new Xilinx Zynq-7020, the converter control structure has been closed on the FPGA target [154].

4.2 Modeling and control of the 3Φ5L E-Type Rectifier

The aims of the rectifier control strategy are to regulate both DC-bus voltage and the input sinusoidal current. The block diagram of the 3Φ5L E-Type Rectifier control strategy is depicted in Fig. 54. It can be recognized the field-oriented control structure, which allows to adjust the d-axis and q-axis currents. The DC-bus voltage is regulated by the outer voltage loop. The DC-bus voltage reference V^*_{BUS} is set to the desired operating DC-bus voltage, $i_{d,ref}$ and $i_{q,ref}$ are used to control the PMSG torque and flux, respectively. In order to control the DC-bus variation voltage Δv_{BUS}, a second loop is used.

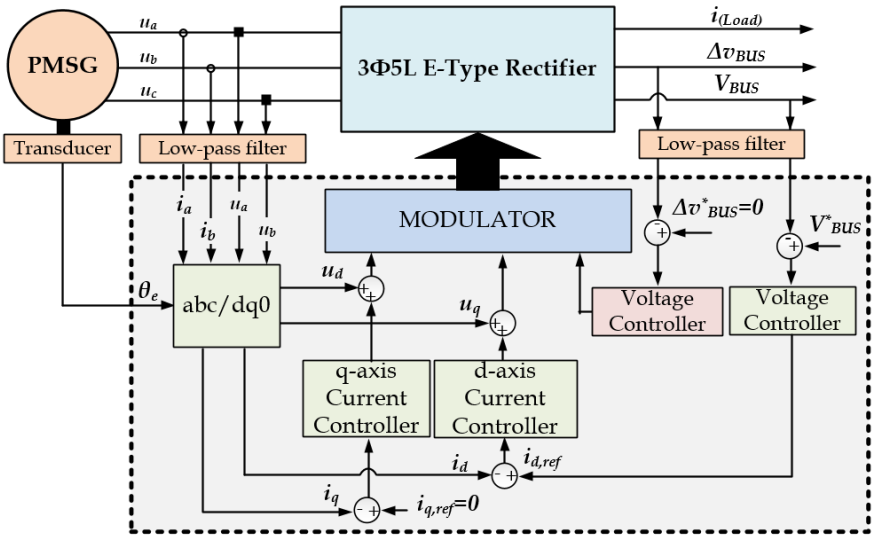


Fig. 54. Block diagram of the 3Φ5L E-Type Rectifier control strategy.

The simplified block diagrams to be used for tuning the voltage control loop are shown in Fig. 55, where it's possible to identify the following transfer functions:

- $G_{vc}(s)$ is the transfer function of the DC-bus voltage controller,
- $G_{cc,d}(s)$ is the transfer function of the d-axis current loop,
- $G_{id}(s)$ is the system transfer function defined as i_d/d_d,
- $G_{vi}(s)$ is the system transfer function defined as V_{BUS}/i_d,
- $G_{lf}(s)$ is the transfer function of the feedback low-pass filter,
- $G_{cc,q}(s)$ is the transfer function of the q-axis current loop,
- $G_{iq}(s)$ is the system transfer function defined as i_q/d_q,
- $G_{\Delta vc}(s)$ is the transfer function of the voltage controller,

- $G_{\Delta vd0}(s)$ is the system transfer function defined as $\Delta v_{BUS}/d_0$.

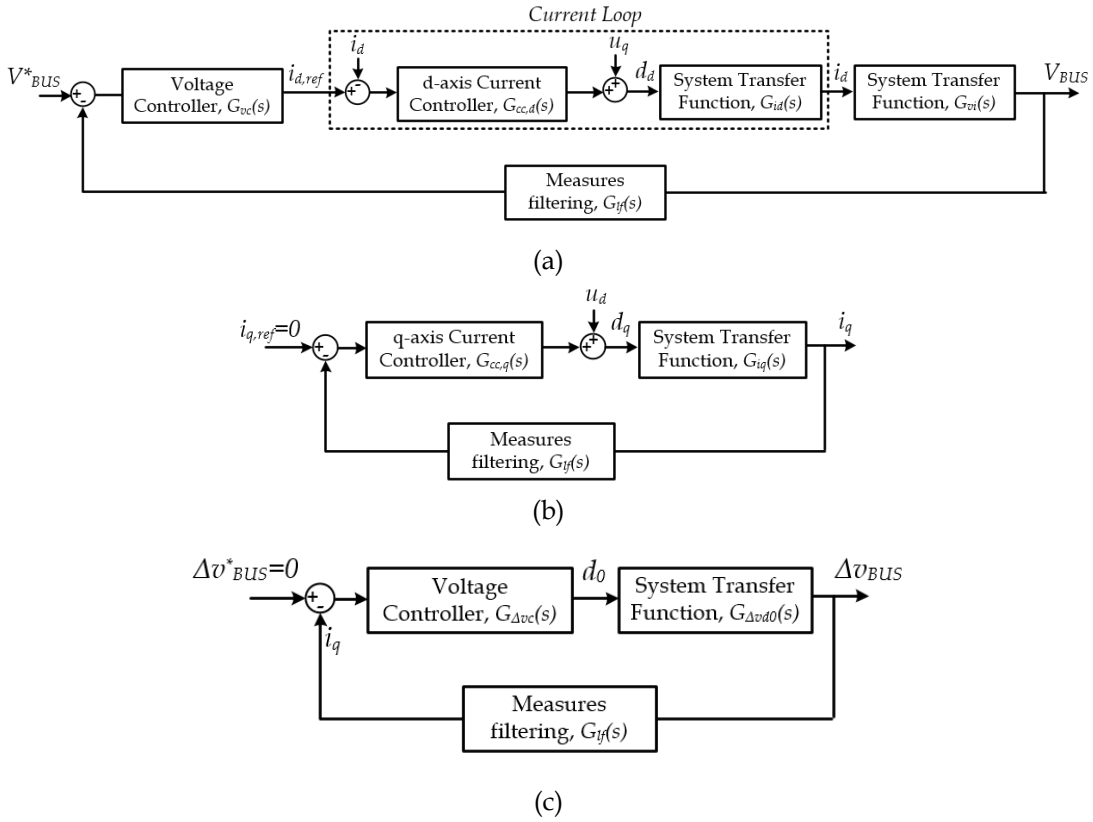


Fig. 55. Simplified control algorithm structure for a generic dq0 axis control: a) d-axis; b) q-axis; c) 0-axis.

In order to understand the dynamic behavior of the 3Φ5L E-Type Rectifier, the large signal and small signal models have been derived. A deepened analysis of the large signal model of 3Φ5L E-Type Rectifier will be discussed in the next section. After that, performing the local linearization around the nominal operating point, the rectifier small signal model will be obtained.

4.2.1 Benefits of the Modeling Approach

The converter topologies normally require control circuits to ensure the best input and output characteristics. Switching converter topologies are highly nonlinear systems due to the presence of power semiconductors. It is difficult to predict their dynamic characteristics due to the nonlinear time-varying nature of the switching converters such as AC-DC and/or DC-AC topologies. The linearization of the power converter behavior is at the basis of a more predictable

tuning procedure of the related control loops. It can be achieved by applying the well-known stability criteria of the linear systems [132], [133]. Consequently, converters control loop design requires the achievement of the system dynamic model (i.e. analytical description). The aim of the power electronic converters modeling is to provide a mathematical expression that contains the information on the steady-state and the dynamic behavior of the system. A low-frequency state-space model of the converter can result by applying the state space averaging method [134]. As consequence, from the large signal average system description, it is very important to develop reliable small-signal models that allow designers to obtain the converter dynamic behaviors reducing the prototyping cost and the design cycle time [135], [136]. The provided small-signal model is at the basis of control loops design, starting from linear control strategies such as PI-based vector control or even more complex model-based control structures. Especially for the latter topologies, the control action performance is directly related to the model representation. Without the small-signal analytical description, except for some specific controllers that do not require any tuning (i.e. hysteretic controllers), the designer cannot take advantage of the well-known control system theory and he is forced to use the so-called trial-and-error approach, which yields unsatisfactory dynamic performance. Moreover, the availability of the linearized system equations results in the possibility to use non-linear and adaptive control structures to strongly improve the complete dynamic response, as it is described in [137]. The methodology used to derive the averaged model is often based on state-space averaging technique. The small signal model based on the large signal model is proposed for the Vienna rectifier [6], [35], [36], [138], [139].

4.2.2 Low-Frequency State-Space Model for 3Φ5L E-Type Rectifier

In order to perform a modal analysis or to build linear control laws, it is necessary to develop linear models around a certain operating point. The average

model of the 3Φ5L E-Type Rectifier is based on the state-space averaging (SSA) technique [152]. This model is valid as long as the converter inputs and state variables change slowly with respect to the switching period. The rectifier average model is mainly based on two separate steps:

1) the equivalent average model equations, which describe the input AC-side and the output DC-side of the converter, are achieved;
2) from the averaging model, initially expressed in *abc* stationary reference, system physical variables are transformed into the dq0 synchronous reference frame.

In order to simplify the *abc* analytical model (nonlinear fifth-order time-varying system), the *abc*-to-*dq0* transformation has been applied (nonlinear fourth-order time-varying system).

4.2.2.1 State-Space Equations

Let's assume an equal DC-bus partial voltage across v_{CB1}, v_{CB2} and v_{CB3}, v_{CB4} as defined in (16), namely the two balancing circuits will be neglected and $\Delta v_{BUS}=(v_{CB3}+v_{CB4})-(v_{CB1}+v_{CB2})$ is the only unbalanced voltage. The rectifier load is modeled through power resistors connected in parallel to each DC-bus capacitor.

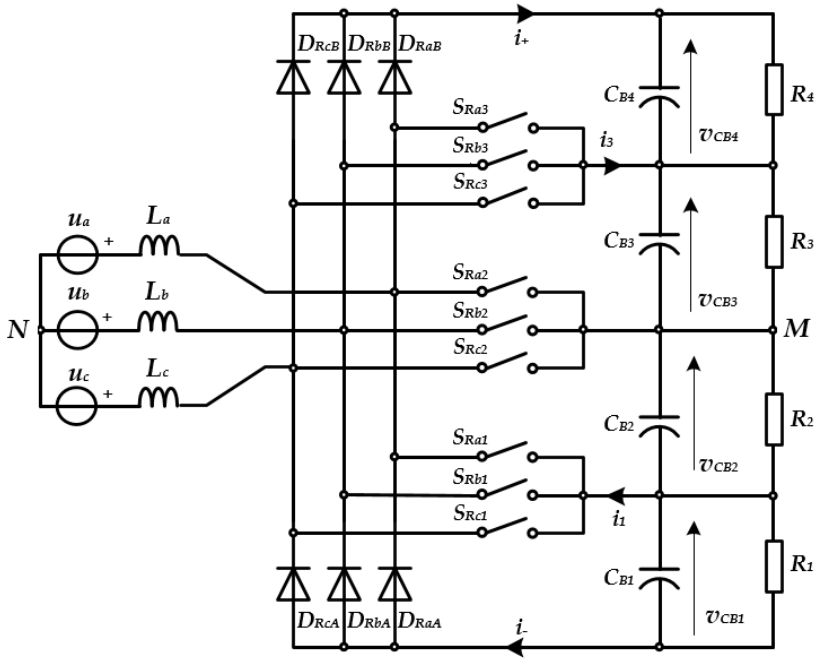


Fig. 56. Complete scheme of the 3Φ5L E-Type Rectifier with the dedicated balancing circuit.

Additionally, the power semiconductors are considered as an ideal switch. A

complete circuit diagram of the 3Φ5L E-Type Rectifier with the is shown in Fig. 56.

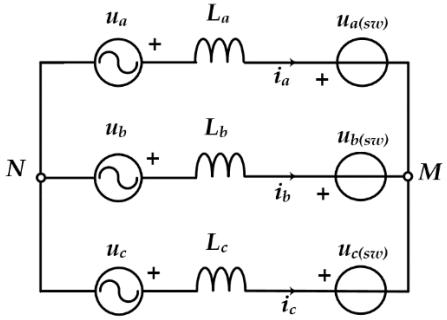


Fig. 57. AC-side three-phase equivalent average circuit for the 3Φ5L E-Type Rectifier.

The AC-side rectifier equivalent average model is depicted in Fig. 57, where u_a, u_b, u_c are the symmetrical three-phase input voltages, and $u_{a(sw)}$, $u_{b(sw)}$, $u_{c(sw)}$ are the input-to-neutral switching voltages. The AC-side of the system can be described by three dependent voltage sources as in (19), where u_{NM} is the middle point voltage related to the main neutral.

$$\begin{aligned} u_a &= L_a \frac{di_a}{dt} + u_{a(sw)} + u_{NM} \\ u_b &= L_b \frac{di_b}{dt} + u_{b(sw)} + u_{NM} \\ u_c &= L_c \frac{di_c}{dt} + u_{c(sw)} + u_{NM} \end{aligned} \tag{19}$$

Assuming L_a=L_b=L_c=L_R and that the three phase input voltages are symmetrical and pure sinewaves, (20) can be straightforwardly defined

$$\begin{aligned} u_a(t) + u_b(t) + u_c(t) = 0 \\ i_a(t) + i_b(t) + i_c(t) = 0 . \end{aligned} \tag{20}$$

Substituting (20) in (19), the middle point voltage can be derived as (21).

$$u_{NM} = -\frac{1}{3}\left(u_{a(sw)} + u_{b(sw)} + u_{c(sw)}\right) \tag{21}$$

Combining the equations (11),(17), (19) and (22), the AC-side state model of the rectifier can be achieved as in (23). Considering Fig. 56, the application of the first Kirchhoff's law to the DC-side nodes of the circuit, yields directly the equations reported in (24), where i_+ and i_- are the currents through respectively plus and minus DC-bus connections.

$$
\begin{cases}
\begin{bmatrix} u_a \\ u_b \\ u_c \end{bmatrix} = L_R \dfrac{d}{dt}\begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} + \boldsymbol{\Gamma}\dfrac{V_{BUS}}{4}\left(2SGN_1 + 2\dfrac{\Delta v_{BUS}}{V_{BUS}}\mathbf{I} - \left(1+\dfrac{\Delta v_{BUS}}{V_{BUS}}\right)\cdot \right. \\
\qquad \left. \cdot SGN_2\begin{bmatrix} S_{Ra3} \\ S_{Rb3} \\ S_{Rc3} \end{bmatrix} + \left(1-\dfrac{\Delta v_{BUS}}{V_{BUS}}\right) SGN_3 \begin{bmatrix} S_{Ra1} \\ S_{Rb1} \\ S_{Rc1} \end{bmatrix}\right)\begin{bmatrix} 1-S_{Ra2} \\ 1-S_{Rb2} \\ 1-S_{Rc2} \end{bmatrix} \\
\Gamma = \begin{bmatrix} 2/3 & -1/3 & -1/3 \\ -1/3 & 2/3 & -1/3 \\ -1/3 & -1/3 & 2/3 \end{bmatrix},\ \mathbf{I} = \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix} \\
SGN_1 = \begin{bmatrix} sgn(i_a) & 0 & 0 \\ 0 & sgn(i_b) & 0 \\ 0 & 0 & sgn(i_c) \end{bmatrix} \\
SGN_2 = \dfrac{1+SGN_1}{2},\ SGN_3 = \dfrac{1-SGN_1}{2}
\end{cases}
\tag{23}
$$

$$
\begin{aligned}
i_+ &= C_{B4}\frac{dv_{CB4}}{dt} + i_{R4} \\
i_- &= C_{B1}\frac{dv_{CB1}}{dt} + i_{R1} \\
C_{B1}\frac{dv_{CB1}}{dt} &= C_{B2}\frac{dv_{CB2}}{dt} - i_1 - i_{R1} + i_{R2} \\
C_{B4}\frac{dv_{CB4}}{dt} &= C_{B3}\frac{dv_{CB3}}{dt} - i_3 + i_{R3} - i_{R4}
\end{aligned}
\tag{24}
$$

Accordingly, i_+ and i_- are given in (25), where i_{RCB}, i_{RBB}, i_{RAB} and i_{RCA}, i_{RBA}, i_{RAA} are the currents through the top and bottom diodes in each phase.

$$
\begin{aligned}
i_+ &= i_{RaB} + i_{RbB} + i_{RcB} \\
i_- &= i_{RaA} + i_{RbA} + i_{RcA}
\end{aligned}
\tag{25}
$$

Diodes current analytical expressions can be derived according to the switching function as in (26), where i_1 and i_3 are respectively the currents through the switches according to the functions S_{RP1} and S_{RP3}.

$$
\begin{aligned}
i_+ &= \sum_{P=a,b,c}(1-S_{RP2})(1-S_{RP3})i_P\theta(i_P) \\
i_- &= \sum_{P=a,b,c}(1-S_{RP2})(1-S_{RP1})i_P\bar{\theta}(i_P) \\
i_1 &= \sum_{P=a,b,c}(1-S_{RP2})S_{RP1}i_P\bar{\theta}(i_P) \\
i_3 &= \sum_{P=a,b,c}(1-S_{RP2})S_{RP3}i_P\theta(i_P)
\end{aligned}
\tag{26}
$$

Substituting (26) into (24) and considering the voltage across the DC-bus

capacitors as state variables, the DC-side state equations are the following

$$\begin{aligned} C\frac{dV_{BUS}}{dt} &= C_{B4}\frac{dv_{CB4}}{dt}+C_{B3}\frac{dv_{CB3}}{dt}+C_{B2}\frac{dv_{CB2}}{dt}+C_{B1}\frac{dv_{CB1}}{dt}= \\ &= \sum_{P=a,b,c}(1-S_{RP2})|i_P|\left[2-S_{RP3}\theta(i_P)-S_{RP1}\bar{\theta}(i_P)\right]\mathrm{sgn}(i_P)- \\ &\quad -i_{R1}-i_{R2}-i_{R3}-i_{R4} \\ C\frac{d\Delta v_{BUS}}{dt} &= C_{B4}\frac{dv_{CB4}}{dt}+C_{B3}\frac{dv_{CB3}}{dt}-C_{B2}\frac{dv_{CB2}}{dt}-C_{B1}\frac{dv_{CB1}}{dt}= \\ &= \sum_{P=a,b,c}(1-S_{RP2})|i_P|\left[2-S_{RP3}\theta(i_P)-S_{RP1}\bar{\theta}(i_P)\right]+ \\ &\quad +i_{R1}+i_{R2}-i_{R3}-i_{R4} \end{aligned} \tag{27}$$

4.2.2.2 State-space Average Model

The modeling approach applied to the 3Φ5L E-Type Rectifier is based on the state-space averaging (SSA) technique [131], [142]. This mathematical approach was introduced so far in the electrical circuit analysis in [143], [144], [145]. Nowadays, it is a consolidated technique used to describe time-varying circuits as power electronics converters [146], [147], [148]. Being the SSA very simple to be implemented on computers thanks to its inherent matrix representation, it has been used to highlight the behaviors of complex system drastically reducing the simulation time [150], [151], [152]. In this method, all the variables are averaged across one PWM sampling period T_S, as it is shown in (28).

$$\langle x(\mathrm{t})\rangle_{T_s}=\frac{1}{T_s}\int_{t-T_s}^{t}x(\tau)\,\mathrm{d}\tau \tag{28}$$

Applying the average operator (28) to the equations (23), the converter AC-side equivalent model is summarized in (29), where d_{RP1}, d_{RP2}, d_{RP3} are the switch duty cycle related to the switches 1, 2, and 3 of the phase P (P$\in\{a,b,c\}$).

$$\begin{cases} \begin{bmatrix} u_a \\ u_b \\ u_c \end{bmatrix} = L_R\frac{d}{dt}\begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix}+\boldsymbol{\Gamma}\frac{V_{BUS}}{4}\left(2SGN_1+2\frac{\Delta v_{BUS}}{V_{BUS}}\mathbf{I}-\left(1+\frac{\Delta v_{BUS}}{V_{BUS}}\right)\cdot\right. \\ \left.\cdot SGN_2\begin{bmatrix} d_{Ra3} \\ d_{Rb3} \\ d_{Rc3} \end{bmatrix}+\left(1-\frac{\Delta v_{BUS}}{V_{BUS}}\right)SGN_3\begin{bmatrix} d_{Ra1} \\ d_{Rb1} \\ d_{Rc1} \end{bmatrix}\right)\begin{bmatrix} 1-d_{Ra2} \\ 1-d_{Rb2} \\ 1-d_{Rc2} \end{bmatrix} \end{cases} \tag{29}$$

The equations (29) are related to the time-varying model that depends also on the sign of the input line currents. In order to overcome this drawback, the

following input transformation is proposed:

$$d'_{RP} = (1 - d_{RP2})\left[2\,\mathrm{sgn}(i_P) + 2\frac{\Delta v_{BUS}}{V_{BUS}} + \left(1 - \frac{\Delta v_{BUS}}{V_{BUS}}\right) d_{RP1}\bar{\theta}(i_P) + \right.$$
$$\left. - \left(1 + \frac{\Delta v_{BUS}}{V_{BUS}}\right) d_{RP3}\theta(i_P) \right], \tag{30}$$

where $\boldsymbol{d'_{RP}}=[d'_{Ra}, d'_{Rb}, d'_{Rc}]$ is the new control vector related to the complete three-phase system representation. Substituting (30) into (29), a compact matrix representation can be written as in (31), where $\boldsymbol{u_P}=[u_a, u_b, u_c]^T$ is the input voltage vector, $\boldsymbol{i_P}=[i_a, i_b, i_c]^T$ is the input current vector and $\boldsymbol{d'_{RP}}=[d'_{Ra}, d'_{Rb}, d'_{Rc}]^T$ the control vector.

$$L_R \frac{d\mathbf{i_P}}{dt} = \mathbf{v_P} - \frac{V_{BUS}}{4}\boldsymbol{\Gamma}\mathbf{d'_{RP}} \tag{31}$$

Applying the average operator (28) to the equations (27), the DC-side equivalent average model is given in (32).

$$\begin{cases} C\dfrac{dV_{BUS}}{dt} = \displaystyle\sum_{P=a,b,c} d'_{RP}|i_P|\left(1 - \frac{\Delta v_{BUS}}{V_{BUS}}\mathrm{sgn}(i_P)\right) - i_{R1} + \\ \qquad - i_{R2} - i_{R3} - i_{R4} \\ C\dfrac{d\Delta v_{BUS}}{dt} = \displaystyle\sum_{P=a,b,c} d'_{RP}|i_P|\left(\mathrm{sgn}(i_P) - \frac{\Delta v_{BUS}}{V_{BUS}}\right) + i_{R1} + \\ \qquad + i_{R2} - i_{R3} - i_{R4} \end{cases} \tag{32}$$

Equations (31) and (32) represent the basic low frequency model of the converter in the stationary frame. The input equation (31) is time-invariant whereas the output expression (32) is time dependent. In fact, (32) still depends on the sign of the input currents that depend by the time evolution of the current. To overcome this drawback, it seems more convenient to average all variables across the AC inputs fundamental period T_0 (instead of T_s), jointly with the usage of the Park's transformation that is rewritten in (33).

$$\mathbf{K} = \frac{2}{3}\begin{bmatrix} \sin(\omega_{IN}\,t) & \sin(\omega_{IN}\,t - 2\pi/3) & \sin(\omega_{IN}\,t - 4\pi/3) \\ \cos(\omega_{IN}\,t) & \cos(\omega_{IN}\,t - 2\pi/3) & \cos(\omega_{IN}\,t - 4\pi/3) \\ 3/2 & 3/2 & 3/2 \end{bmatrix} \tag{33}$$

Applying Park's transformation at the equation (31) and (32), and performing some algebraic manipulation, the *dq0*-axis state-space average model for the 3Φ5L E-Type Rectifier can be written in (34), where α is a constant parameter equals to $2/\pi$ [152]. Equations (34) represent a fourth-order non-linear dynamic system, having i_d, i_q, v_{BUS}, Δv_{BUS} as state variables; d'_{Rd}, d'_{Rq} and d'_{R0} as control inputs; and finally, v_d and v_q as disturbance inputs.

$$\begin{cases} L_R \dfrac{di_d}{dt} = u_d + L_R \omega_{IN} i_q - \dfrac{V_{BUS}}{4} d'_{Rd} \\ L_R \dfrac{di_q}{dt} = u_q - L_R \omega_{IN} i_d - \dfrac{V_{BUS}}{4} d'_{Rq} \\ C \dfrac{dV_{BUS}}{dt} = \dfrac{3}{2}\left(d'_{Rd} i_d + d'_{Rq} i_q\right) - \alpha \dfrac{\Delta v_{BUS}}{v_{BUS}} d'_{R0} i_d + \\ \qquad - i_{R1} - i_{R2} - i_{R3} - i_{R4} \\ C \dfrac{d\Delta v_{BUS}}{dt} = -\dfrac{3}{2} \dfrac{\Delta v_{BUS}}{V_{BUS}}\left(d'_{Rd} i_d + d'_{Rq} i_q\right) + \alpha d'_0 i_d + \\ \qquad + i_{R1} + i_{R2} - i_{R3} - i_{R4} \end{cases} \tag{34}$$

The corresponding equivalent circuit model is shown in Fig. 58, where $i_1=3/2d'_{Rd}i_d$, $i_2=3/2d'_{Rq}i_q$, $i_3=\alpha(\Delta v_{BUS}/v_{BUS})d'_{R0}i_d$, $i'_1=\alpha d'_{R0}i_d$, $i'_2=3/2(\Delta v_{BUS}/V_{BUS})d'_{Rq}i_d$, $i'_3=3/2(\Delta v_{BUS}/V_{BUS})d'_{Rq}i_q$.

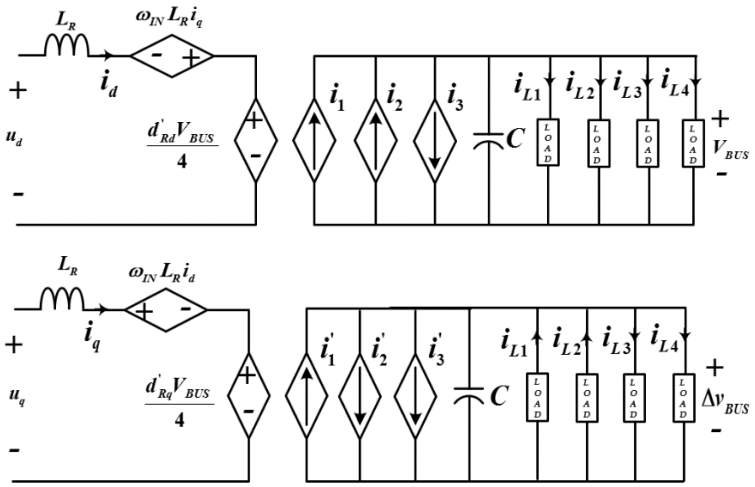


Fig. 58. Complete dq-axis state-space average model for the 3Φ5L E-Type Rectifier.

4.2.2.3 Steady-state operating condition

Let's assume the balanced three-phase input voltages (35), the unity power factor (36) and the balanced DC-bus capacitors voltage (37), where V_{IN} is the

RMS value of the supply voltages, I^*_{IN} is the reference value for the RMS AC line currents and V^*_{BUS} is the reference value for the total DC output voltage.

$$\begin{cases} u_a(\mathrm{t}) = \sqrt{2}\,\mathrm{V}_{IN}\sin(\omega_{IN}\,\mathrm{t}) \\ u_b(\mathrm{t}) = \sqrt{2}\,\mathrm{V}_{IN}\sin(\omega_{IN}\,\mathrm{t} - 2\pi/3) \\ u_c(\mathrm{t}) = \sqrt{2}\,\mathrm{V}_{IN}\sin(\omega_{IN}\,\mathrm{t} - 4\pi/3) \end{cases} \tag{35}$$

$$\begin{cases} i_a(\mathrm{t}) = \sqrt{2}I^*_{IN}\sin(\omega_{IN}\,\mathrm{t}) \\ i_b(\mathrm{t}) = \sqrt{2}I^*_{IN}\sin(\omega_{IN}\,\mathrm{t} - 2\pi/3) \\ i_c(\mathrm{t}) = \sqrt{2}I^*_{IN}\sin(\omega_{IN}\,\mathrm{t} - 4\pi/3) \end{cases} \tag{36}$$

$$\begin{aligned} & v_{CB1} = v_{CB2} = v_{CB3} = v_{CB4} = \frac{V^*_{BUS}}{4} \\ & \Delta v^*_{BUS} = 0 \end{aligned} \tag{37}$$

Applying Park's transformation to the voltage and current expressions (35) and (36), time invariant vectors expressed in the rotating frame are as in (38).

$$\begin{bmatrix} u_d \\ u_q \\ u_0 \end{bmatrix} = \begin{bmatrix} \sqrt{2}V_{IN} \\ 0 \\ 0 \end{bmatrix} \text{ and } \begin{bmatrix} i_d \\ i_q \\ i_0 \end{bmatrix} = \begin{bmatrix} \sqrt{2}I^*_{IN} \\ 0 \\ 0 \end{bmatrix} \tag{38}$$

Substituting expressions (37) and (38) back into (34), the non-linear averaged model is first linearized around the static operating point. This leads to the following expressions for the control inputs

$$\begin{aligned} d'^*_{Rd} &= \frac{4\sqrt{2}V_{IN}}{V^*_{BUS}} \\ d'^*_{Rq} &= -\frac{4L_R\omega_{IN}\sqrt{2}I^*_{IN}}{V^*_{BUS}} \\ d'^*_{R0} &= \frac{\left(i^*_{R4} + i^*_{R3}\right) - \left(i^*_{R1} + i^*_{R2}\right)}{\alpha\sqrt{2}I^*_{IN}} \end{aligned} \tag{39}$$

The steady-state values of the control input depend respectively on the input and output voltages, the input currents and the load. Assuming a balanced purely resistive DC load, it can be written

$$i_{R1} = \frac{V_{BUS} - \Delta v_{BUS}}{4R};\quad i_{R2} = \frac{V_{BUS} - \Delta v_{BUS}}{4R};\quad i_{R3} = \frac{V_{BUS} + \Delta v_{BUS}}{4R};\quad i_{R4} = \frac{V_{BUS} + \Delta v_{BUS}}{4R}$$

with $R_{R1}=R_{R2}=R_{R3}=R_{R4}=R$. The considered load resistors can be achieved by $R=V^2_{BUS}/4P_{nom}$, being P_{nom} the whole DC-bus load power.

4.2.2.4 Large Signals Model Simulation Results

The large signals model of the 3Φ5L E-Type Rectifier has been verified through numerical results. A proper implementation of both the average model and the full-rectifier switching model have been realized in the Matlab/Simulink environment. Achieved equations have been used to deploy the model that is summarized as the block scheme shown in Fig. 59, where *K* is the *abc*-to-*dq0* transformation matrix as defined in (33). The implemented average model can be executed in the discrete time domain, further speeding up the simulation time.

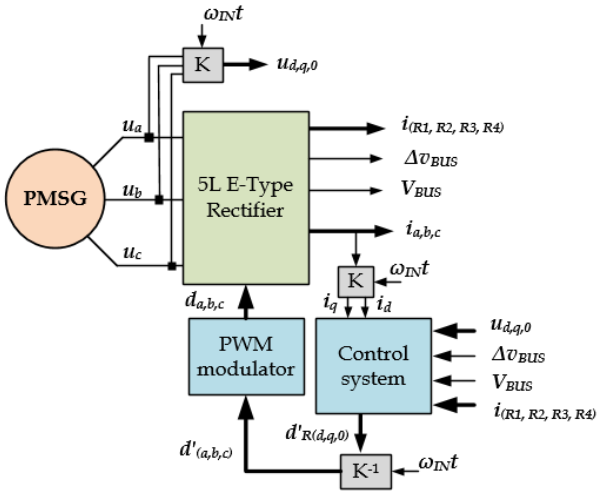
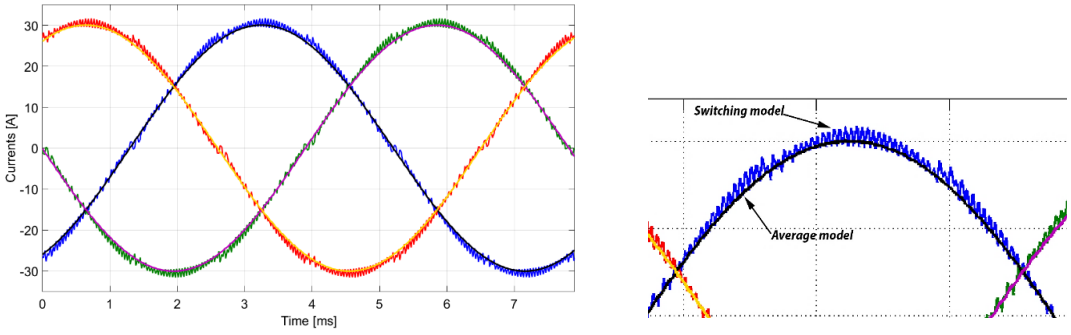


Fig. 59. Block scheme of the implemented average model.

The simulations results have been performed with reference to the operating condition listed in Table 3. Output load is modeled as a pure resistor.



(a) (b)

Fig. 60. a) AC-DC input phase currents for the average model and the switching model; b) Zoomed phase currents.

Fig. 60a shows the line currents of the switching model with superimposed the ones obtained from the average model for the same operating conditions. A

zoom of Fig. 60a is reported in Fig. 60b to better highlight the matching between average and switching models. Simulation results exhibit a good matching with the proposed average model. Fig. 61 shows the line-to-line voltages of the discrete-time average model and of the switching model when the modulation depth $M_{R,0}$ is around 0.95. In this condition, the PM machine speed is set at 3500rpm and the phase peak current is still set at 30A. Depicted line-to-line voltages that result from the switching model clearly exhibit the five levels. As a comparison, line-to-line voltages from the discrete average model are superimposed.

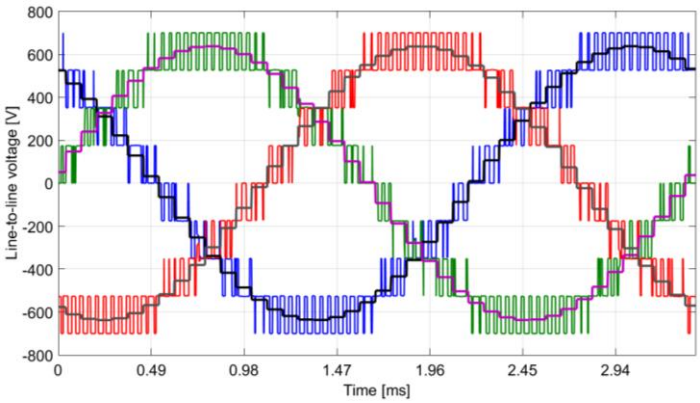
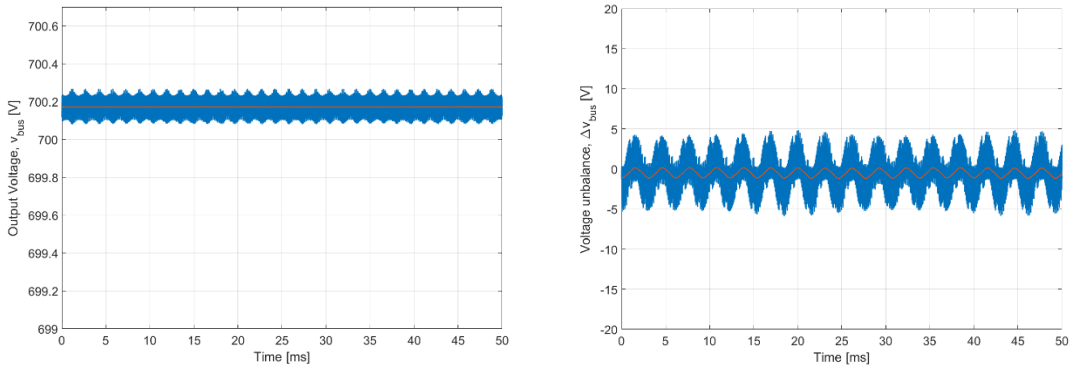


Fig. 61. Line-to-line voltages of the discrete-time average model and of the switching model at modulation index close to 0.9.

In Fig. 62a and Fig. 62b are depicted respectively the DC-bus voltage and the DC-bus voltage unbalance, V_{BUS} and Δv_{BUS}, for the average model and the switching model.



(a) (b)

Fig. 62. a) DC-bus voltage V_{BUS} for the average model (red-line) and the switching model (blue-line); b) Δv_{BUS} voltage for the average model (red-line) and the switching model(blue-line).

The proposed model is able to describe the average behavior of the rectifier physical characteristics.

4.2.3 Small-Signal Model

The small-signal linearization system consists of representing each time variable as the sum of two terms, its desired steady-state value (DC) and a first order time-varying signal (AC), neglecting higher order variations. The AC signal represents the assumed small variation of the variable nearby its steady state DC value. In order to establish the small-signal dynamic model, the equations (34) are analytically linearized around the DC operating point defined in (39). Accordingly, the linear state equations can be written in a compact matrix form as in (40), where $\tilde{x}(\mathrm{t}) = \left[\tilde{i}_d(\mathrm{t}), \tilde{i}_q(\mathrm{t}), \tilde{v}_{BUS}(\mathrm{t}), \Delta\tilde{v}_{BUS}(\mathrm{t})\right]^T$ is the state vector, $\tilde{d}(\mathrm{t}) = \left[\tilde{d}'_{Rd}(\mathrm{t})\ \tilde{d}'_{Rq}(\mathrm{t})\ \tilde{d}'_{R0}(\mathrm{t})\right]^T$ is the control or input vector, and $\tilde{u}(\mathrm{t}) = \left[\tilde{u}_d(\mathrm{t})\ \tilde{u}_q(\mathrm{t})\right]^T$ is the disturbance vector.

$$\dot{\tilde{x}}(\mathrm{t}) = \mathbf{A}\tilde{x}(\mathrm{t}) + \mathbf{B}\tilde{d}(\mathrm{t}) + \mathbf{E}\tilde{u}(\mathrm{t}) \tag{40}$$

The state matrix *A*, the control matrix *B*, the disturbance matrix *E* are defined as in (41), where the nonlinear function *f* describes the system as in (34) and x_0 is the selected operating point. The application to (34) of the partial differentiation, as defined in (40), leads to the expressions (42).

$$A = \left.\frac{\partial f}{\partial x_{\sim}}\right|_{x=x_0}, \quad B = \left.\frac{\partial f}{\partial d_{\sim}}\right|_{x=x_0}, \quad E = \left.\frac{\partial f}{\partial u_{\sim}}\right|_{x=x_0} \tag{41}$$

Applying the Laplace's transform to the state equations (40), the well-known frequency-domain representation of the converter is obtained as in (43), where *I* denote the 4x4 identity matrix and $\tilde{X}(s)$, $\tilde{D}(s)$, $\tilde{U}(s)$ are respectively the Laplace' transforms of vectors $\tilde{x}(t)$, $\tilde{d}(t)$, $\tilde{u}(t)$.

$$A=\begin{pmatrix} 0 & \omega_0 & -\dfrac{\sqrt{2}V_{IN}}{LV^*_{BUS}} & 0 \\ -\omega_0 & 0 & \dfrac{\omega_0\sqrt{2}I^*_{IN}}{V^*_{BUS}} & 0 \\ \dfrac{6\sqrt{2}V_{IN}}{CV^*_{BUS}} & -\dfrac{6L_R\omega_{IN}\sqrt{2}I^*_{IN}}{CV^*_{BUS}} & -\dfrac{1}{RC} & 0 \\ 0 & 0 & 0 & -\dfrac{12V_{IN}I^*_{IN}}{CV^{*2}_{BUS}}-\dfrac{1}{RC} \end{pmatrix}, \quad (42)$$

$$B=\begin{pmatrix} -\dfrac{V^*_{BUS}}{4L_R} & 0 & 0 \\ 0 & -\dfrac{V^*_{BUS}}{4L_R} & 0 \\ \dfrac{3\sqrt{2}I^*_{IN}}{2C} & 0 & 0 \\ 0 & 0 & \dfrac{\alpha\sqrt{2}I^*_{IN}}{C} \end{pmatrix}, \quad E=\begin{pmatrix} \dfrac{1}{L_R} & 0 \\ 0 & \dfrac{1}{L_R} \\ 0 & 0 \\ 0 & 0 \end{pmatrix}$$

$$\tilde{X}(s)=(sI-\mathbf{A})^{-1}\mathbf{B}\tilde{D}(s)+(sI-\mathbf{A})^{-1}\mathbf{E}\tilde{U}(s) \quad (43)$$

Substituting (42) into (43) and performing some algebraic manipulations, a compact matrix representation can be written as in (44).

$$\begin{bmatrix} \tilde{i}_d(s) \\ \tilde{i}_q(s) \\ \tilde{v}_{BUS}(s) \\ \Delta\tilde{v}_{BUS}(s) \end{bmatrix}=\begin{pmatrix} G_{id11} & G_{id12} & G_{id13} \\ G_{id21} & G_{id22} & G_{id23} \\ G_{vd11} & G_{vd12} & G_{vd13} \\ G_{\Delta vd11} & G_{\Delta vd12} & G_{\Delta vd13} \end{pmatrix}\begin{bmatrix} \tilde{d}'_{Rd}(s) \\ \tilde{d}'_{Rq}(s) \\ \tilde{d}'_{R0}(s) \end{bmatrix}+\begin{pmatrix} G_{iu11} & G_{iu12} \\ G_{iu21} & G_{iu22} \\ G_{vu11} & G_{vu12} \\ G_{\Delta vu11} & G_{\Delta vu12} \end{pmatrix}\begin{bmatrix} \tilde{u}_d(s) \\ \tilde{u}_q(s) \end{bmatrix} \quad (44)$$

Result of (44) represents the small signal model of the 3Φ5L E-Type Rectifier. It can be noticed that the system is described by twenty transfer functions, relating the five inputs $\{\tilde{d}'_{Rd}\ \tilde{d}'_{Rq}\ \tilde{d}'_{R0}\ \tilde{u}_d\ \tilde{u}_q\}$ to the four outputs $\{\tilde{\imath}_d\ \tilde{\imath}_q\ \tilde{v}_{BUS}\ \Delta\tilde{v}_{BUS}\}$. The used notation is in the form $G_{xyzt}(s)$, where x is an output coming from the vector $\tilde{X}(s)$, y is an input being an element of either $\tilde{D}(s)$ or $\tilde{U}(s)$, z is the rank of the output x in the vector $\tilde{X}(s)$ and t is the rank of the input y in the vector $\tilde{D}(s)$ or $\tilde{U}(s)$. The expressions of the transfer functions are summarized in Table 4 and Table 5.

Table 4. 3Φ5L E-Type Rectifier Transfer Functions

$G_{id11}=\frac{\tilde{\hat{i}}_d}{\tilde{\hat{d}}'_{Rd}}=-\frac{V^*_{BUS}}{4L_R}\frac{s^2+\beta_{11}s}{s^3+\tau s^2+\left(\omega^2_{IN}\beta_{12}+\beta_{13}\right)s+\tau\omega^2_{IN}}$,
$G_{id12}=\frac{\tilde{\hat{i}}_d}{\tilde{\hat{d}}'_{Rq}}=-\frac{V^*_{BUS}\omega_{IN}}{4L_R}\frac{s+\beta_{11}}{s^3+\tau s^2+\left(\omega^2_{IN}\beta_{12}+\beta_{13}\right)s+\tau\omega^2_{IN}}$,
$G_{id13}=\frac{\tilde{\hat{i}}_d}{\tilde{\hat{d}}'_{R0}}=0,$
$G_{id21}=\frac{\tilde{\hat{i}}_q}{\tilde{\hat{d}}'_{Rd}}=\frac{V^*_{BUS}\omega_{IN}}{4L_R}\frac{\beta_{12}s+\tau}{s^3+\tau s^2+\left(\omega^2_{IN}\beta_{12}+\beta_{13}\right)s+\tau\omega^2_{IN}}$,
$G_{id22}=\frac{\tilde{\hat{i}}_q}{\tilde{\hat{d}}'_{Rq}}=-\frac{V^*_{BUS}}{4L_R}\frac{s^2+\tau s+\beta_{13}}{s^3+\tau s^2+\left(\omega^2_{IN}\beta_{12}+\beta_{13}\right)s+\tau\omega^2_{IN}}$,
$G_{id23}=\frac{\tilde{\hat{i}}_q}{\tilde{\hat{d}}'_{R0}}=0,$
$G_{vd11}=\frac{\tilde{v}_{BUS}}{\tilde{\hat{d}}'_{Rd}}=\frac{3\sqrt{2}I^*_{IN}}{2C}\frac{s^2+\beta_{14}s}{s^3+\tau s^2+\left(\omega^2_{IN}\beta_{12}+\beta_{13}\right)s+\tau\omega^2_{IN}}$,
$G_{vd12}=\frac{\tilde{v}_{BUS}}{\tilde{\hat{d}}'_{Rq}}=\frac{3\sqrt{2}I^*_{IN}\omega_{IN}}{2C}\frac{s+\beta_{14}}{s^3+\tau s^2+\left(\omega^2_{IN}\beta_{12}+\beta_{13}\right)s+\tau\omega^2_{IN}}$,
$G_{vd13}=\frac{\tilde{v}_{BUS}}{\tilde{\hat{d}}'_{R0}}=0$, $G_{\Delta vd11}=\frac{\Delta\tilde{v}_{BUS}}{\tilde{\hat{d}}'_{Rd}}=0$, $G_{\Delta vd12}=\frac{\Delta\tilde{v}_{BUS}}{\tilde{\hat{d}}'_{Rq}}=0,$
$G_{\Delta vd13}=\frac{\Delta\tilde{v}_{BUS}}{\tilde{\hat{d}}'_{R0}}=\frac{\sqrt{2}I^*_{IN}\alpha}{C}\frac{1}{s+\beta_{15}}$,
$G_{iu11}=\frac{\tilde{\hat{i}}_d}{\tilde{u}_d}=\frac{1}{L_R}\frac{s^2+\tau s+\beta_{16}}{s^3+\tau s^2+\left(\omega^2_{IN}\beta_{12}+\beta_{13}\right)s+\tau\omega^2_{IN}}$,
$G_{iu12}=\frac{\tilde{\hat{i}}_d}{\tilde{u}_q}=\frac{\omega_{IN}}{L_R}\frac{s+\beta_{11}}{s^3+\tau s^2+\left(\omega^2_{IN}\beta_{12}+\beta_{13}\right)s+\tau\omega^2_{IN}}$,
$G_{iv21}=\frac{\tilde{\hat{i}}_q}{\tilde{u}_d}=-\frac{\omega_{IN}}{L_R}\frac{s+\beta_{17}}{s^3+\tau s^2+\left(\omega^2_{IN}\beta_{12}+\beta_{13}\right)s+\tau\omega^2_{IN}}$,
$G_{iu22}=\frac{\tilde{\hat{i}}_q}{\tilde{u}_q}=\frac{1}{L_R}\frac{s^2+\tau s+\beta_{13}}{s^3+\tau s^2+\left(\omega^2_{IN}\beta_{12}+\beta_{13}\right)s+\tau\omega^2_{IN}}$,

Table 5. 3Φ5L E-Type Rectifier Transfer Functions

$$G_{vu11} = \frac{\tilde{v}_{BUS}}{\tilde{u}_d} = \frac{6\sqrt{2}V_{IN}}{CL_R V^*_{BUS}} \frac{s+\beta_{18}}{s^3+\tau s^2+\left(\omega^2_{IN}\beta_{12}+\beta_{13}\right)s+\tau\omega^2_{IN}},$$

$$G_{vu12} = \frac{\tilde{v}_{BUS}}{\tilde{u}_q} = -\frac{6\sqrt{2}I^*_{IN}\omega_{IN}}{CV^*_{BUS}} \frac{s+\beta_{14}}{s^3+\tau s^2+\left(\omega^2_{IN}\beta_{12}+\beta_{13}\right)s+\tau\omega^2_{IN}},$$

$$G_{\Delta vu11} = \frac{\Delta\tilde{v}_{BUS}}{\tilde{u}_d} = 0,\ G_{\Delta vu12} = \frac{\Delta\tilde{v}_{BUS}}{\tilde{u}_q} = 0,$$

$$\tau = \frac{1}{RC},\ \beta_{11} = \tau + \frac{12V_{IN}I^*_{IN}}{CV^{*2}_{BUS}},\ \beta_{12} = 1 + \frac{12L_R I^{*2}_{IN}}{CV^{*2}_{BUS}},\ \beta_{13} = \frac{12V^2_{IN}}{CLV^{*2}_{BUS}},\ \beta_{14} = -\frac{V_{IN}}{L_R I^*_{IN}},$$

$$\beta_{15} = \tau - \frac{6V_{IN}I^*_{IN}}{CV^{*2}_{BUS}},\ \beta_{16} = \frac{12L_R\omega^2_{IN}I^{*2}_{IN}}{CV^{*2}_{BUS}},\ \beta_{17} = \tau - \frac{12V_{IN}I^*_{IN}}{CV^{*2}_{BUS}},\ \beta_{18} = \frac{L_R\omega^2_{IN}I^*_{IN}}{V_{IN}}.$$

4.2.3.1 Small Signals Simulation Results

In order to validate the 3Φ5L E-Type Rectifier small signal model, a full digital-switching converter description has been developed within the Matlab/Simulink environment. The obtained model has been analyzed using the provided linear analysis tool.

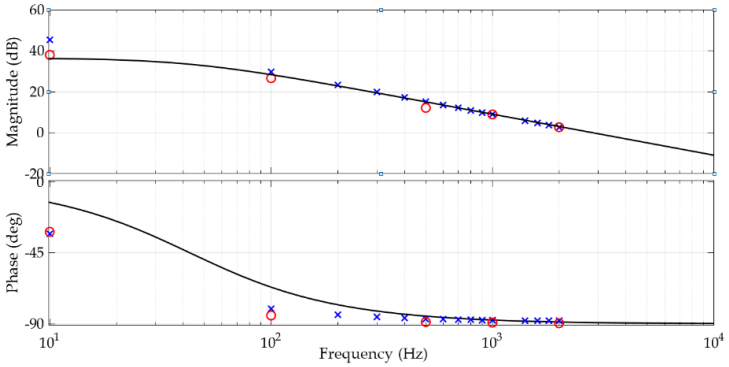


Fig. 63. Bode diagrams related to the transfer function control input $\tilde{d}'_{R0}$ to output $\Delta\tilde{v}_{BUS}$: small signal model (solid trace), average model (blue cross) and linearized switching model (red circle).

The operating condition of the PMSG and rectifier are the same as described in the previous section (operating specifications as in Table 3, output load is modeled as a pure resistor, the electric generator mechanical speed is set to *3500 rpm*, resulting in a rectifier modulation depth around *0.95)*. In such conditions, the steady-state values of the RMS supply voltage, the RMS phase current and

the DC-bus output voltage are respectively equal to *250 V*, *22 A* and *700 V*. The Bode diagram between the control inputs $\tilde{d}'_{R0}$ and the output $\Delta\tilde{v}_{BUS}$ is depicted in Fig. 63, where it exhibits a first order system behavior. It can be recognized the good agreement between the proposed linear system analytical representation and the linearized models.

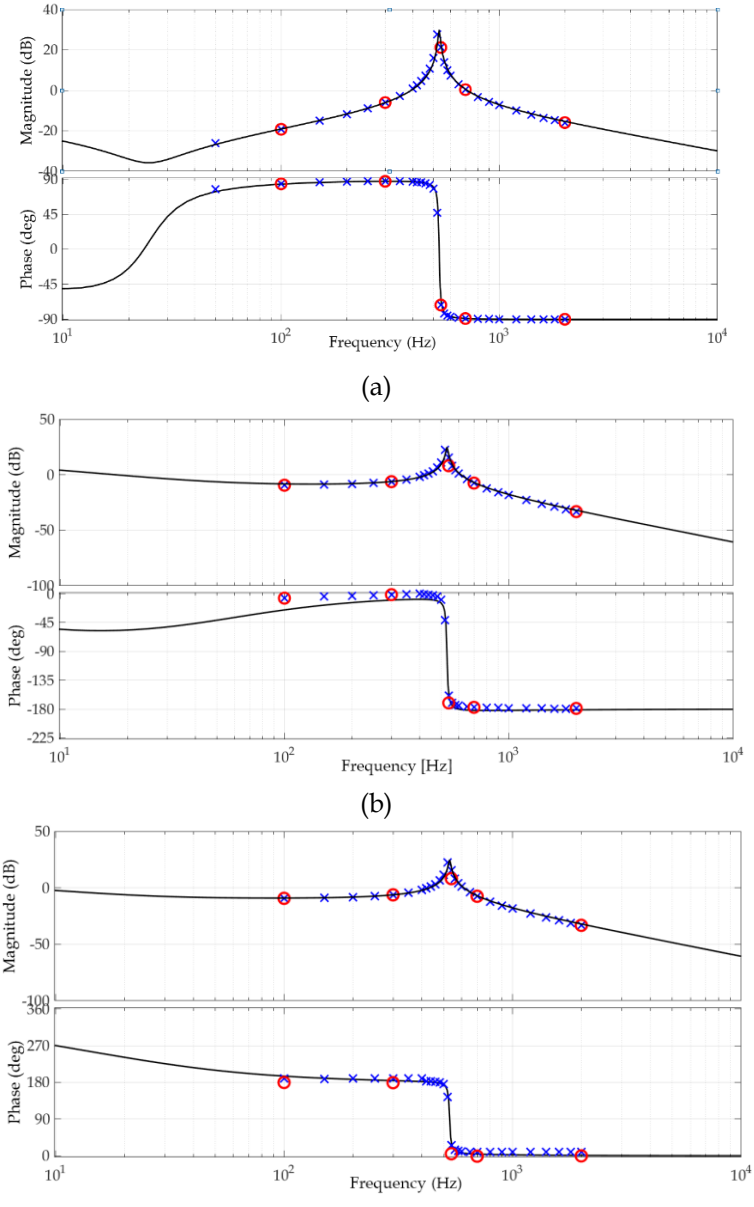
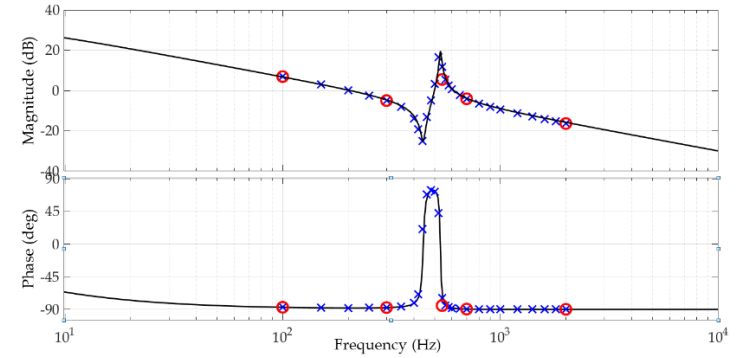


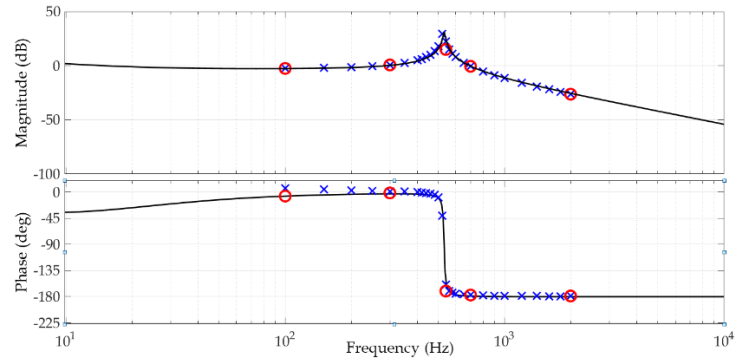
Fig. 64. Bode diagrams related to the transfer functions inputs $\tilde{u}_d$, $\tilde{u}_q$ to outputs $\tilde{\imath}_d$, $\tilde{\imath}_q$ and $\tilde{v}_{BUS}$: small signal model (solid trace), average model (blue cross) and linearized switching model (red circle). a) G_{iu11}(s), b) G_{iu12}(s), c) G_{iu21}(s).

Fig. 64 and Fig. 65 show the results of the group of transfer functions (TFs) between the disturbance inputs $\tilde{u}_d$, $\tilde{u}_q$ and the outputs $\tilde{\imath}_d$, $\tilde{\imath}_q$, $\tilde{v}_{BUS}$ and

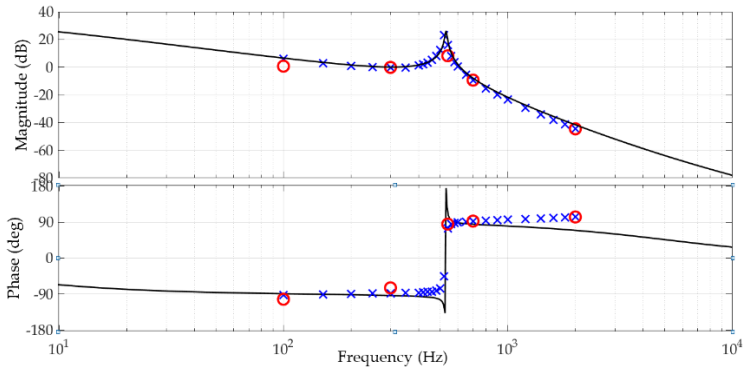
$\Delta\tilde{v}_{BUS}$. The TFs in this group have in common to be 3rd order systems due to inductance and capacitors degeneration as highlighted in Fig. 58. It can be noticed that the three completely different analytical descriptions exhibit a good matching for all the non-zero transfer functions.



(a)



(b)



(c)

Fig. 65. Bode diagrams related to the transfer functions inputs $\tilde{u}_d$, $\tilde{u}_q$ to outputs $\tilde{\imath}_d$, $\tilde{\imath}_q$ and $\tilde{v}_{BUS}$: small signal model (solid trace), average model (blue cross) and linearized switching model (red circle). a) $G_{iu22}(s)$, b) $G_{vu11}(s)$, c) $G_{vu12}(s)$.

The remaining TFs will be shown in the next section since they have been validated through the experimental test.

4.3 Experimental Results

4.3.1 Setup description

The conceptual scheme of the test rig used to perform the experimental tests is depicted in Fig. 66.

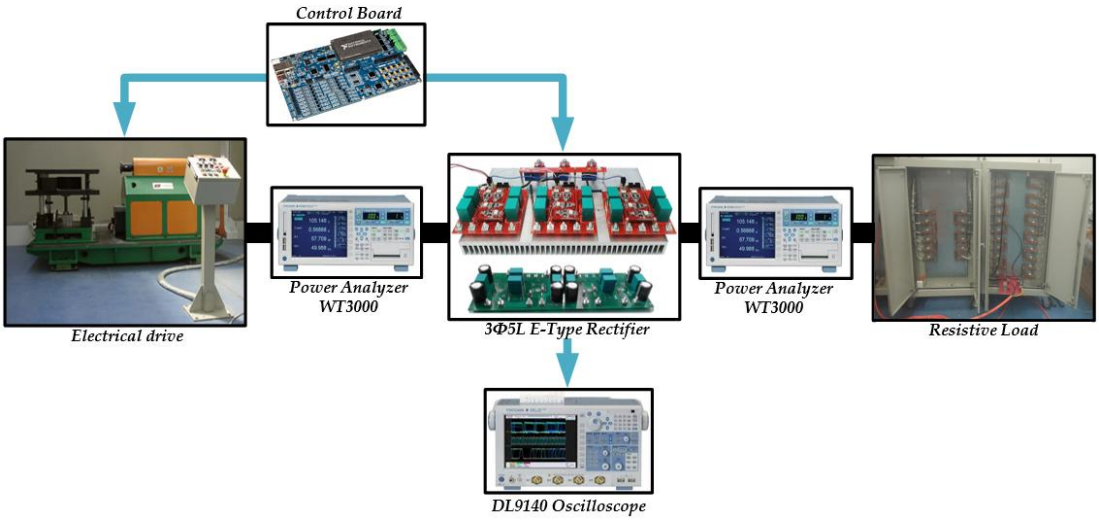


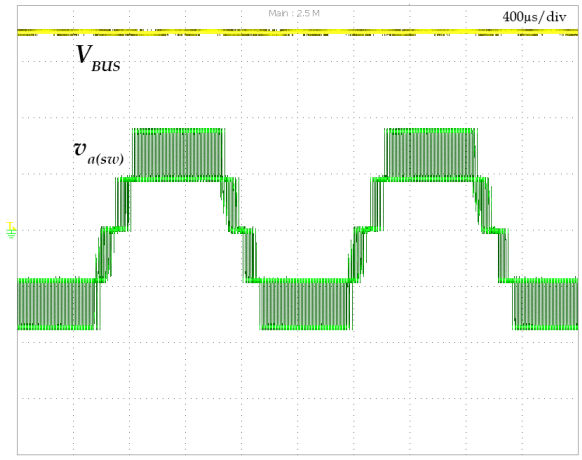
Fig. 66. Experimental setup.

The generator speed was set to 15000 rpm, to fully exploit all the five levels of the 3Φ5L E-Type Rectifier; consequently, the PMSG phase EMF measures 250 Vrms. The experimental tests were performed constant torque and variable rotation speed. The DC-bus voltage was properly controlled at 700 V through a dedicated outer voltage loop. Furthermore, the fundamental frequency, the switching frequency, the SRBC switching frequency, the rated phase current at rated torque and the synchronous inductance were set at 750 Hz, 12 kHz, 20 kHz, 22 Arms and 100 μH, respectively. The gains of the Proportional-Integral controllers have been tuned using the previously obtained and described TFs to provide 750 Hz bandwidth on both d and q axes.

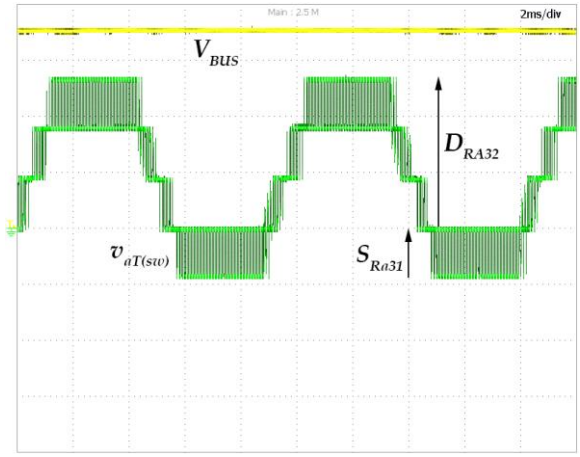
4.3.2 Voltage and current waveforms

The 3Φ5L E-Type Rectifier has been loaded by a pure resistive load. The selected resistive load is 36Ω. With reference to the nomenclature of the Fig. 45,

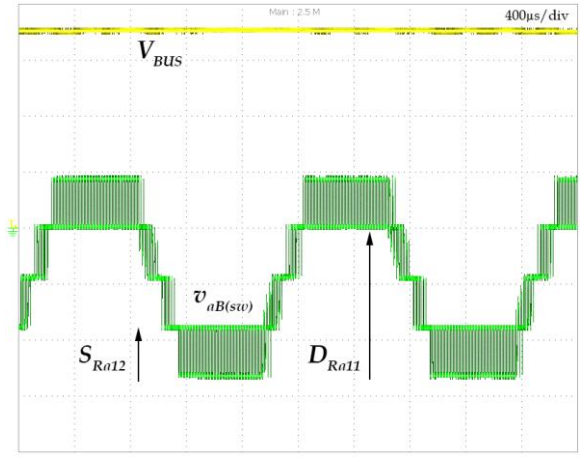
Fig. 67 shows the DC-bus voltage, the input-to-neutral switching voltage $u_{a(sw)}$, the voltage across the top middle leg $u_{aT(sw)}$ and the voltage across bottom middle leg $u_{aB(sw)}$, respectively.



(a)



(b)



(c)

Fig. 67. a) DC-bus voltage V_{BUS} and input-to-neutral switching voltage $u_{a(sw)}$; b) DC-bus voltage V_{BUS} and top middle leg to neutral voltage $u_{aT(sw)}$; c) DC-bus voltage V_{BUS} and Bottom-middle leg to neutral voltage $u_{aB(sw)}$. Voltage (200 V/div).

It can be seen from Fig. 67a that the maximum blocking voltage across the switches S_{A22}, S_{A21} and the diodes D_{A22}, D_{A21} is $½V_{BUS}$. Fig. 67b illustrates that the maximum blocking voltages across the switch S_{A31} and diode D_{A32} are $¼V_{BUS}$ and $¾V_{BUS}$, respectively; instead, the maximum blocking voltages across the switch S_{A12} and diode D_{A11} are $¼V_{BUS}$ and $¾V_{BUS}$, respectively, Fig. 67c.

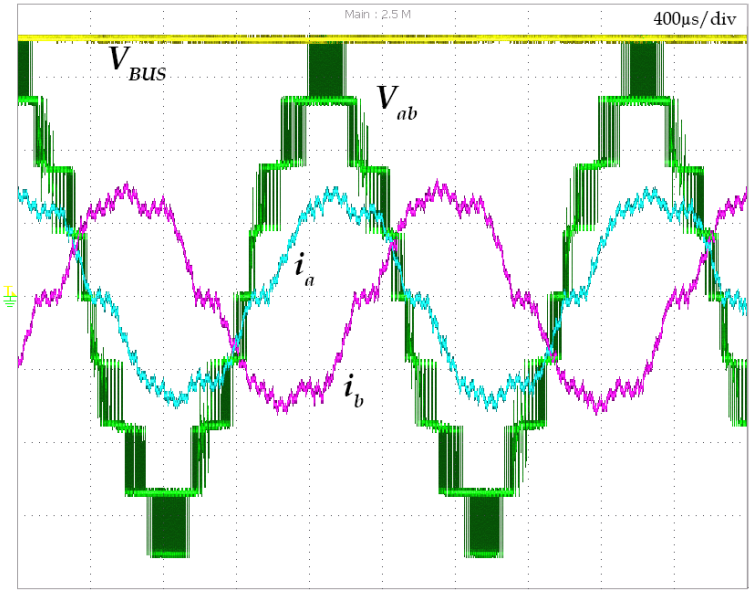
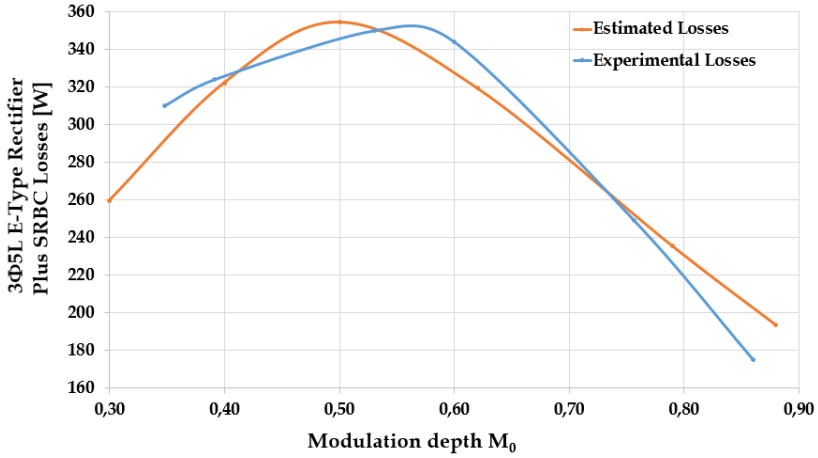


Fig. 68. DC-bus voltage V_{BUS} (yellow line), line-to-line voltage (green line) and phase currents (magenta and blue line). Voltage (200 V/div), current (20 A/div).

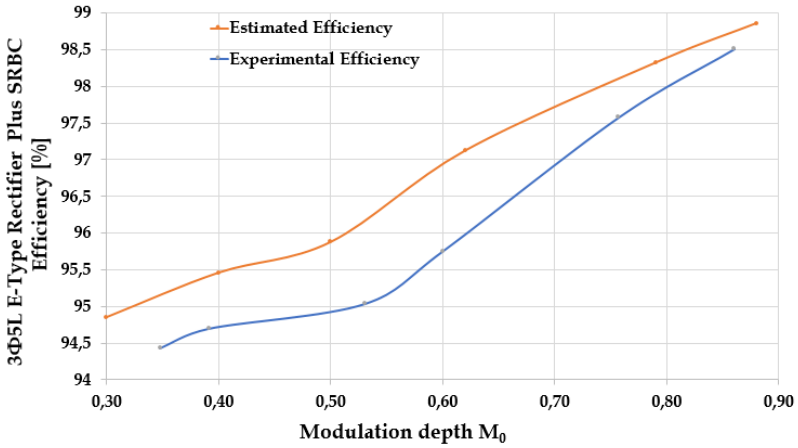
Finally, Fig. 68 shows the DC-bus voltage V_{BUS}, line-to-line voltage V_{ab} and phase currents i_a, i_b.

4.3.3 Losses results

The experimentally achieved losses and efficiency of the 3Φ5L E-Type Rectifier are compared with the estimated losses and efficiency in order to confirm the theoretical performance analysis. It can be seen in Fig. 69, the experimental results exhibit a good matching compared to the theoretical analysis. Consequently, the achieved experimental point validates the theoretical performance analysis of the rectifier.



(a)



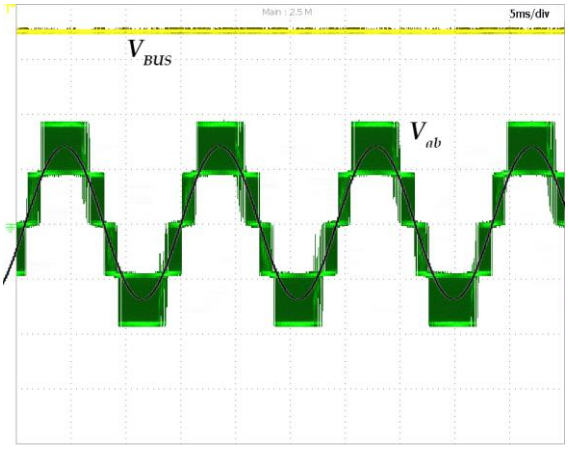
(b)

Fig. 69. Experimental and estimated performance of the 3Φ5L E-Type Rectifier versus modulation depth M_0: a) losses; b) efficiency.

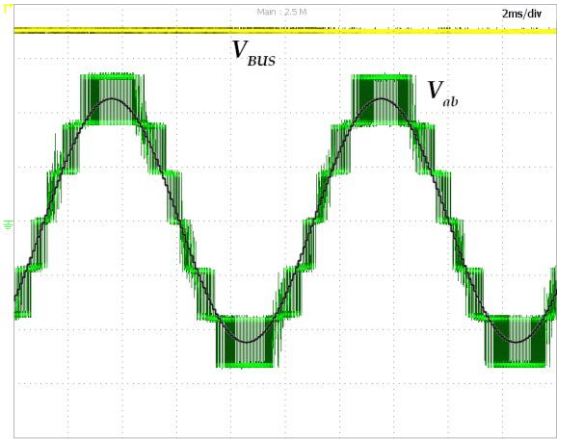
4.3.4 Large and Small Signal Experimental results

Three different operating conditions have been considered according to the rectifier output voltage levels, in order to validate the large signal model. Fig. 70 shows the DC-Bus voltage and the rectifier input line-to-line voltage V_{ab} with superimposed the line-to-line voltage achieved from the average model. In Fig. 70a the generator mechanical speed is set around 1600 r/min, giving as a results a rectifier modulation index around 0.45. In Fig. 70b the PM machine speed is set at 2700 r/min and the modulation index is 0.7. Results obtained for PM machine speed around 3500 r/min and modulation index around 0.9 are depicted in Fig. 70c. It can be seen a good matching between the experimental result and the analytical equations simulation model. In each case, the phase peak current is set

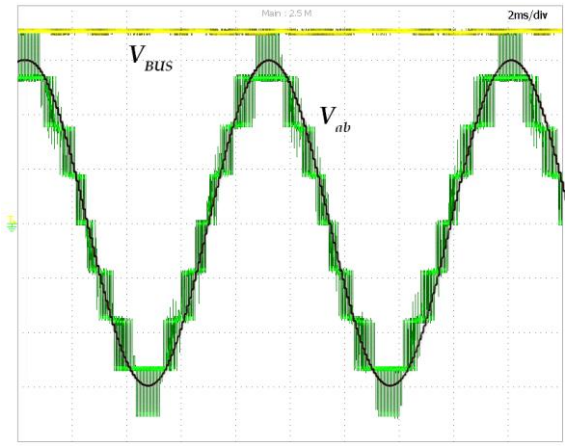
at 30 A, the displacement is close to one and the phase disposition PWM modulation with sinusoidal third–harmonic injection is considered.



(a)



(b)



(c)

Fig. 70. Converter experimental line-to-line input voltage (200 V/div) with superimposed the result from the average model: (a) modulation index close to 0.45 (3 levels operation), modulation index closes to 0.70 (4 levels operation), modulation index closes to 0.90 (5 levels operation).

Simulation results shown in Fig. 62 can be compared with the experimental behavior depicted in Fig. 71, where both V_{BUS} and Δv_{BUS} are illustrated. It can be seen from Fig. 71 that the V_{BUS} has been achieved removing the DC component from the measured DC-bus voltage, resulting in a straightforward comparison with the results of Fig. 62.

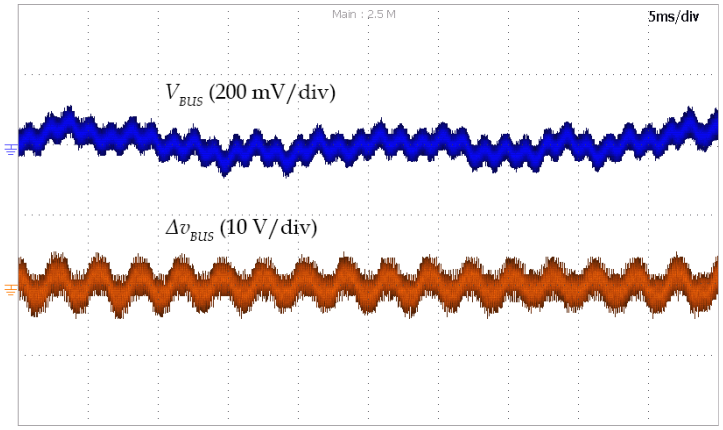
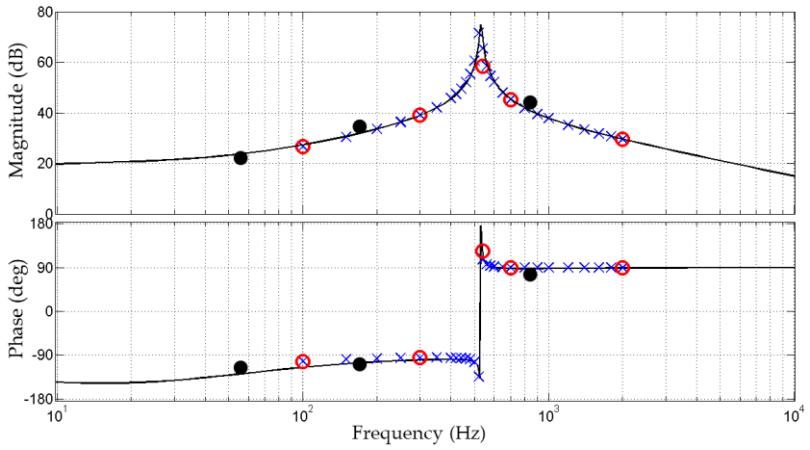


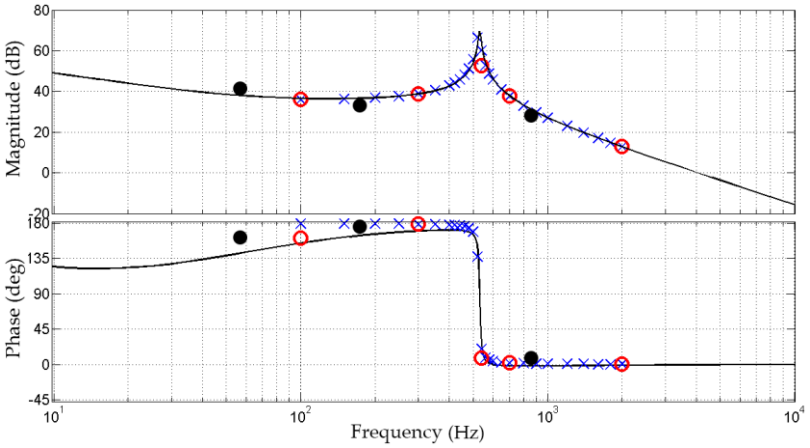
Fig. 71. Experimental waveform: a) V_{BUS}, b) Δv_{BUS}.

The experimental results of the small signal model were carried out according to the following procedure. In order to stimulate the system, the sinusoidal perturbation has been generated internally to an FPGA. Each perturbation was characterized by a proper amplitude, frequency and zero reference phase. Afterwards, the output measure to be considered for each TF has been analyzed by a Yokogawa WT3000 precision analyzer setup in harmonic mode. Thus, the related output harmonic can be obtained with respect to magnitude and phase. However, phase synchronization is a hard issue when TFs have to be carried out. In order to overcome this issue, the input stimulus and the output measurement have been synchronized by a dedicated trigger signal which was internally generated by the FPGA and acquired by the WT3000 as zero-phase reference. Fig. 73 shows the simulation and experimental results of the TFs group that relates the control inputs $\tilde{d}'_{Rd}$ and $\tilde{d}'_{Rq}$ to the outputs $\tilde{\imath}_d$, $\tilde{\imath}_q$ and $\tilde{v}_{BUS}$. The reported TFs are still related to 3rd order systems having the same pole locations but different zeros of the previous TFs groups. Solid line is related to the small-signal model, whereas cross, circle and black dot are the achieved results from the large

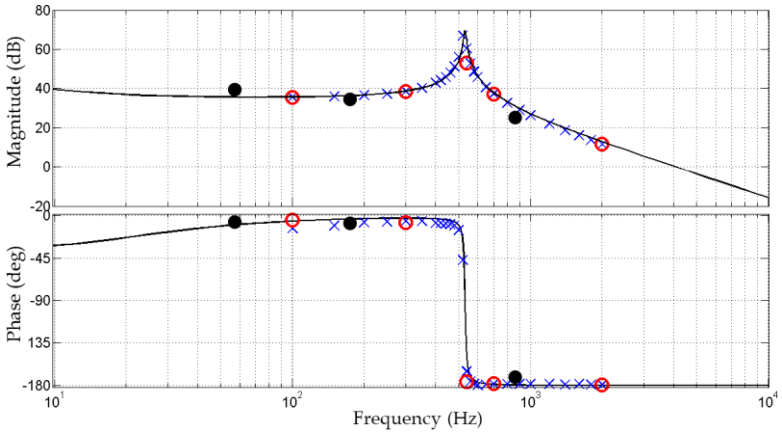
signal average model, the linearized switching model and the experimental results, respectively.



(a)

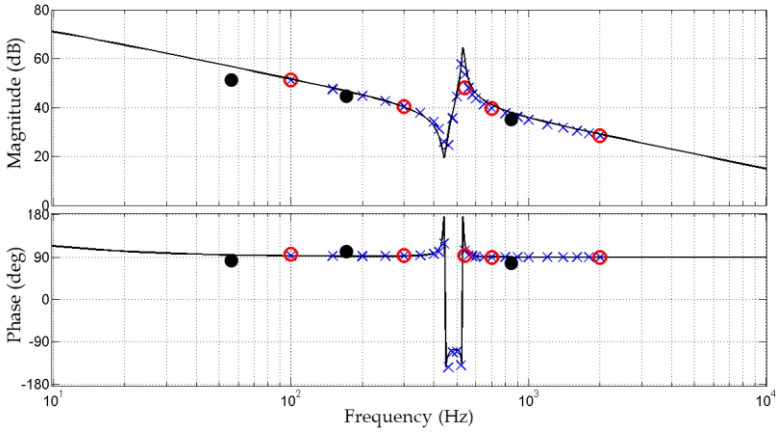


(b)

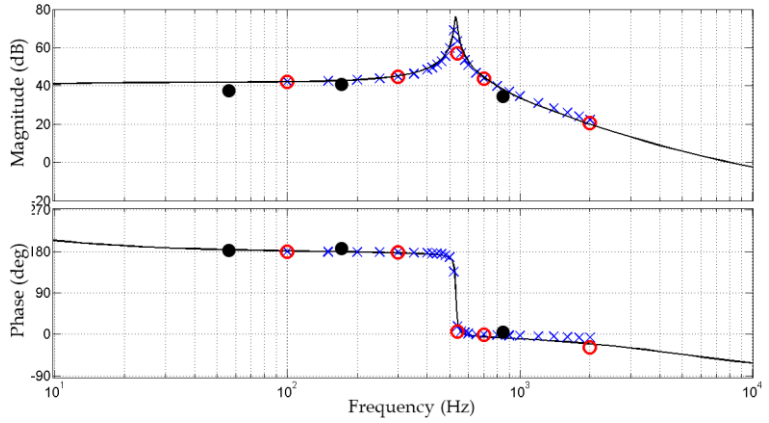


(c)

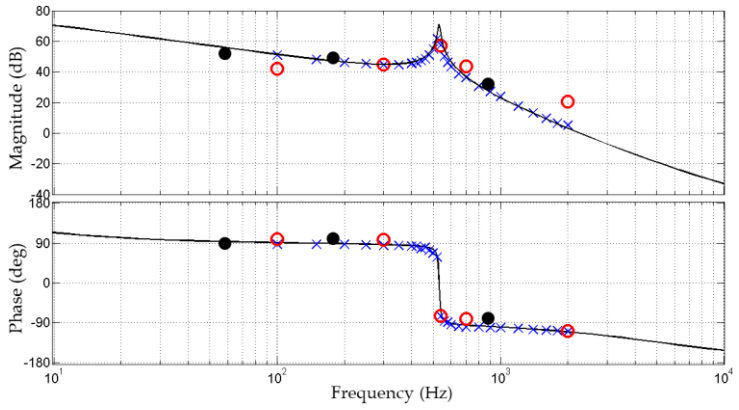
Fig. 72. Bode diagrams related to the transfer functions control inputs $\tilde{d}'_{Rd}$ and $\tilde{d}'_{dq}$ to outputs $\tilde{\imath}_d$, $\tilde{\imath}_q$ and $\tilde{v}_{BUS}$: small signal model (solid trace), average model (blue cross), linearized switching model (red circle) and experimental results (black dot). a) G_{id11}(s), b) G_{id12}(s), c) G_{id21}(s).



(a)



(b)



(c)

Fig. 73. Bode diagrams related to the transfer functions control inputs $\tilde{d}'_{Rd}$ and $\tilde{d}'_{dq}$ to outputs $\tilde{\imath}_d$, $\tilde{\imath}_q$ and $\tilde{v}_{BUS}$: small signal model (solid trace), average model (blue cross), linearized switching model (red circle) and experimental results (black dot). a) G_{id22}(s), b) G_{vd11}(s), c) G_{vd12}(s).

PART THREE

5 LEVEL E-TYPE BACK-TO-BACK CONVERTER

5 INTRODUCTION

5.1 Operating Principle of the 5L BTB Converter

The 3Φ5L E-Type Rectifier discussed in the previous chapter is used in the double conversion system AC/AC because of the achieved interesting results in terms of the efficiency, weight and volume. The basic circuit diagram of the solution under consideration is shown in Fig. 74. The complete system consists of a 3Φ5L E-Type Rectifier, a split DC-bus, a 3Φ5L E-Type Inverter and a bi-directional DC-DC converter.

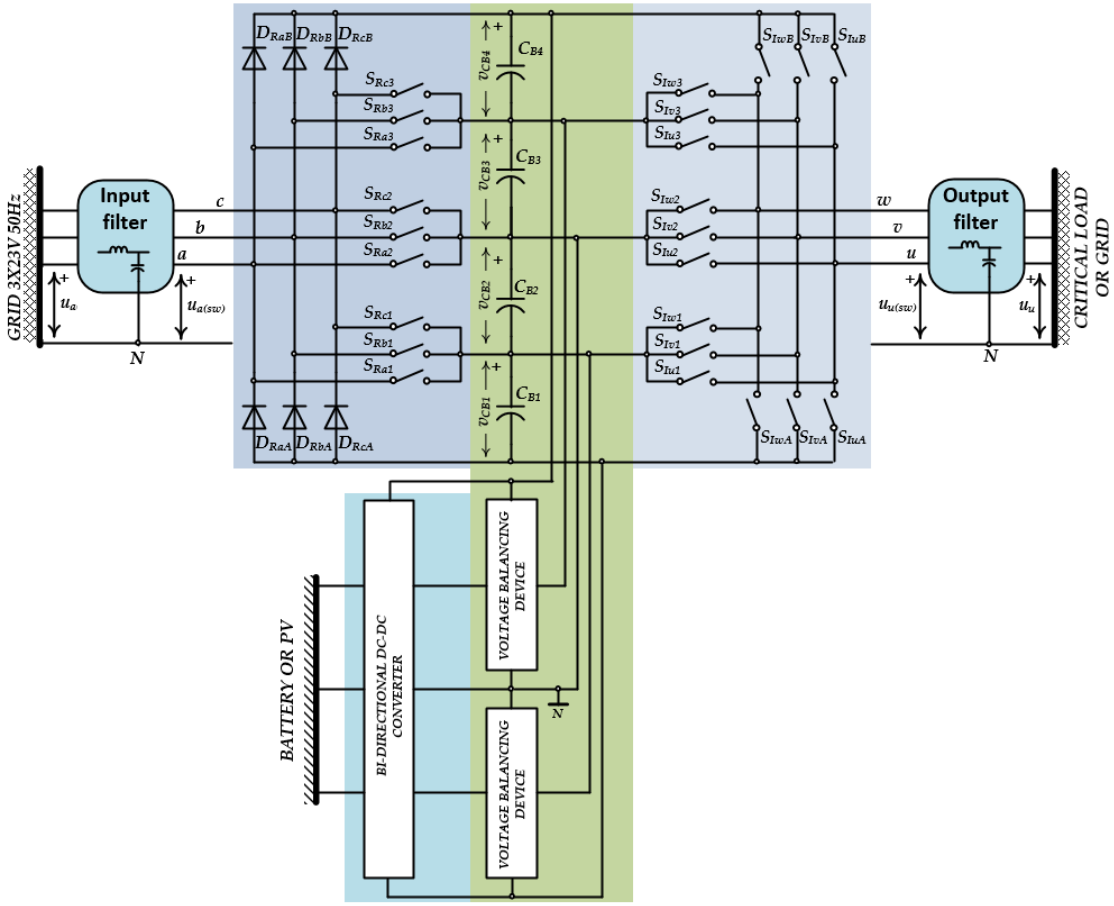


Fig. 74. Basic circuit diagram of the 5L E-Type Back-To-Back Converter plus Voltage Balancing Devices plus DC-DC Converter.

The Inverter is realized by a three-phase bidirectional bridge and a set of bidirectional switches connected between the DC-bus and the AC-side. The inverter, henceforward named as 5L E-Type Inverter, is controlled in a way to

maintain a sinusoidal output voltages u_u, u_v and u_w. The bi-directional DC-DC converter is used to manage the power flow between the DC-bus and the eventual DC source (battery or PV).

5.2 The Inverter Characteristics

The output specifications are defined as in Table 6.

Table 6. The 5 BTB Converter Output Variables Definition

Output Apparent Power	S_{OUT}	20kVA
Output Power Factor	PF_{OUT}	1
Output Voltage (Phase to Neutral RMS)	V_{OUT}	230 V
Output frequency	f_{OUT}	50 Hz
Output Current	$I_{OUT} = \frac{S_{OUT}}{3V_{OUT}}$	28.99 A
Output Voltage THD	THD_v	< 1%

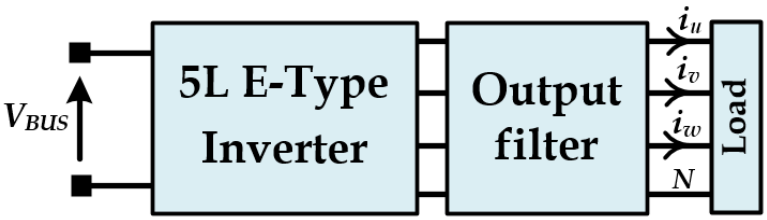


Fig. 75. Block scheme of the inverter as part of the complete conversion system.

Fig. 75 shows the block scheme related to the output system under examination.

5.3 The Rectifier Characteristics

The input specifications for the 5L BTB Converter are defined as in Table 7.

Table 7. 5L BTB Converter Input Variables Definition

Input Power Factor	PF_{IN}	1
Input Apparent Power	$S_{IN} = S_{OUT} \frac{PF_{OUT}}{PF_{IN}}$	
Input Voltage (Phase to Neutral RMS)	V_{IN}	230 V
Input voltage range	$V_{IN(\min)}$	176Vac - 276 Vac
Input Frequency	f_{IN}	50 Hz
Maximum Input Current (RMS)	$I_{GRID(\max)} = \frac{S_{OUT}}{3V_{IN(\min)}} \frac{PF_{OUT}}{PF_{IN}}$	
Input current THD	THD_i	< 3%
DC-bus Voltage	V_{BUS}	680 V ÷ 800 V

Fig. 76 shows the block scheme related to the input system under examination.

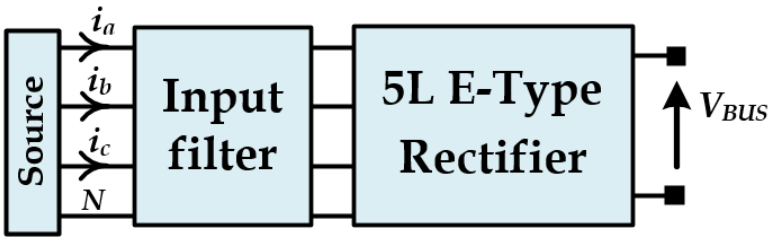


Fig. 76. Block scheme of the input rectifier.

The 5L E-Type Rectifier is controlled in order to ensure a sinusoidal input current and constant DC-bus voltage.

6 THEORETICAL ANALYSIS OF THE 5-LEVEL E-TYPE CONVERTER

6.1 5L E-Type BTB Converter Characteristics

Three-phase four wire equivalent circuit diagram of the 5L E-Type BTB Converter is presented in Fig. 77. The input current and voltage are defined in (7) and (8) with values of the RMS input voltage, RMS input current and frequency as in Table 7.

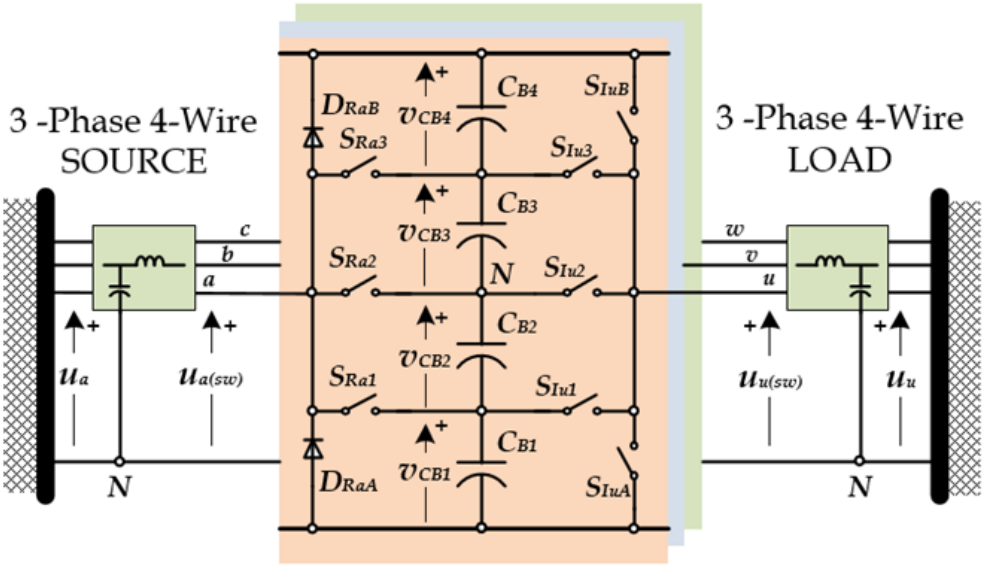


Fig. 77. Circuit diagram of the 5L E-Type BTB Converter.

The output voltage and current are summarized in (45) and (46), where φ_{OUT} is the phase displacement between the output voltage and the corresponding output current at the fundamental frequency.

$$\begin{cases} u_u(t) = \sqrt{2}V_{OUT}\sin(\omega_{OUT}t) \\ u_v(t) = \sqrt{2}V_{OUT}\sin\left(\omega_{OUT}t - \frac{2}{3}\pi\right) \\ u_w(t) = \sqrt{2}V_{OUT}\sin\left(\omega_{OUT}t - \frac{4}{3}\pi\right) \end{cases} \quad (45)$$

$$\begin{cases} i_u(\mathrm{t}) = \sqrt{2} I_{OUT} \sin\left(\omega_{OUT} t - \varphi_{OUT}\right) \\ i_v(\mathrm{t}) = \sqrt{2} I_{OUT} \sin\left(\omega_{OUT} t - \frac{2}{3}\pi - \varphi_{OUT}\right) \\ i_w(\mathrm{t}) = \sqrt{2} I_{OUT} \sin\left(\omega_{OUT} t - \frac{4}{3}\pi - \varphi_{OUT}\right) \end{cases} \tag{46}$$

From the output voltage specification, V_{OUT}, we can obtain the modulation depth for the inverter, (47).

$$M_{0,I} = \frac{2\sqrt{2} V_{OUT}}{V_{BUS}} \tag{47}$$

The 5L E-Type Rectifier characteristic has been obtained in the part two of this dissertation. Obviously, output-to-neutral switching voltage $u_{Q(sw)}$, with $Q \in \{u, v, w\}$, can be obtained in the same manner. In the 5L E-Type Inverter the top-middle and bottom-middle legs are not unidirectional. For this reason, the threshold function will not be considered. The switching function of the 5L E-Type Inverter S_{IQy}, with $y \in \{\mathrm{A}, 1, 2, 3, \mathrm{B}\}$ is defined by (48).

$$S_{IQy} = \begin{cases} 0 & \text{switch off} \\ 1 & \text{switch on} \end{cases} \tag{48}$$

The output-to-neutral switching voltage $u_{Q(sw)}$ can be obtained as in (49).

$$u_{Q(sw)} = \left(1 - S_{IQ2}\right)\left[u_{BUS,Ih} - u_{BUS,Il}\right] \tag{49}$$

The upper and lower DC-bus voltages, $u_{BUS,Ih}$ and $u_{BUS,Il}$, can be written as in (50).

$$\begin{aligned} u_{BUS,\mathrm{Il}} &= v_{CB2}\left(S_{IQA} - S_{IQ1}\right)^2 + v_{CB1}\left(1 - S_{IQ1}\right) S_{IQA} \\ u_{BUS,Ih} &= v_{CB3}\left(S_{IQB} - S_{IQ3}\right)^2 + v_{CB4}\left(1 - S_{IQ3}\right) S_{IQB} \end{aligned} \tag{50}$$

Substituting (10) and (50) into (49), the output-to-neutral switching voltage can be completely defined as in (51).

$$u_{Q(sw)} = \frac{V_{BUS}}{4}\left(1 - S_{IQ2}\right)\left[\left(2S_{IQB} + S_{IQ3} - 3S_{IQ3}S_{IQB}\right) - \left(2S_{IQA} + S_{IQ1} - 3S_{IQ1}S_{IQA}\right)\right] \tag{51}$$

When the switching functions S_{IQA} and S_{IQB} are always "on" (switches always closed), the equation (51) degenerates into equation (15). As shown in Table 8, the output-to-neutral switching voltage can take one of the 5 values; $\pm V_{BUS}/2$, $\pm V_{BUS}/4$ and 0.

Table 8. Output-to-neutral switching voltage versus switching function.

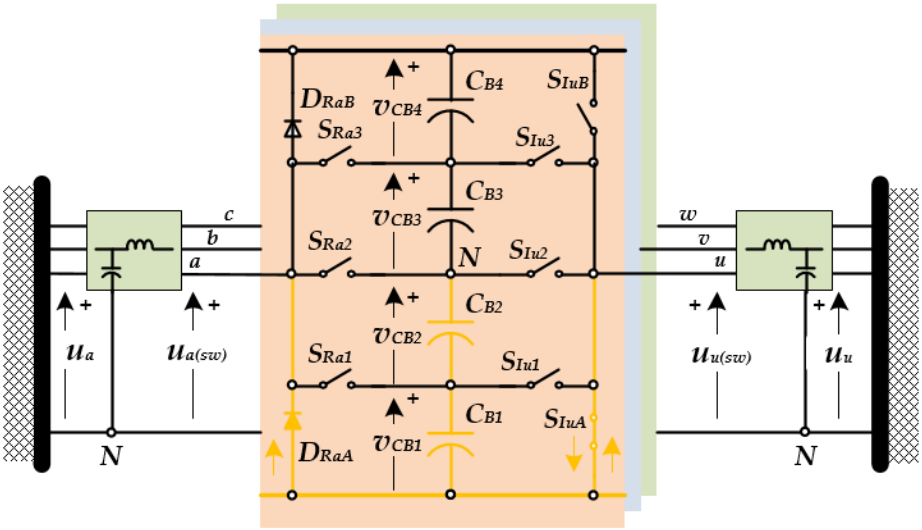
State I	S_{IQA}	S_{IQ1}	S_{IQ2}	S_{IQ3}	S_{IQB}	$s_{Q(sw)}$
1	0	0	0	0	0	0
2	0	0	0	0	1	$V_{BUS}/2$
3	0	0	0	1	0	$V_{BUS}/4$
4	0	0	0	1	1	0
5	0	0	1	0	0	0
6	0	0	1	0	1	0
7	0	0	1	1	0	0
8	0	0	1	1	1	0
9	0	1	0	0	0	$-V_{BUS}/4$
10	0	1	0	0	1	$V_{BUS}/4$
11	0	1	0	1	0	0
12	0	1	0	1	1	$- V_{BUS}/4$
13	0	1	1	0	0	0
14	0	1	1	0	1	0
15	0	1	1	1	0	0
16	0	1	1	1	1	0
17	1	0	0	0	0	$- V_{BUS}/2$
18	1	0	0	0	1	0
19	1	0	0	1	0	$- V_{BUS}/4$
20	1	0	0	1	1	$- V_{BUS}/2$
21	1	0	1	0	0	0
22	1	0	1	0	1	0
23	1	0	1	1	0	0
24	1	0	1	1	1	0
25	1	1	0	0	0	0
26	1	1	0	0	1	$V_{BUS}/2$
27	1	1	0	1	0	$V_{BUS}/4$
28	1	1	0	1	1	0
29	1	1	1	0	0	0
30	1	1	1	0	1	0
31	1	1	1	1	0	0
32	1	1	1	1	1	0

6.2 5L E-Type BTB Converter Operating Areas

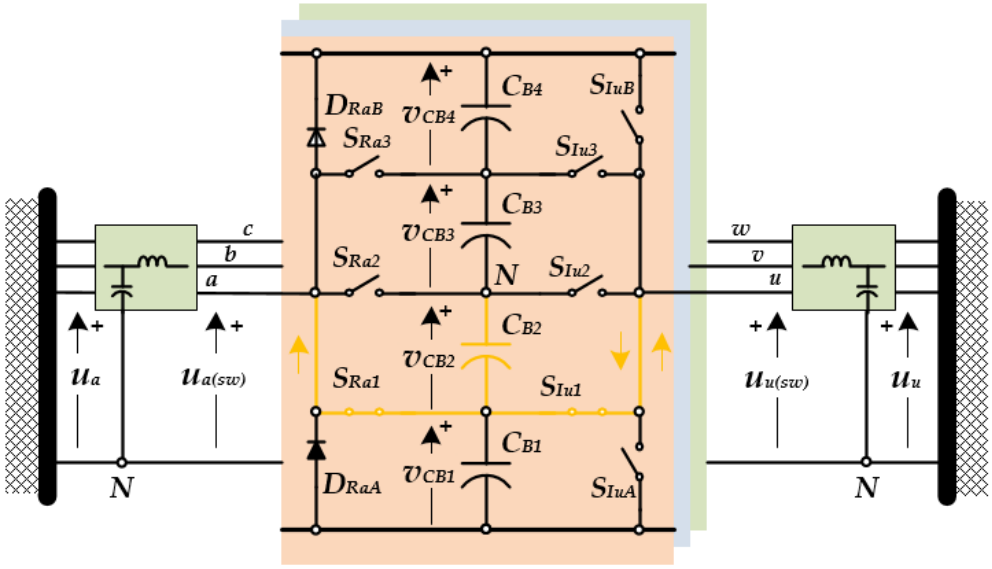
The input/output-to-neutral switching voltage (equations (15) and (51)) show five voltage levels. According to the Fig. 42, the 5L E-Type BTB Converter can operates in four different areas.

a) Area 1

The phase-to-neutral voltages u_{aN} and u_{uN} are negative and the input/output-to-neutral switching voltages $u_{a(sw)}$ and $u_{u(sw)}$ can assume the two discrete values -½V_{BUS} and -¼V_{BUS} depending on the states of the switches S_{Ra1} and S_{Iu1}, S_{IuA}, Fig. 78. The input phase current i_a is negative (the direction is from the DC-side to AC-side). The output phase current i_u can be both positive and negative.



(a)



(b)

Fig. 78. Converter operating area 1: a) $u_{a(sw)}$=$u_{u(sw)}$=-½V_{BUS}, b) $u_{a(sw)}$=$u_{u(sw)}$=-¼V_{BUS}.

b) Area 2

The phase-to-neutral voltages u_{aN} and u_{uN} are negative and the

input/output-to-neutral switching voltage $u_{a(sw)}$ and $u_{u(sw)}$ can assume the two discrete values -¼V_{BUS} and 0 depending on the status of the switches S_{Ra2} and S_{Iu1}, S_{Iu2}, Fig. 78b and Fig. 79. In this area, the switch S_{Ra1} is "always on" and the switch S_{IuA} is "always off". The input phase current i_a is negative (the direction is from the DC-side to AC-side). The output phase current i_u can be both positive and negative.

c) Area 3

The phase-to-neutral voltages u_{aN} and u_{uN} are positive and the input/output to-neutral switching voltage $u_{a(sw)}$ and $u_{u(sw)}$ can assume the two discrete values 0 and ¼V_{BUS} depending on the status of the switches S_{Ra2} and S_{Iu2}, S_{Iu3}, Fig. 79 and Fig. 80a. The input phase current i_a is positive (the direction is from the AC-side to DC-side). The output phase current i_u can be both positive and negative.

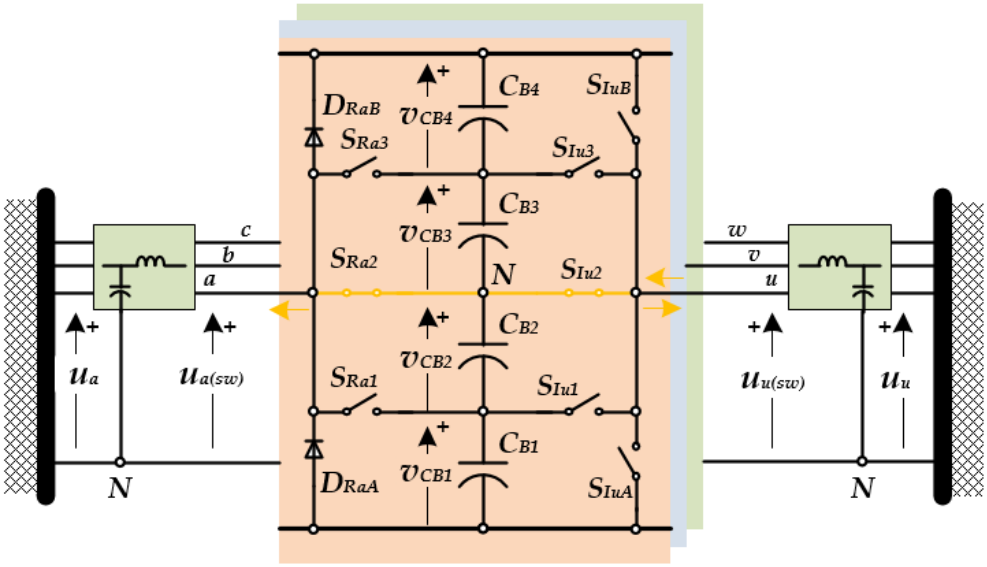
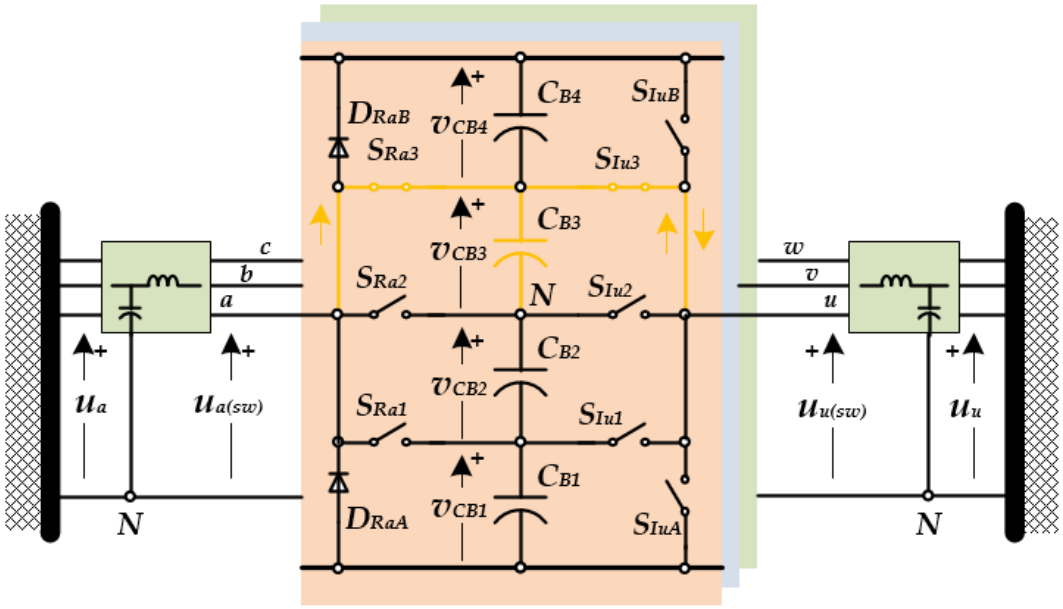


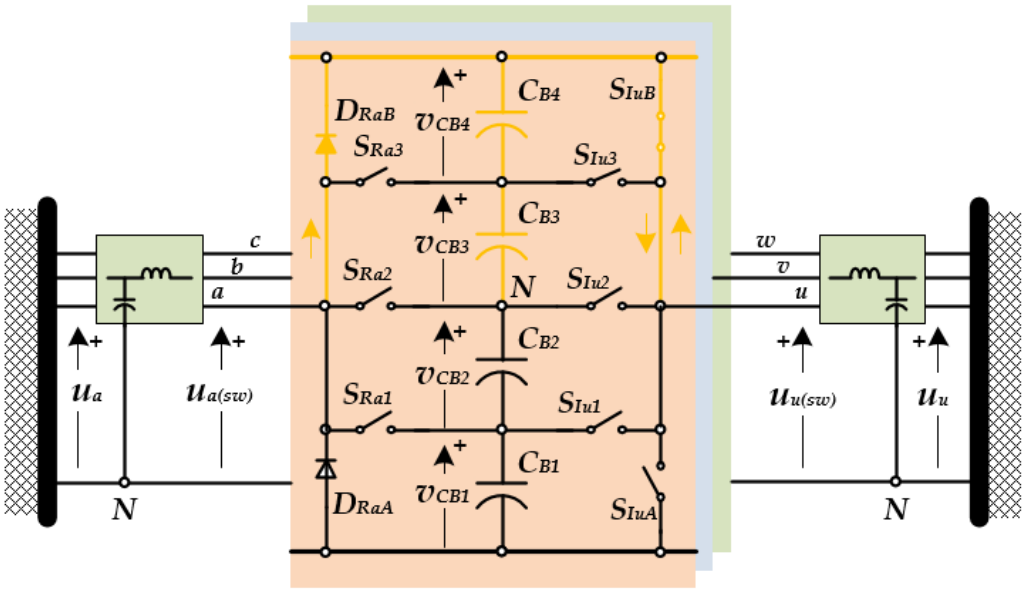
Fig. 79. Converter operating area 2: $u_{a(sw)}$=$u_{u(sw)}$=0.

a) Area 4

The phase-to-neutral voltages u_{aN} and u_{uN} are positive and the input/output to-neutral switching voltage $u_{a(sw)}$ and $u_{u(sw)}$ can assume the two discrete values ¼V_{BUS} and ½V_{BUS} depending on the status of the switches S_{Ra3} and S_{Iu3}, S_{IuB}, Fig. 80a and Fig. 80b. The input phase current i_a is positive (the direction is from the AC-side to DC-side). The output phase current i_u can be both positive and negative.



(a)



(b)

Fig. 80. Converter operating area 4: a) $u_{a(sw)}=u_{u(sw)}=¼V_{BUS}$, b) $u_{a(sw)}=u_{u(sw)}= ½V_{BUS}$.

6.3 Power Semiconductors Realization and Selection

Until now the power devices located into each leg of the 5L E-Type BTB Converter have been considered as ideal switches. Namely, when the switch is closed, the current flow through the switch is equal to the current of the filter inductor and the voltage across the switch terminal is equal to zero. When the switch is open, the current flow through the switch is equal to zero and the

voltage across the switch is not zero. An ideal switch does not exist, it is just an approximation! Let's see how to properly realize and select prospective power devices for the 5L E-Type BTB Converter, namely, how to choose the technology, the family, the voltage and current rating of the power semiconductors.

6.3.1 Switches Configuration

The 5L E-Type Rectifier shows a unidirectional power flow; therefore, the switches located in the top/bottom-middle leg-rectifier, S_{RP1} and S_{RP3}, are voltage bidirectional and current unidirectional, Fig. 81. For the bottom-middle leg-rectifier the current directional is from the DC-bus capacitors to the AC-side; whereas, for the top-middle leg-rectifier the current direction is from the AC-side to the DC-bus capacitors.

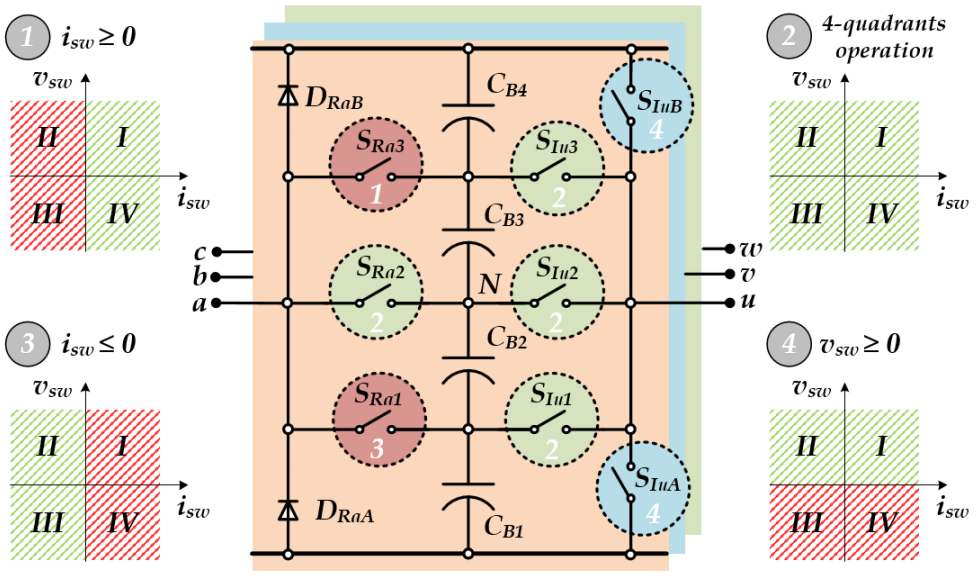


Fig. 81. 5L E-Type BTB Converter switches realization. 1: voltage bidirectional and current unidirectional ($i_{sw} \geq 0$), 2: voltage and current bidirectional, 3: voltage bidirectional and current unidirectional ($i_{sw} \leq 0$), 4: voltage unidirectional and current bidirectional.

The switch placed in the middle leg-rectifier S_{RP2} and the switches located in the middle, top-middle and bottom-middle leg-inverter, S_{IQ1} S_{IQ2} and S_{IQ3}, are voltage and current bidirectional, Fig. 81. The devices located in the outer leg-inverter S_{IQA} and S_{IQB} are voltage unidirectional and current bidirectional, Fig. 81.According to this analysis, a possible solution for realizing the switches S_{RP1}

and S_{RP3} is the series connection of either IGBT or MOSFET and diode, as depicted in Fig. 82a and Fig. 82b. The switches S_{RP2}, S_{IQ1}, S_{IQ2} and S_{IQ3} can be created by connecting two unidirectional switches IGBT or MOSFET in Common Collector CC (or common source) or in Common Emitter CE (or common drain), Fig. 82c and Fig. 82d. Additionally, we can realize a hybrid configuration by connecting a mixed combination of both IGBT and MOSFET, Fig. 82e.

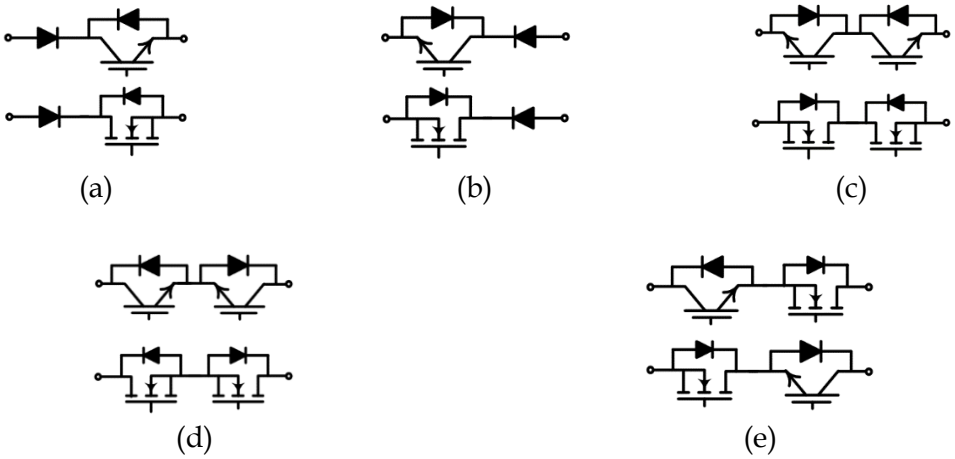


Fig. 82. Possible configuration of switches: a) voltage bidirectional and current unidirectional ($i_{sw} \geq 0$), b) voltage bidirectional and current unidirectional ($i_{sw} \leq 0$), c) bidirectional switches in CC, d) bidirectional switches in CE, e) hybrid bidirectional switches in CE.

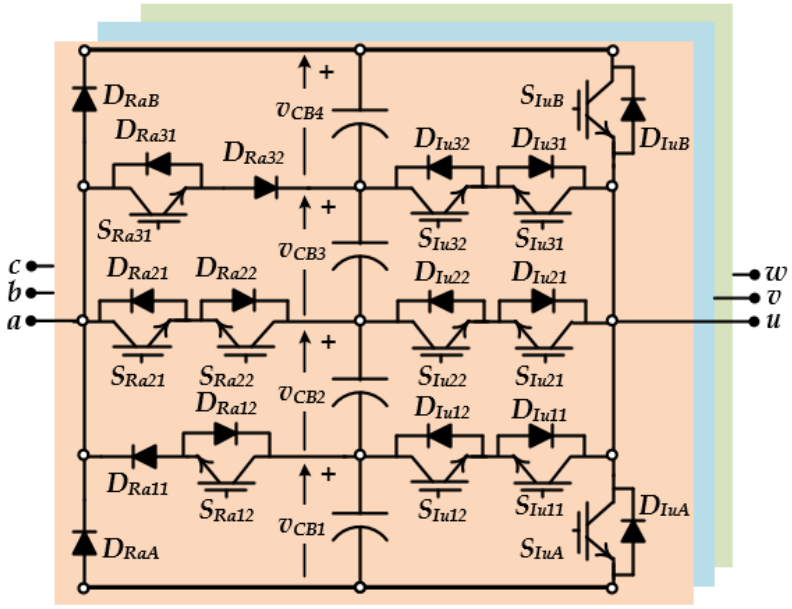


Fig. 83. Potential Configuration of the 5L E-Type BTB Converter.

Consequently, a possible configuration's devices for the 5L E-Type BTB Converter is shown in Fig. 83. As the switches' configuration is selected, we need to understand which devices should be used to assemble the converter. To this

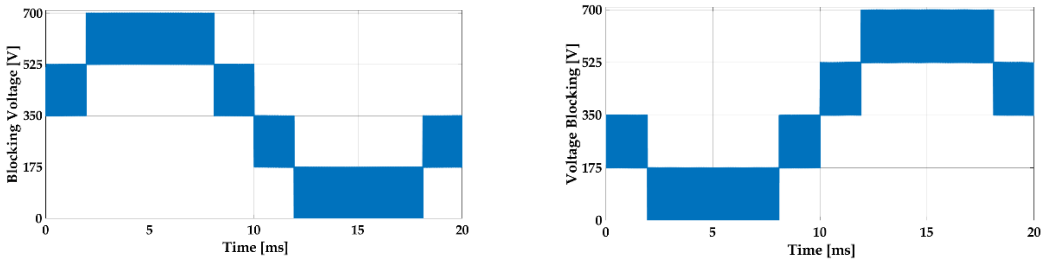
purpose, we need to know the devices' voltage stress and the devices' current stress.

6.4 The Switch Voltage Rating

The first step in the design of power electronic converters is to determine the voltage rating of potential power semiconductors. This step is important because if the rating of the devices is too close to the operating voltage, the risk of failure will be large, adversely affecting the converter reliability. On the other hand, if the voltage rating is chosen with excessive safety margins, overall efficiency and performance will suffer since higher rated devices require thicker silicon, which generates higher losses. The switches and diodes voltage rating are a function of the maximum blocking voltage $V_{BL(max)}$ across the devices during the commutation. In steady state, the maximum blocking voltage depends on the total DC-bus voltage V_{BUS} and the number of levels N according to the equation (52).

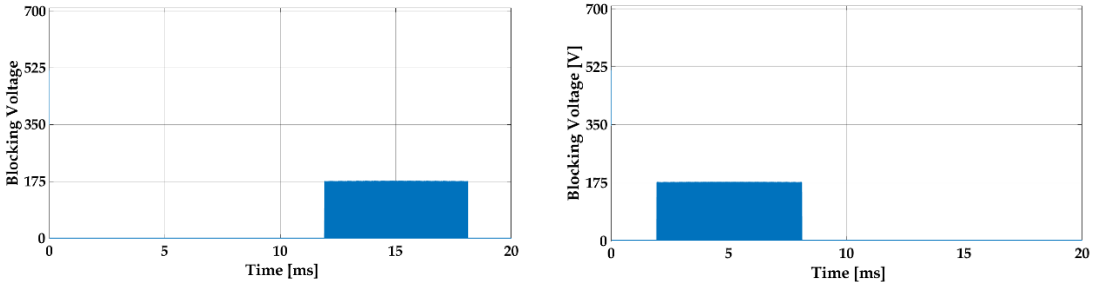
$$V_{BL(\max)} \overset{STEADY\ STATE}{=} \frac{V_{BUS}}{N-1} \tag{52}$$

The equation (52) is only valid for some of the devices of the 5L E-Type BTB Converter; the blocking voltage $V_{BL(max)}$ at a steady state depends on the power devices position into 5L E-Type BTB Converter. Considering the operating condition as mentioned in the previous section, namely $V_{IN(rms)}=V_{OUT(rms)}=230V$, $f_{IN}=f_{OUT}=50Hz$ and $V_{BUS}=700V$, the steady state blocking voltage across the diodes D_{RPA}, D_{RPB}, D_{IQA}, D_{IQB} and the switches, S_{IQA} and S_{IQB} with P∈{a, b, c} and $Q \in \{u, v, w\}$, (see Fig. 83) is depicted in Fig. 84. The fundamental period is shown for each waveform of interest. The maximum blocking voltage across these devices is V_{BUS}=700V.



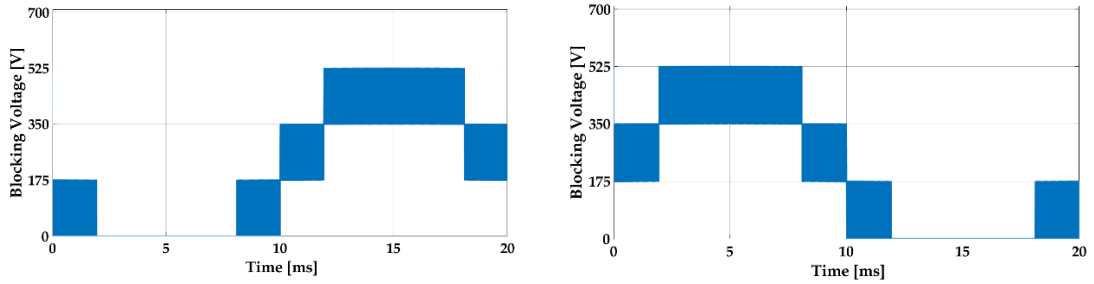
(a) (b)

Fig. 84. Blocking voltage at steady state: a) D_{RPA}, S_{IQA} and D_{IQA}; b) D_{RPB}, S_{IQB} and D_{IQB}.



(a) (b)

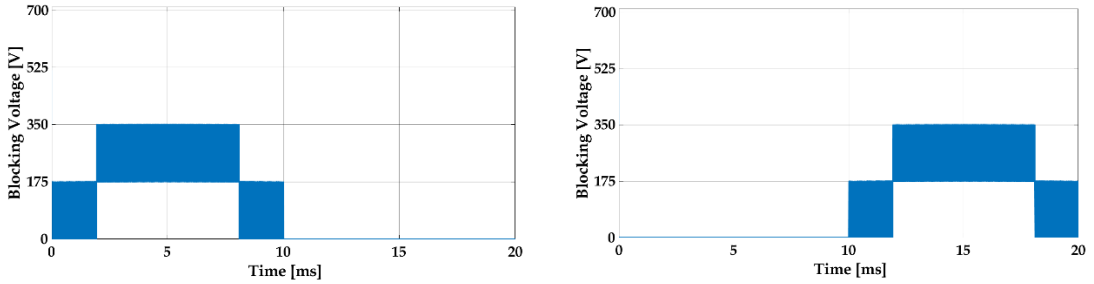
Fig. 85. Blocking voltage at steady state: a) D_{RP12}, D_{IQ12}, S_{RP12} and S_{IQ12}; b) D_{RP31}, D_{IQ31}, S_{RP31} and S_{IQ31}.



(a) (b)

Fig. 86. Blocking voltage at steady state: a) D_{RP11}, D_{IQ11} and S_{IQ11}; b) D_{RP32}, D_{IQ32} and S_{IQ32}.

The steady state blocking voltage across the diodes D_{RP12}, D_{IQ12}, S_{RP12} and S_{IQ12} and the switches D_{RP31}, D_{IQ31}, S_{RP31} and $S_{IQ31}$is shown in Fig. 85.



(a) (b)

Fig. 87. Blocking voltage at steady state: a) D_{RP21}, D_{IQ21}, S_{RP21} and S_{IQ21}; b) D_{RP22}, D_{IQ22}, S_{RP22} and S_{IQ22}.

The maximum blocking voltage across these devices is $¼V_{BUS}$=175V. The

maximum blocking voltage of the diodes and switches arranged in the bottom-middle and top-middle legs, D_{RP11}, D_{IQ11}, S_{IQ11} and D_{RP32}, D_{IQ32}, S_{IQ32}, is $¾V_{BUS}$=525V, as it results in Fig. 86.

Table 9. Blocking voltages at steady state for the devices in the 5L E-Type BTB Converter.

Devices	Blocking voltages
5L E-Type Rectifier	
$\boldsymbol{D_{RPA}}$, $\boldsymbol{D_{RPB}}$	V_{BUS}
$\boldsymbol{D_{RP11}}$, $\boldsymbol{D_{RP32}}$	$¾V_{BUS}$
$\boldsymbol{S_{RP12}}$, $\boldsymbol{D_{RP12}}$, $\boldsymbol{S_{RP31}}$, $\boldsymbol{D_{RP31}}$	$¼V_{BUS}$
$\boldsymbol{S_{RP21}}$, $\boldsymbol{S_{RP22}}$, $\boldsymbol{D_{RP21}}$, $\boldsymbol{D_{RP22}}$	$½V_{BUS}$
5L E-Type Inverter	
$\boldsymbol{S_{IQA}}$, $\boldsymbol{S_{IQB}}$, $\boldsymbol{D_{IQA}}$, $\boldsymbol{D_{IQB}}$	V_{BUS}
$\boldsymbol{S_{IQ11}}$, $\boldsymbol{S_{IQ32}}$, $\boldsymbol{D_{IQ11}}$, $\boldsymbol{D_{IQ32}}$	$¾V_{BUS}$
$\boldsymbol{S_{IQ12}}$, $\boldsymbol{S_{IQ31}}$, $\boldsymbol{D_{IQ12}}$, $\boldsymbol{D_{IQ31}}$	$¼V_{BUS}$
$\boldsymbol{S_{IQ21}}$, $\boldsymbol{S_{IQ22}}$, $\boldsymbol{D_{IQ21}}$, $\boldsymbol{D_{IQ22}}$	$½V_{BUS}$

The maximum blocking voltage of the diodes and switches located in the middle, D_{RP21}, D_{RP22}, D_{IQ21}, D_{IQ22}, and S_{RP21}, S_{RP22}, S_{IQ21}, S_{IQ22}, is $½V_{BUS}$=350V. The blocking voltages at steady state for the devices in the 5L E-Type BTB Converter are summarized in Table 9. Besides the blocking voltage at steady state, we have to take into account the commutation over-voltage Δv that occurs during the commutation. The commutation over-voltage Δv is defined as in (53), where k_R is the coefficient that takes into account the resonance of the DC-bus circuit, L_ξ is the commutation inductance (6), di_{sw}/dt is the device current slope and V_{FR} is the forward recovery voltage of the complementary freewheeling diode.

$$\Delta v = k_R L_\xi \frac{di_{sw}}{dt} + V_{FR} \tag{53}$$

Consequently, the switches and diodes voltage rating are given by the sum of two terms: the maximum blocking voltage at steady state and the commutation over-voltage, as depicted in equation (54).

$$V_{sw} = \overbrace{V_{BL(\max)}}^{STEADY\ STATE} + \overbrace{k_R L_\xi \frac{di_{sw}}{dt} + V_{FR}}^{TRANSIENT} \tag{54}$$

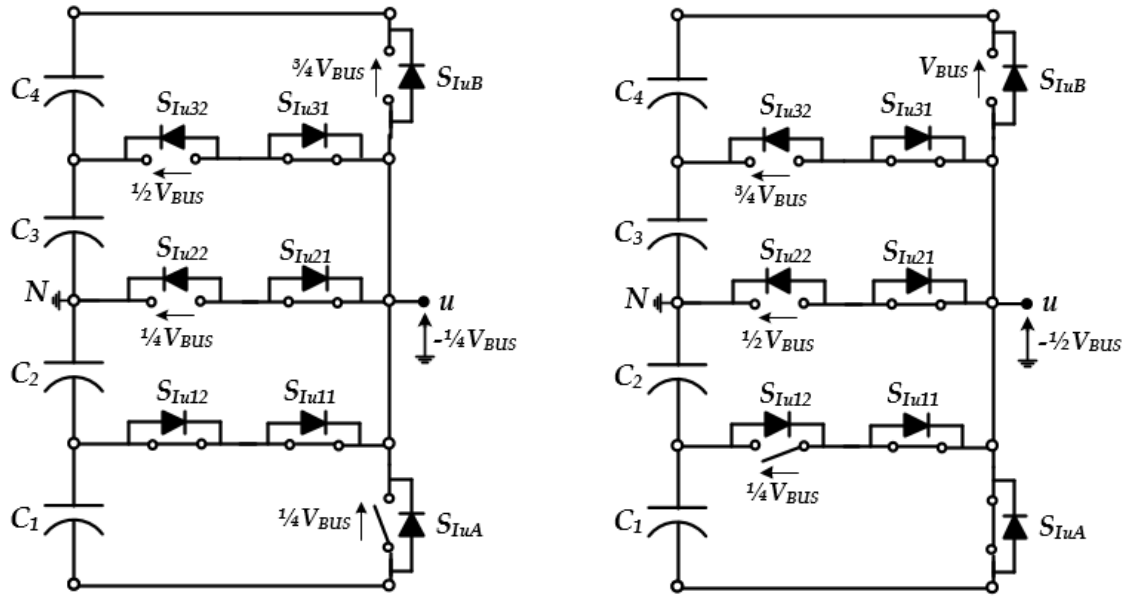
Actually, the equation (54) is valid when the devices works in active switch

mode; whereas when the switch operates in passive switch mode, the equation (54) is not valid.

6.4.1 Passive and Active Switch Mode

When the device is "OFF", the voltage rating is set by the circuit and the commutation over-voltage Δv does not occur; the voltage rating of the switch is equal to the blacking voltage. Let's call this condition passive switch mode (PSM). For example, during the peak negative of the modulating signal the equivalent circuit is shown in Fig. 88 (the modulation scheme will be explained in the next section). The commutation occurs between S_{IuA} and S_{Iu12}. When S_{Iu12} is "ON" (S_{IuA} is "OFF") the output voltage is $-¼V_{BUS}$, the blocking voltage across the switch S_{IuB} is $¾V_{BUS}$. When S_{IuA} is "ON" (S_{Iu12} is "OFF") the output voltage is $-½V_{BUS}$, the blocking voltage across the switch S_{IuB} is V_{BUS}. In both cases the commutation over-voltage Δv is zero. It can be seen that even switches S_{Iu22} and S_{Iu32} operate in PSM.

Active switch mode (ASM) occurs when the current flows through the devices during the commutation. In this case, the voltage rating of the devices is given by equation (54). For example, considering the Fig. 88 the switches S_{IuA} and S_{Iu12} operate in ASM and the commutation over-voltage Δv can occur. It can be noticed that each power device in the 5L E-Type BTB Converter are switched with the blocking voltage at a steady state equal to $¼V_{BUS}$; this means that the commutation over-voltage Δv happen with low blocking voltage at a steady state ($¼V_{BUS}$).



(a) (b)

Fig. 88. Single-phase equivalent circuit diagram of the 5L E-Type Inverter during the peak negative of the modulating signal: a) S_{Iu12} is "ON" and S_{IuA} is "OFF, b) S_{Iu12} is "OFF" and S_{IuA} is "ON.

6.4.2 Few Words about the Devices Technology

Once the voltage rating has been determined, the next step is the selection of the device type and technology according to the voltage rating previously determined. Different switch technologies can be selected to create the 5L E-Type BTB Converter. The use of 1200V IGBTs could be the best solution for the inverter outer switches S_{IQA}, S_{IQB} since they have to sustain the full DC-bus voltage (> V_{BUS}). The diodes placed in the outer leg and in the top-middle leg, D_{RPA}, D_{RPB} and D_{RP11}, D_{RP32}, can be silicon carbide (SiC) devices, due to their attractive characteristic of strongly reduction of the reverse recovery losses. Two switch technologies can be proposed for the middle legs: super-junction MOSFET and IGBTs. In order to reduce the losses, super-junction 650V MOSFET for the switches S_{RP21}, S_{RP22}, and S_{IQ21}, S_{IQ22} could be used. However, the poor reverse recovery characteristics of the internal body diode of the super-junction MOSFET makes them difficult to be used in the 5L E-Type Inverter. Thus, the switches situated in the middle leg rectifier could be super-junction MOSFET and the switches placed in the middle leg inverter should be Si-IGBT with Si or SiC FWD.

Finally, we can choose two different semiconductor's technologies in the bottom-middle and top-middle leg given two different switch voltage ratings, $¼V_{BUS}$ and $¾V_{BUS}$. The switches having $¼V_{BUS}$ voltage ratings, S_{RP12}, S_{RP31}, S_{IQ12} and S_{IQ31}, 250 V OptiMOS™ technology could be the best choice to improve the overall efficiency. The switches having $¾V_{BUS}$ voltage ratings S_{IQ11} and S_{IQ32}, 650V IGBT can be the switch of choice. The preferred semiconductor's technology and switches voltage ratings of the 5L BTB Converter have been summarized in Table 10.

Table 10. The semiconductor's technology of the 5L E-Type BTB Converter.

Devices	**Rated Voltage [V]**	**Technology**
5L E-Type Rectifier		
D_{RPA}, D_{RPB}, D_{RP11}, S_{RP32}	1200	SiC Diode
S_{RP12}, D_{RP31}	250	OptiMOS™
S_{RP21}, S_{RP22}	650	CoolMOS™
5L E-Type Inverter		
S_{IQA}, S_{IQB}, S_{IQ11}, S_{IQ32}	1200	Si-IGBT
S_{IQ12}, S_{IQ31}	250	OptiMOS™
S_{IQ21}, S_{IQ22}	650	Si-IGBT

6.4.3 Improving the Voltage Rating Devices of the 5L E-Type BTB Converter

Multi-level topologies have been conceived to use devices like IGBTs in traction applications in place to thyristors (SCR) and GTOs during 80's [153]. Afterwards, multilevel topologies have also been used in industrial applications given the excellent benefits such as the use of power devices with a low voltage rating. Thus, the power semiconductors must withstand only reduced DC-bus voltages. To this purpose, more power devices have been connected in series and/or in parallel to create a specific multi-level topology. In other words, if the devices have to withstand the total DC-bus voltage, we can use more switches in series connection. The devices in series connection are crossed by the same current flow, this means that the conduction losses would increase. As a result,

we are improving the switches voltage rating; however, on the other hand, we are getting worse the conduction losses. We have seen in the previous section, that the more stressed devices in the 5L E-Type BTB Topology are located in the outer, bottom-middle and top-middle leg, D_{RPA}, D_{RPB} and S_{IQA}, S_{IQB}, Fig. 89a. Can we do something to improve the 5L E-Type BTB Converter? The answer is yes! We can make a small modification in the 5L E-Type BTB Converter using two series connection switches in order to obtain a great improvement from the point of view of the switches voltage rating.

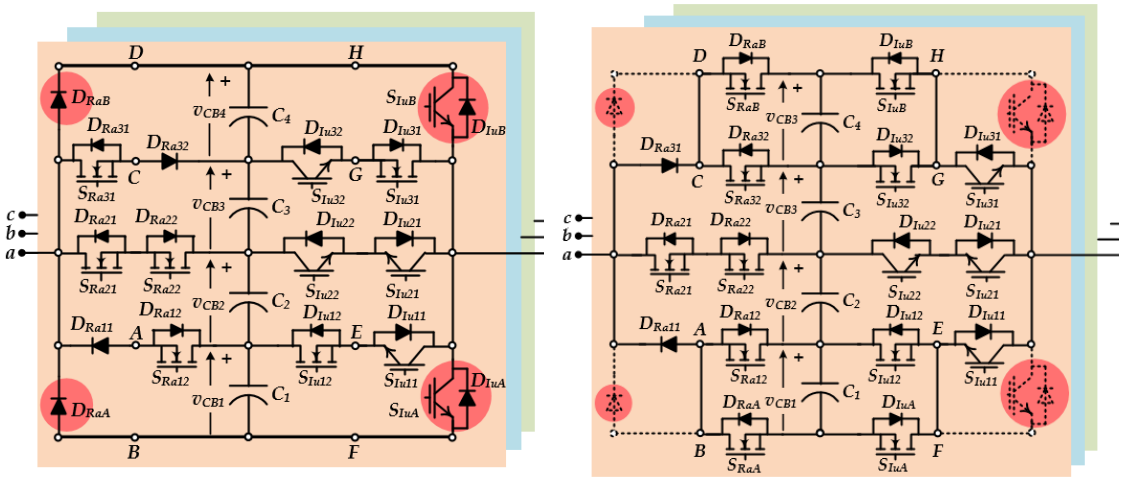


Fig. 89. 5L E-Type BTB Converter: a) High switches voltage rating, b) topology change.

The main idea is to swap the devices in the top-middle leg, $S_{IQ31} \leftrightarrow S_{IQ32}$ and $S_{RP31} \leftrightarrow D_{RP32}$, and insert a short circuit between the points A-B, C-D, E-F and GH, Fig. 89b. Given the diodes $D_{RaA} \leftrightarrow D_{Ra11}$, $D_{RaB} \leftrightarrow D_{Ra31}$ and IGBTs $S_{IuA} \leftrightarrow S_{Iu11}$, $S_{IuB} \leftrightarrow S_{Iu31}$ have the same function, the diodes D_{RPA} and D_{RPB} and the IGBTs S_{IQA} and S_{IQB} are removed and new devices are inserted into outer legs (S_{RPA}, S_{RPB}, S_{IuA}, S_{IuB}, see Fig. 89b). The new converter called New 5L E-Type BTB Converter (N5L E-Type BTB Converter) can be drawn as in Fig. 90. The N5L E-Type BTB Converter presents the same input/output-to-neutral switching voltage, equations (15) and (51), and the same characteristic shown in the previous configuration of Fig. 42.

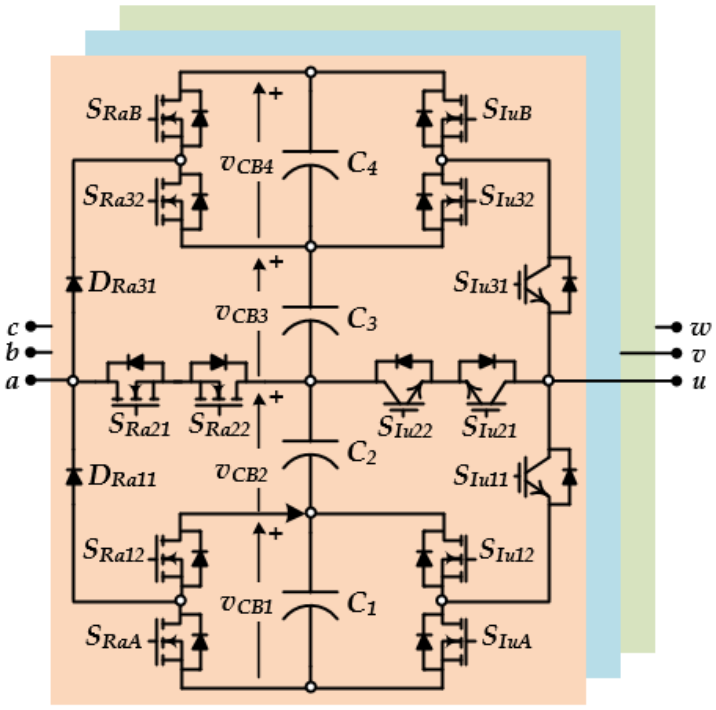


Fig. 90. New 5L E-Type BTB Converter.

The voltage stress of the switches S_{RPA}, S_{RPB}, S_{IQA} and S_{IQB} is reduced. Fig. 91 and Fig. 92 show the blocking voltages of the switches in the N5L E-Type BTB Converter.

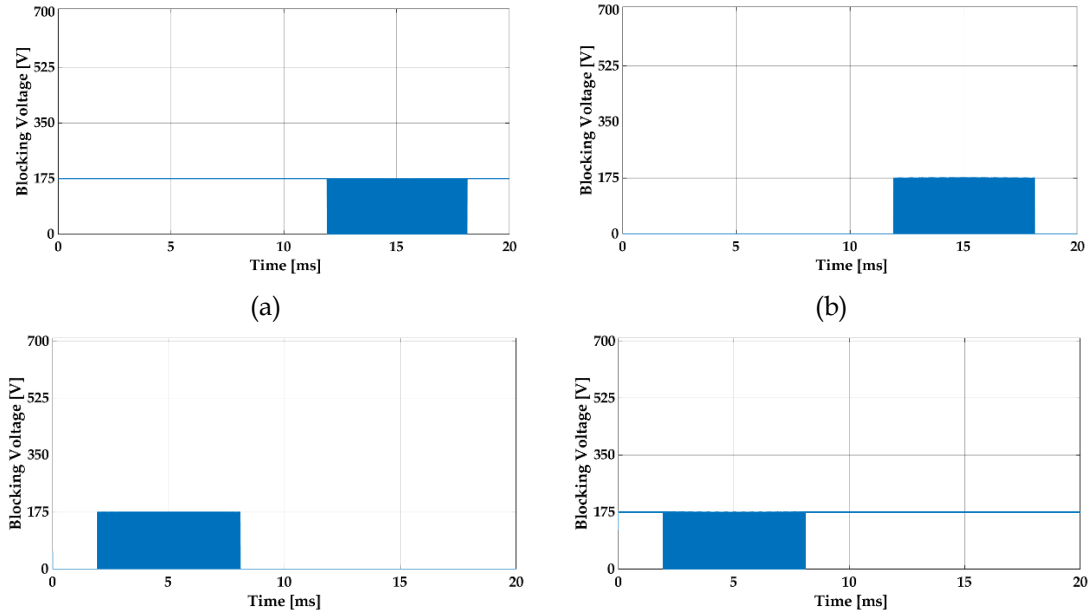


Fig. 91. Steady state blocking voltages of the switches in the N5L E-Type BTB Converter: a) S_{RPA}, S_{IQA}, D_{RPA} and D_{IQA}, b) S_{RP12}, S_{IQ12}, D_{RP12} and D_{IQ12}, c) S_{RP32}, S_{IQ32}, D_{RP32} and D_{IQ32}, d) S_{RPB}, S_{IQB}, D_{RPB} and D_{IQB}.

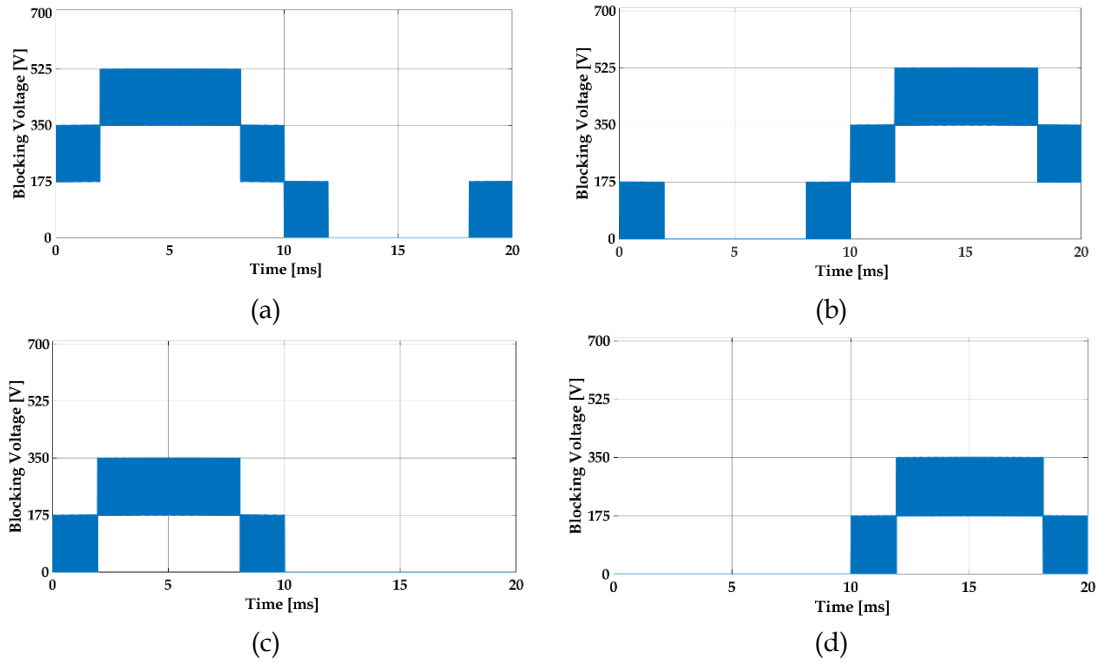


Fig. 92. Steady state blocking voltages of the switches in the N5L E-Type BTB Converter: a) D_{RP11}, D_{IQ11} and S_{IQ11}, b) D_{RP31}, D_{IQ31} and S_{IQ31}, c) S_{RP21}, S_{IQ21}, D_{RP21} and D_{IQ21}, d) S_{RP22}, S_{IQ22}, D_{RP22} and D_{IQ22}.

The maximum blocking voltage across S_{RPA}, S_{RPB}, S_{IQA} and S_{IQB} is $¼V_{BUS}$. The maximum voltage stress is $¾V_{BUS}$ for devices D_{RP31}, D_{RP11}, S_{IQ31} and S_{IQ11}. As mentioned for the previous 5L E-Type BTB Topology even in the New 5L E-Type BTB Converter all power semiconductors are switched with the blocking voltage at a steady state equal to $¼V_{BUS}$. Power devices D_{RP31}, D_{RP11}, S_{IQ31} and S_{IQ11} operate in PSM, as a consequence commutation over-voltage Δv does not occur and the voltage rating of the switch is equal to the blacking voltage ($¾V_{BUS}$).

Furthermore, as it will be explained later, the New 5L E-Type BTB Converter shows a short commutation loop for high modulation index. In other words, only two power devices in the rectifier side, S_{RPB}, S_{RP32} (or S_{RPA}, S_{RP12}), and two power devices in the inverter side, S_{IQB}, S_{IQ32} (or S_{IQA}, S_{IQ12}), are involved in the commutation loop during the positive (or negative) peak of the modulation index. As a consequence, we have lower commutation inductance, which results in low commutation over-voltage Δv. Thus, the 250 V OptiMOS could be used for the switches S_{RPA}, S_{RPB}, S_{IQA} and $S_{IQB,}$ due to the low voltage ratings. The preferred semiconductor's technology and switches voltage ratings of the N5L

BTB Converter have been summarized in Table 11.

Table 11. The semiconductor's technology of the N5L E-Type BTB Converter.		
Devices	**Rated Voltage [V]**	**Technology**
5L E-Type Rectifier		
D_{RP11}, D_{RP31}	650	SiC Diode
S_{RPA}, S_{RPB}, S_{RP12}, S_{RP32}	250	OptiMOS™
S_{RP21}, S_{RP22}	650	CoolMOS™
5L E-Type Inverter		
S_{IQ11}, S_{IQ31}	650	Si-IGBT
S_{IQA}, S_{IQB}, S_{IQ12}, S_{IQ32}	250	OptiMOS™
S_{IQ21}, S_{IQ22}	650	Si-IGBT

6.5 Modulation Scheme of the N5L E-Type BTB Converter

The N5L E-Type Converter is controlled using the multilevel-PWM. In particular, the phase disposition carrier control technique has been selected for the proposed topology [155]. The modulation scheme uses four different carriers; all the carrier signals, c_{t1}, c_{t2}, c_{t3} and c_{t4}, have the same amplitude and frequency, and are in phase with each other, Fig. 93. It can be seen that $A_{n,car}$ is the amplitude of the carriers and $m_{n,car}$ is the offset of the carriers (with n=1,2,3,4). In this case, $A_{1,car}=A_{2,car}=A_{3,car}=A_{4,car}=½$ and $m_{1,car}=-¾$, $m_{2,car}=-¼$, $m_{3,car}=¼$, $m_{4,car}=¾$. Each carrier controls two different power devices in opposite phase as listed in Table 12. The modulating signals of the 5L E-Type Rectifier and 5L E-Type Inverter, $m_{P,R}(t)$ and $m_{Q,I}(t)$, depend on the type of PWM modulation that is chosen. A pure sinusoidal modulating signal, $m_{P,R}(t)$ (or $m_{Q,I}(t)$), is shown in Fig. 93 for the sake of simplicity. The equations for the sinusoidal PWM modulation techniques are summarized in (55) and (56), where $M_{0,R}$ and $M_{0,I}$ are the rectifier and inverter modulation depth, $-1 \leq M_{0,R} \leq 1$, $-1 \leq M_{0,I} \leq 1$, established in (9) and (47), ω_{IN} and ω_{OUT} are the input and output frequency and ψ is the input to output voltage displacement.

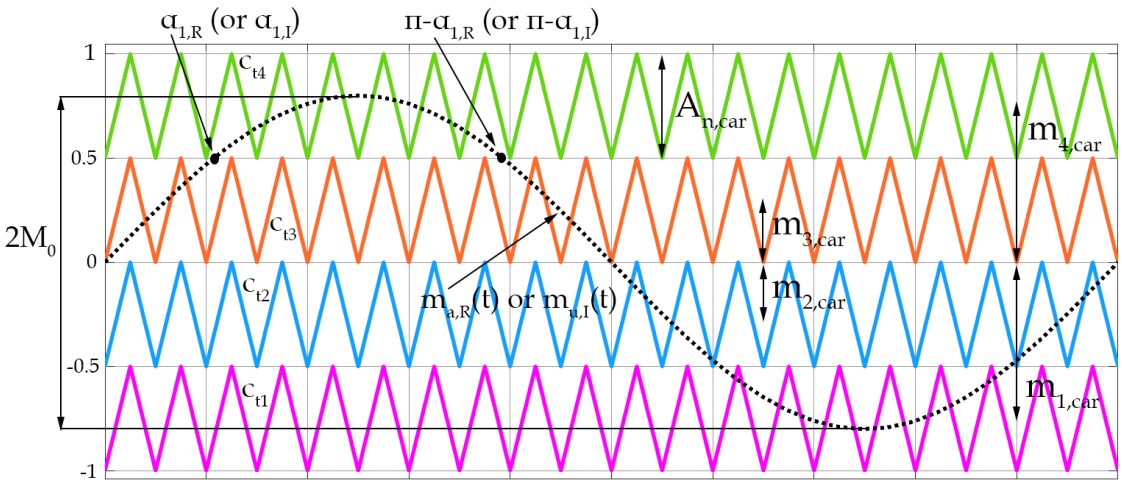


Fig. 93. Modulating scheme of the N5L E-Type BTB Converter.

Table 12. Carriers versus power devices.

Carriers	Rectifier Devices	Inverter Devices
c_{t1}	S_{RPA}, S_{RP12}	S_{IQA}, S_{IQ12}
c_{t2}	S_{RP22}	S_{IQ22}, S_{IQ11}
c_{t3}	S_{RP21}	S_{IQ31}, S_{IQ21}
c_{t4}	S_{RPB}, S_{RP32}	S_{IQB}, S_{IQ32}

$$\begin{aligned} m_{a,R}(t) &= M_{0,R}\sin(\omega_{IN}t) \\ m_{b,R}(t) &= M_{0,R}\sin\left(\omega_{IN}t-\frac{2\pi}{3}\right) \\ m_{c,R}(t) &= M_{0,R}\sin\left(\omega_{IN}t+\frac{2\pi}{3}\right) \end{aligned} \tag{55}$$

$$\begin{aligned} m_{u,I}(t) &= M_{0,I}\sin(\omega_{OUT}t-\psi) \\ m_{v,I}(t) &= M_{0,I}\sin\left(\omega_{OUT}t-\frac{2\pi}{3}-\psi\right) \\ m_{w,I}(t) &= M_{0,I}\sin\left(\omega_{OUT}t+\frac{2\pi}{3}-\psi\right) \end{aligned} \tag{56}$$

Considering the single-phase "*a*" and "*u*", the modulating signal $m_{a,R}(t)$ and $m_{u,I}(t)$ reach a 0.5 value (see Fig. 93) with an angle given by the equations (57) and (58).

$$\begin{cases} \alpha_{1,R} = \arcsin\left(\dfrac{1}{2M_{0,R}}\right) \\ \alpha_{2,R} = \pi - \alpha_1 \end{cases} \tag{57}$$

$$\begin{cases} \alpha_{1,I} = \psi + \arcsin\left(\dfrac{1}{2M_{0,I}}\right) \\ \alpha_{2,I} = \pi - \alpha_1 \end{cases} \tag{58}$$

The devices switching states depend on the modulation index $m_{P,R}(t)$ and $m_{Q,I}(t)$;

in particular, we can distinguish 4 regions both for the rectifier -1≤$m_{P,R}$(t)<-0.5, -0.5≤$m_{P,R}$(t)<0, 0≤$m_{P,R}$(t)≤0.5, 0.5<$m_{P,R}$(t)≤1 and for the inverter -1≤$m_{Q,I}$(t)<-0.5, -0.5≤$m_{Q,I}$(t)<0, 0≤$m_{Q,I}$(t)≤0.5, 0.5<$m_{Q,I}$(t)≤1. According to this, Table 13 and Table 14 illustrates the switches states versus modulation index $m_{P,R}(t)$ and $m_{Q,I}(t)$.

Table 13. 5L E-Type Rectifier Switching Conditions.

	-1≤$m_{P,R}$(t)<-0.5	-0.5≤$m_{P,R}$(t)<0	0≤$m_{P,R}$(t)≤0.5	0.5<$m_{P,R}$(t)≤1
S_{RPA}	OFF if $m_{P,R}$(t)>c_{t1}(t) ON if $m_{P,R}$(t)<c_{t1}(t)	OFF	OFF	OFF
S_{RP12}	ON if $m_{P,R}$(t)> c_{t1}(t) OFF if $m_{P,R}$(t)<c_{t1}(t)	ON	ON	ON
S_{RP22}	OFF	ON if $m_{P,R}$(t)>c_{t2}(t) OFF if $m_{P,R}$(t)<c_{t2}(t)	ON	ON
S_{RP21}	ON	ON	ON if c_{t3}(t)>$m_{P,R}$(t) OFF if c_{t3}(t)<$m_{P,R}$(t)	OFF
S_{RP32}	ON	ON	ON	ON if c_{t4}(t)>$m_{P,R}$(t) OFF if c_{t4}(t)<$m_{P,R}$(t)
S_{RPB}	OFF	OFF	OFF	OFF if c_{t4}(t)>$m_{P,R}$(t) ON if c_{t4}(t)<$m_{P,R}$(t)

Table 14. 5L E-Type Inverter Switching Conditions.

	-1≤$m_{Q,I}$(t)<-0.5	-0.5≤$m_{Q,I}$(t)<0	0≤$m_{Q,I}$(t)≤0.5	0.5<$m_{Q,I}$(t)≤1
S_{IQA}	OFF if $m_{Q,I}$(t)>c_{t1}(t) ON if $m_{Q,I}$(t)<c_{t1}(t)	OFF	OFF	OFF
S_{IQ11}	ON	OFF if $m_{Q,I}$(t)>c_{t2}(t) ON if $m_{Q,I}$(t)<c_{t2}(t)	OFF	OFF
S_{IQ12}	ON if $m_{Q,I}$(t)>c_{t1}(t) OFF if $m_{Q,I}$(t)<c_{t1}(t)	ON	ON	ON
S_{IQ21}	ON	ON	ON if c_{t3}(t)>$m_{Q,I}$(t) OFF if c_{t3}(t)<$m_{Q,I}$(t)	OFF
S_{IQ22}	OFF	ON if $m_{Q,I}$(t)>c_{t2}(t) OFF if $m_{Q,I}$(t)<c_{t2}(t)	ON	ON
S_{IQ32}	ON	ON	ON	ON if c_{t4}(t)>$m_{Q,I}$(t) OFF if c_{t4}(t)<$m_{Q,I}$(t)
S_{IQ31}	OFF	OFF	OFF if c_{t3}(t)>$m_{Q,I}$(t) ON if c_{t3}(t)<$m_{Q,I}$(t)	ON
S_{IQB}	OFF	OFF	OFF	OFF if c_{t4}(t)>$m_{Q,I}$(t) ON if c_{t4}(t)<$m_{Q,I}$(t)(t)

6.5.1 Switching Duty Cycle of the N5L E-Type BTB Converter

Using a sinusoidal multi-level PWM modulation techniques for the N5L E-

Type BTB Converter, the modulating signals $m_{P,R}(t)$ and $m_{Q,I}(t)$, and the switching conditions of the devices are defined in the previous section (equations (55), (56) and Table 13 and Table 14). According to equations (55), (56) and Fig. 90, the duty cycle of the devices can be defined as in (59) and (60), where the amplitude of the carriers $A_{n,car}$ and the offset of the carrier $m_{n,car}$ (with n=1,2,3,4) are shown in Fig. 93.

$$d_{RP}(t)=\frac{1}{A_{n,car}}\left(\left(\frac{A_{n,car}}{2}-m_{n,car}\right)+m_{P,R}(\mathrm{t})\right) \tag{59}$$

$$d_{IQ}(t)=\frac{1}{A_{n,car}}\left(\left(\frac{A_{n,car}}{2}-m_{n,car}\right)+m_{Q,I}(\mathrm{t})\right) \tag{60}$$

Considering the single-phase "*a*" and "*u*", substituting equations (55), (56) into (59) and (60), the duty cycle for each power semiconductor in both the rectifier and the inverter have been obtained in (61)-(74), where $\theta_R=\omega_{IN}t$ and $\theta_I=\omega_{OUT}t-\psi$.

$$d_{S_{RaA}}(t)=\begin{cases}0 & \theta_R\in[0,\pi],\ \theta_R\in[\pi,\pi+\alpha_1],\ \theta_R\in[2\pi-\alpha_1,2\pi]\\ -1-2M_{0,R}\sin(\theta_R) & \theta_R\in[\pi,2\pi-\alpha_1]\end{cases} \tag{61}$$

$$d_{S_{Ra12}}(t)=\begin{cases}1 & \theta_R\in[0,\pi],\ \theta_R\in[\pi,\pi+\alpha_1],\ \theta_R\in[2\pi-\alpha_1,2\pi]\\ 2\left[1+M_{0,R}\sin(\theta_R)\right] & \theta_R\in[\pi+\alpha_1,2\pi-\alpha_1]\end{cases} \tag{62}$$

$$d_{S_{Ra21}}(t)=\begin{cases}1-2M_{0,R}\sin(\theta_R) & \theta_R\in[0,\alpha_1],\ \theta_R\in[\pi-\alpha_1,\pi]\\ 0 & \theta_R\in[\alpha_1,\pi-\alpha_1]\\ 1 & \theta_R\in[\pi,2\pi]\end{cases} \tag{63}$$

$$d_{S_{Ra22}}(t)=\begin{cases}1 & \theta_R\in[0,\pi]\\ 1+2M_{0,R}\sin(\theta_R) & \theta_R\in[\pi,\pi+\alpha_1],\ \theta_R\in[2\pi-\alpha_1,2\pi]\\ 0 & \theta_R\in[\pi+\alpha_1,2\pi-\alpha_1]\end{cases} \tag{64}$$

$$d_{S_{Ra32}}(t)=\begin{cases}1 & \theta_R\in[0,\alpha_1],\ \theta_R\in[\pi-\alpha_1,\pi],\ \theta_R\in[\pi,2\pi]\\ 2\left[1-M_{0,R}\sin(\theta_R)\right] & \theta_R\in[\alpha_1,\pi-\alpha_1]\end{cases} \tag{65}$$

$$d_{S_{RaB}}(t)=\begin{cases}-1+2M_{0,R}\sin(\theta_R) & [\alpha_1,\pi-\alpha_1]\\ 0 & \theta_R\in[0,\alpha_1],\ \theta_R\in[\pi-\alpha_1,\pi],\ \theta_R\in[\pi,2\pi]\end{cases} \tag{66}$$

$$d_{S_{IuA}}(t)=\begin{cases}0 & \theta_I\in[0,\pi],\ \theta_I\in[\pi,\alpha_1+\pi],\ \theta_I\in[2\pi-\alpha_1,2\pi]\\ -1-2M_{0,I}\sin(\theta_I) & \theta_I\in[\alpha_1+\pi,2\pi-\alpha_1]\end{cases} \tag{67}$$

$$d_{S_{Iu12}}(t)=\begin{cases}1 & \theta_I\in[0,\pi],\ \theta_I\in[\pi,\alpha_1+\pi],\ \theta_I\in[2\pi-\alpha_1,2\pi]\\ 2\left[1+M_{0,I}\sin(\theta_I)\right] & \theta_I\in[\alpha_1+\pi,2\pi-\alpha_1]\end{cases} \quad (68)$$

$$d_{S_{Iu11}}(t)=\begin{cases}0 & \theta_I\in[0,\pi]\\ -2M_{0,I}\sin(\theta_I) & \theta_I\in[\pi,\alpha_1+\pi],\ \theta_I\in[2\pi-\alpha_1,2\pi]\\ 1 & \theta_I\in[\alpha_1+\pi,2\pi-\alpha_1]\end{cases} \quad (69)$$

$$d_{S_{Iu21}}(t)=\begin{cases}1-2M_{0,I}\sin(\theta_I) & \theta_I\in[0,\alpha_1],\ \theta_I\in[\pi-\alpha_1,\pi]\\ 0 & \theta_I\in[\alpha_1,\pi-\alpha_1]\\ 1 & \theta_I\in[\pi,2\pi]\end{cases} \quad (70)$$

$$d_{S_{Iu22}}(t)=\begin{cases}1 & \theta_I\in[0,\pi]\\ 1+2M_{0,I}\sin(\theta_I) & \theta_I\in[\pi,\alpha_1+\pi],\ \theta_I\in[2\pi-\alpha_1,2\pi]\\ 0 & \theta_I\in[\alpha_1+\pi,2\pi-\alpha_1]\end{cases} \quad (71)$$

$$d_{S_{Iu31}}(t)=\begin{cases}2M_{0,I}\sin(\theta_I) & \theta_I\in[0,\alpha_1],\ \theta_I\in[\pi-\alpha_1,\pi]\\ 1 & \theta_I\in[\alpha_1,\pi-\alpha_1]\\ 0 & \theta_I\in[\pi,2\pi]\end{cases} \quad (72)$$

$$d_{S_{Iu32}}(t)=\begin{cases}1 & \theta_I\in[0,\alpha_1],\ \theta_I\in[\pi-\alpha_1,\pi],\ \theta_I\in[\pi,2\pi]\\ 2\left[1-M_{0,I}\sin(\theta_I)\right] & \theta_I\in[\alpha_1,\pi-\alpha_1]\end{cases} \quad (73)$$

$$d_{S_{IuB}}(t)=\begin{cases}0 & \theta_I\in[0,\alpha_1],\ \theta_I\in[\pi-\alpha_1,\pi],\ \theta_I\in[\pi,2\pi]\\ -1+2M_0\sin(\theta_I) & \theta_I\in[\alpha_1,\pi-\alpha_1]\end{cases} \quad (74)$$

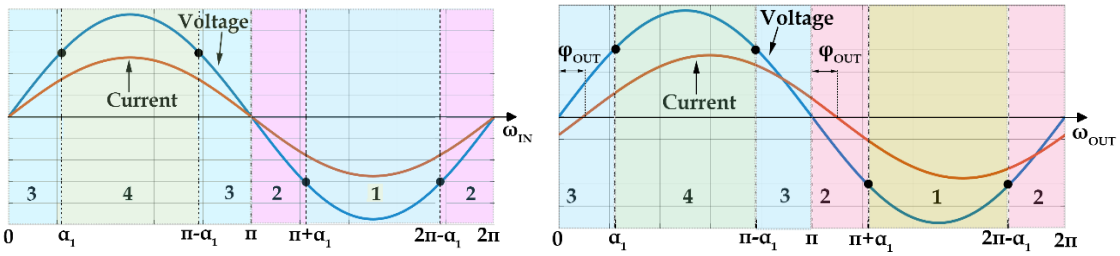
6.5.2 Commutation Loops and Current Paths of the N5L E-Type BTB Converter

In this section, we will determine the current paths in a fundamental period based on the operating status of the switches in the N5L E-Type BTB Converter. Let us consider a single-phase "*a*" and "*u*", the rectifier's PF close to one, the inverter's PF non-unitary and ψ is supposed equal to zero. The input and output phase current are defined as in (75) and (76), where ω_{IN} and ω_{OUT} are the input and output frequency, φ_{OUT} is the phase displacement between the phase output voltage and output current. In these conditions, the 5L E-Type Rectifier works in two areas, 1) and 2) $u_a<0$, $i_a<0$ and 3) and 4) $u_a>0$, $i_a>0$; the 5L E-Type Inverter works in four areas, 1) $u_u<0$, $i_u<0$; 2) $u_u<0$, current can be both $i_u>0$ and $i_u<0$; 3)

u_u>0, current can be both i_u>0 and i_u<0; 4) u_u>0, i_u>0, as shown Fig. 94. As previously discussed, the devices switching states are a function of the modulation index.

$$\begin{cases} i_a(t) = \sqrt{2} I_{IN} \sin(\omega_{IN} t) \\ i_b(t) = \sqrt{2} I_{IN} \sin\left(\omega_{IN} t - \frac{2}{3}\pi\right) \\ i_c(t) = \sqrt{2} I_{IN} \sin\left(\omega_{IN} t - \frac{4}{3}\pi\right) \end{cases} \quad (75)$$

$$\begin{cases} i_u(t) = \sqrt{2} I_{OUT} \sin(\omega_{OUT} t - \varphi_{OUT}) \\ i_v(t) = \sqrt{2} I_{OUT} \sin\left(\omega_{OUT} t - \frac{2}{3}\pi - \varphi_{OUT}\right) \\ i_w(t) = \sqrt{2} I_{OUT} \sin\left(\omega_{OUT} t - \frac{4}{3}\pi - \varphi_{OUT}\right) \end{cases} \quad (76)$$



(a) (b)

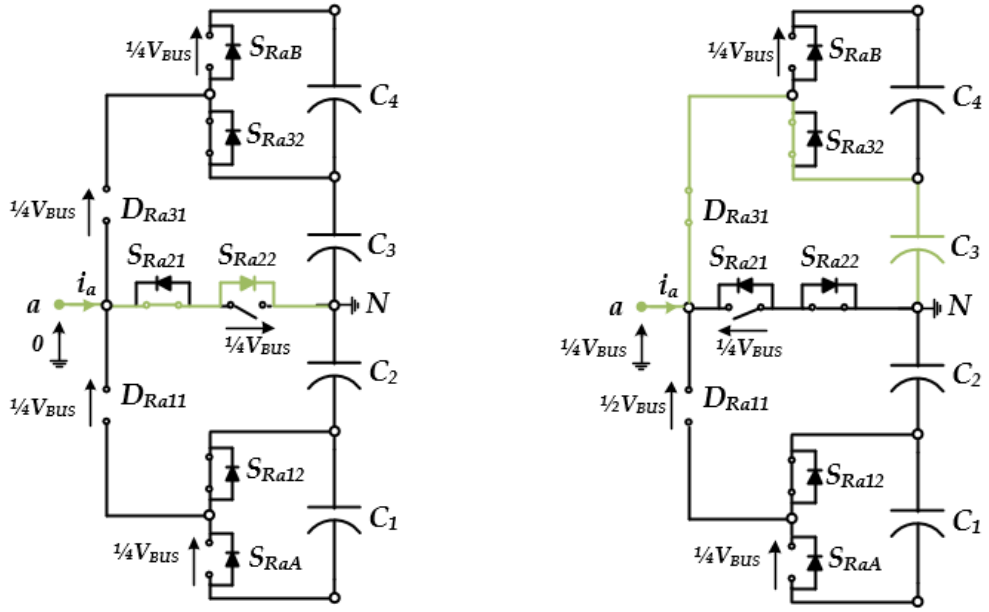
Fig. 94. Operating areas: a) 5L E-Type Rectifier, b) 5L E-Type Inverter.

When $0 \le \omega_{IN} \le \alpha_1$ and $0 \le \omega_{OUT} \le \varphi_{OUT}$, the rectifier and inverter modulation indexes are within 0 and 0.5 ($0 \le m_{P,R}(t) \le 0.5$ and $0 \le m_{Q,I}(t) \le 0.5$); the 5L E-Type Rectifier operate in area 3 and the 5L E-Type Inverter works in area 3 (i_a<0). Considering the switches notation in Fig. 95, the current paths, the devices blocking voltage and the input/output-to-neutral switching voltage $u_{a(sw)}$ and $u_{u(sw)}$ are depicted in Fig. 96 and Fig. 97.

(a) (b) (c)

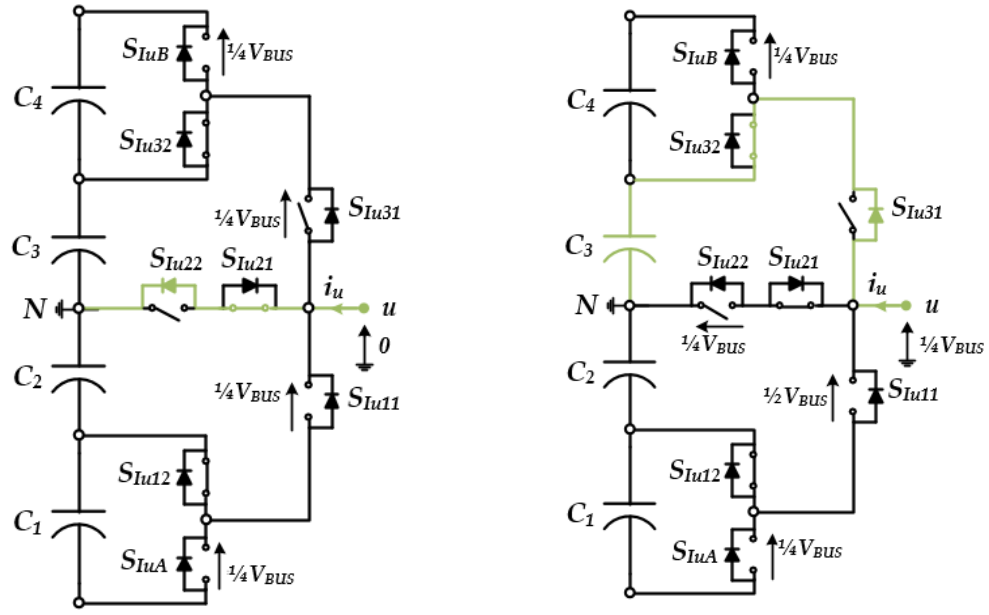
Fig. 95. Switches notation: a) commutation switch, b) close switch, c) open switch.

As soon as the inverter's current is positive, the current paths are depicted in Fig. 98. When $\alpha_1 < \omega_{IN} \le \pi - \alpha_1$ and $\varphi_{OUT} < \omega_{OUT} \le \pi - \alpha_1$, the rectifier and the inverter modulation indexes are $0.5 < m_{P,R}(t) \le 1$ and $0.5 < m_{Q,I}(t) \le 1$; the current paths changes as it is shown in Fig. 99 and Fig. 100. Fig. 99 and Fig. 100 shows the devices blocking voltage and the input/output-to-neutral switching voltage $u_{a(sw)}$ and $u_{u(sw)}$.



(a) (b)

Fig. 96. Current path Rectifier: a) $u_{a(sw)}$=0 V, b) $u_{a(sw)}$=¼V_{BUS} V. Area 3, 0≤ω_{IN} ≤α_1 & π-α_1≤ω_{IN}≤π and 0≤$m_{P,R}$(t)≤0.5.



(a) (b)

Fig. 97. Current path Inverter: a) $u_{u(sw)}$=0 V, b) $u_{u(sw)}$=¼V_{BUS} V. Area 3 with negative current, 0≤φ_{OUT}≤φ_{OUT} and 0≤$m_{Q,I}$(t)≤0.5.

When π-α_1<ω_{IN}≤π, π-α_1<ω_{OUT}≤π, 0≤$m_{P,R}$(t)≤0.5 and 0≤$m_{Q,I}$(t)≤0.5 (area 3 with i_u>0), the current paths are the same shown in Fig. 96 and Fig. 98. Afterwards, the rectifier voltage is negative and the rectifier's current is negative, whereas the inverter's current is positive.

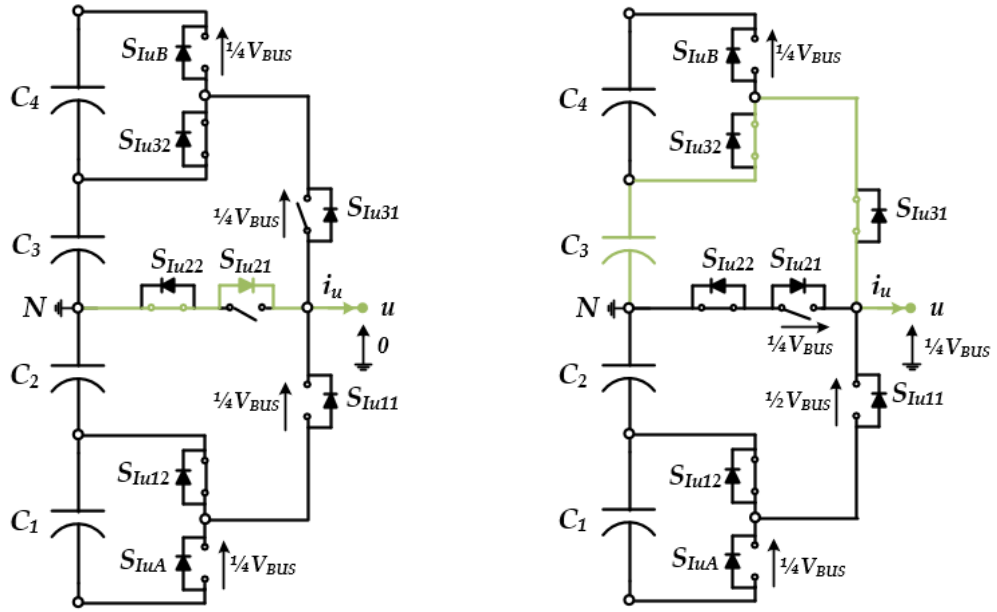


Fig. 98. Current path Inverter: a) $u_{u(sw)}$=0 V, b) $u_{u(sw)}$=¼V_{BUS} V. Area 3 with positive current, $\varphi_{OUT}\leq\omega_{OUT}\leq\alpha_1$ & $\pi-\alpha_1\leq\omega_{OUT}\leq\pi$ and $0\leq m_{Q,I}(t)\leq 0.5$.

Thus, the 5L E-Type Rectifier and Inverter work in area 2. In area 2 ω_{IN} is $\pi<\omega_{IN}\leq\pi+\alpha_1$ and ω_{OUT} is $\pi<\omega_{OUT}\leq\pi+\varphi_{OUT}$, the rectifier and the inverter modulation indexes are $-0.5\leq m_{P,R}(t)<0$ and $-0.5\leq m_{Q,I}(t)<0$.

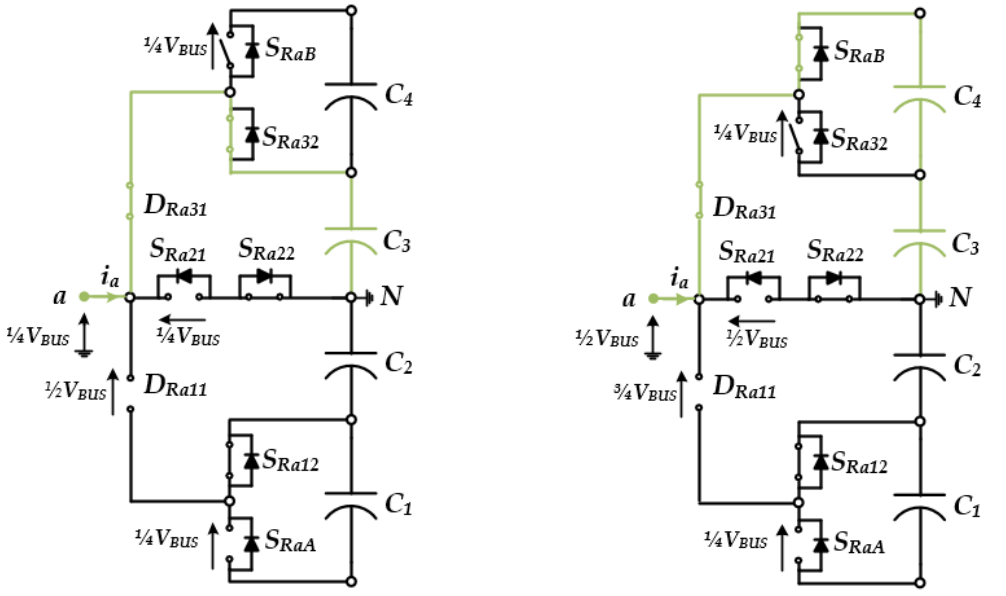


Fig. 99. Current path Rectifier: a) $u_{a(sw)}$=¼V_{BUS} V, b) $u_{a(sw)}$= ½V_{BUS} V. Area 4, $\alpha_1<\omega_{IN}\leq\pi-\alpha_1$, $0.5<m_{P,R}(t)\leq 1$.

In these areas, the current paths are shown in Fig. 101, Fig. 102. The input/output-to-neutral switching voltage $u_{a(sw)}$ and $u_{u(sw)}$ change from 0 V to -

¼V_{BUS}. For a given time, the inverter's current is negative and the 5L E-Type Inverter operates in area 2 ($\omega_{OUT} > \varphi_{OUT}$).

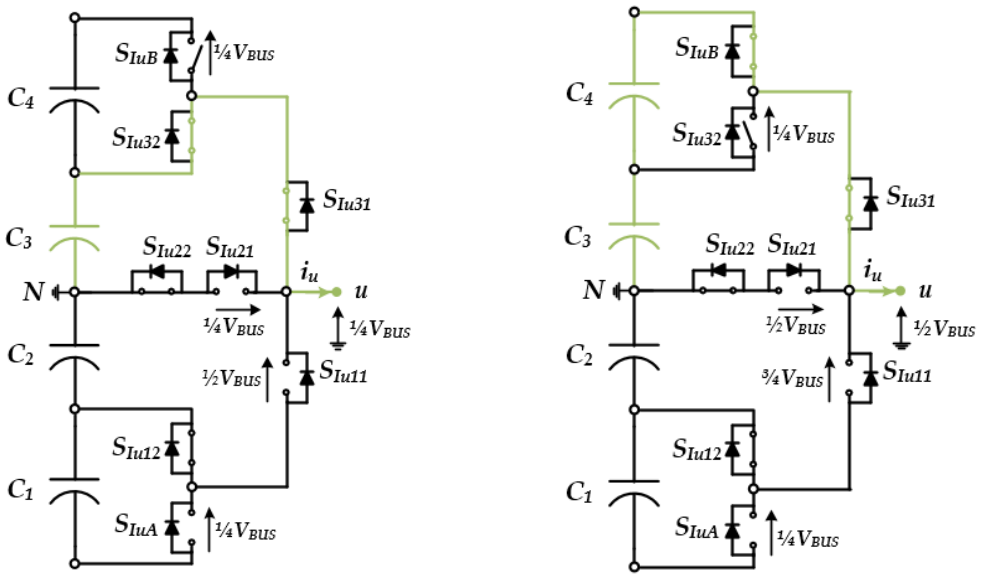


Fig. 100. Current path Inverter: a) $u_{u(sw)}$=¼V_{BUS} V, b) $u_{u(sw)}$= ½V_{BUS} V. Area 4, $\alpha_1 < \omega_{OUT} \leq \pi - \alpha_1$, $0.5 < m_{Q,I}(t) \leq 1$.

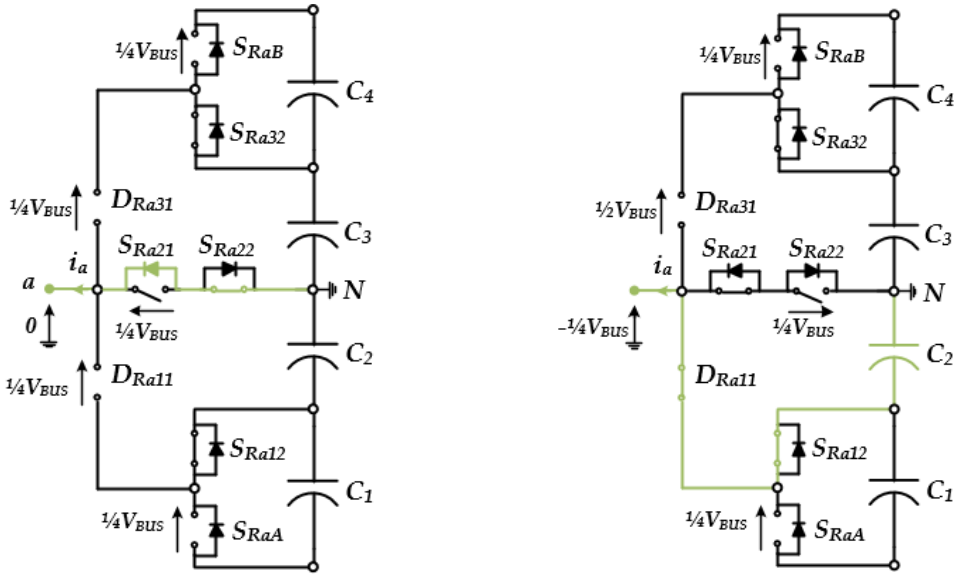


Fig. 101. Current path Rectifier: a) $u_{a(sw)}$=0 V, b) $u_{a(sw)}$=-¼V_{BUS} V. Area 2, $\pi < \omega_{IN} \leq \pi + \alpha_1$ & $2\pi - \alpha_1 < \omega_{IN} \leq 2\pi$ and $-0.5 \leq m_{P,R}(t) < 0$.

The current paths are depicted in Fig. 103. When $\pi + \alpha_1 < \omega_{IN} \leq 2\pi - \alpha_1$ and $\pi + \alpha_1 < \omega_{OUT} \leq 2\pi - \alpha_1$, the rectifier and the inverter modulation indexes are $-1 \leq m_{P,R}(t) < -0.5$ and $-1 \leq m_{Q,I}(t) < -0.5$; the current path changes as in Fig. 104 and Fig. 105. The input/output-to-neutral switching voltages $u_{a(sw)}$ and $u_{u(sw)}$ change

from -¼V_{BUS} V to -½V_{BUS}. Finally, when 2π-α_1<ω_{IN}≤2π and 2π-α_1<ω_{OUT}≤2π, the rectifier and the inverter modulation indexes are -0.5≤$m_{P,R}$(t)<0 and -0.5≤$m_{Q,I}$(t)<0 (area 2 with i_u<0); the current paths are the same as shown in Fig. 101 and Fig. 103. It can be noticed that this analysis is valid as long as φ_{OUT}≤α_1.

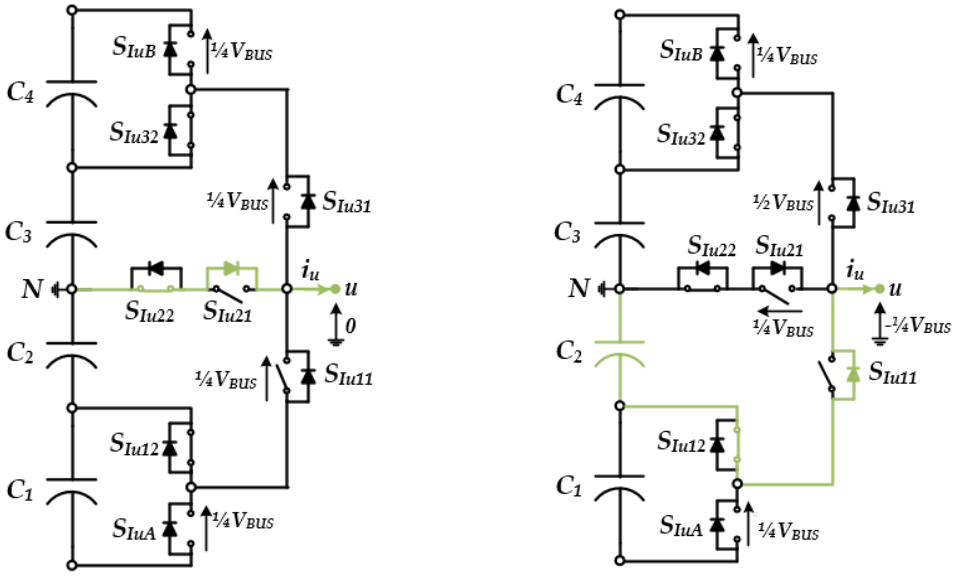


Fig. 102. Current path Inverter: a) $u_{u(sw)}$=0 V, b) $u_{u(sw)}$=-¼V_{BUS} V. Area 2 with positive current, π<ω_{OUT}≤π+φ_{OUT} and -0.5≤$m_{Q,I}$(t)<0.

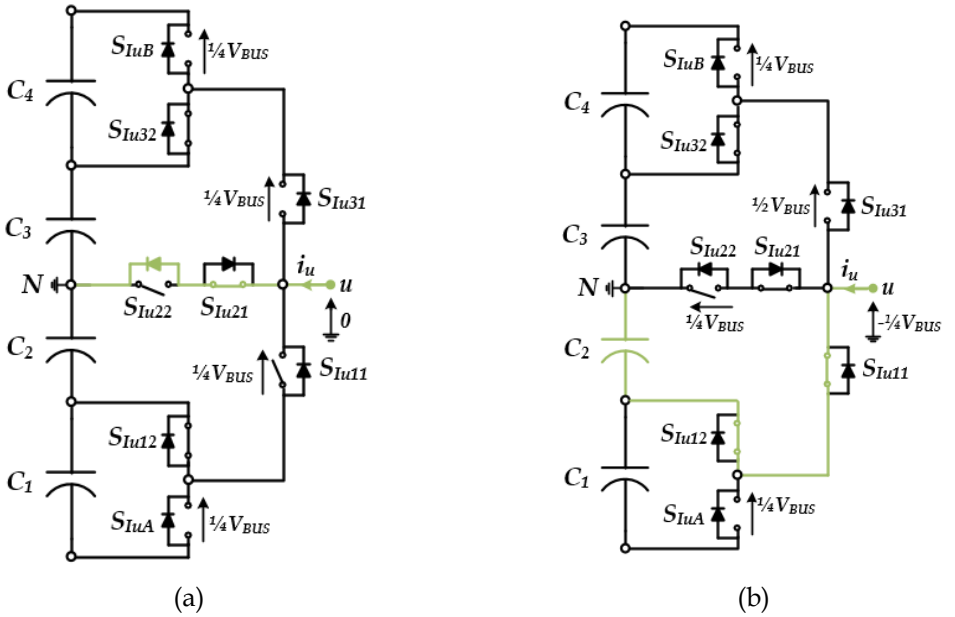
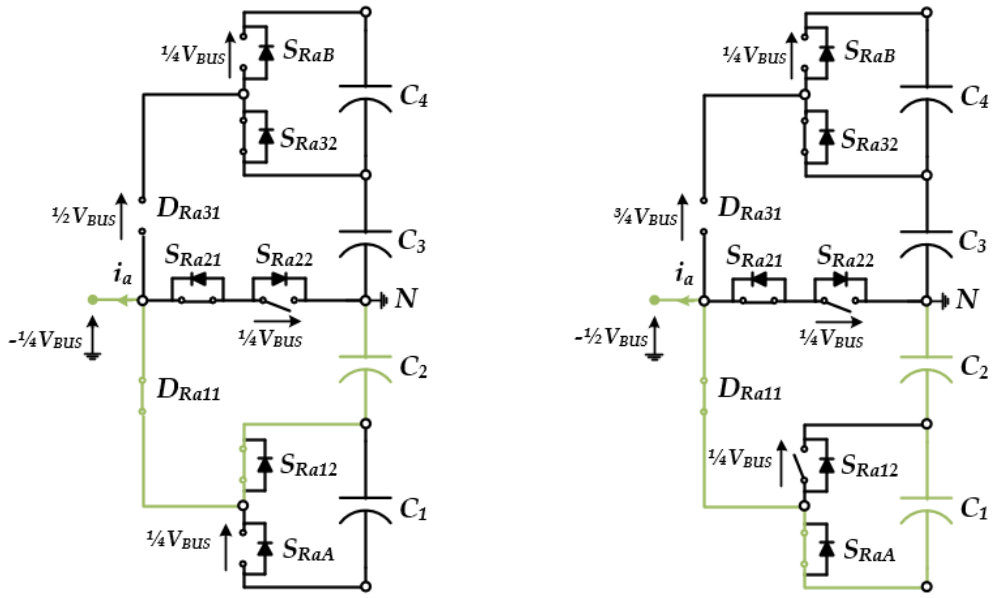
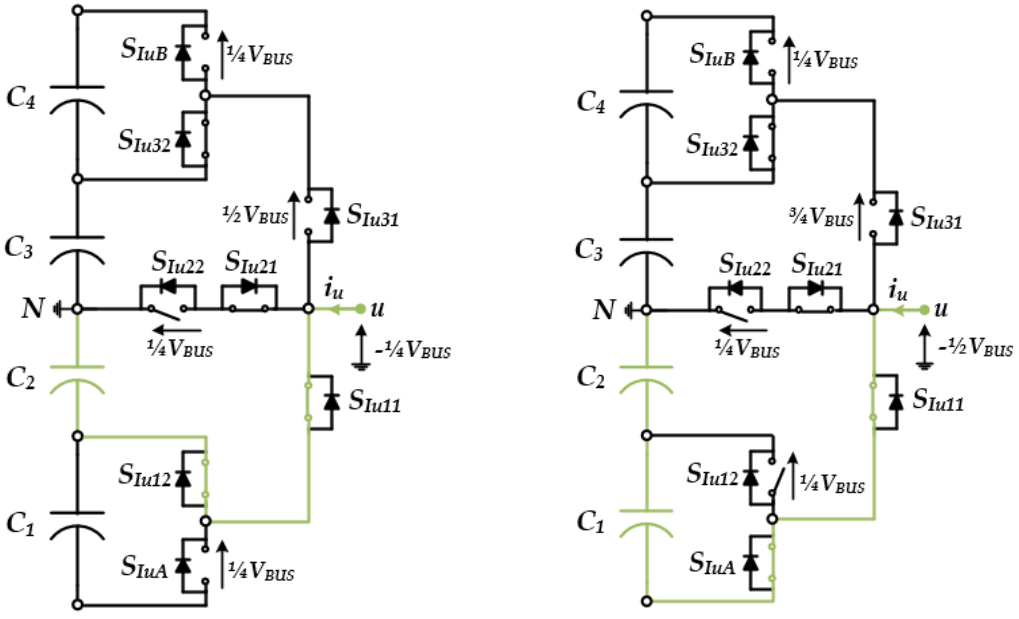


Fig. 103. Current path Inverter: a) $u_{u(sw)}$=0 V, b) $u_{u(sw)}$=-¼V_{BUS} V. Area 2 with negative current, π+φ_{OUT}<ω_{OUT}≤π+α_1 & 2π-α_1<ω_{OUT}≤2π and -0.5≤$m_{Q,I}$(t)<0.



(a) (b)

Fig. 104. Current path Rectifier: a) $u_{a(sw)}$=-¼V_{BUS} V, b) $u_{a(sw)}$=- ½V_{BUS} V. Area 1, $\pi+\alpha_1<\omega_{IN}\leq 2\pi-\alpha_1$, and $-1\leq m_{P,R}(t)<-0.5$.



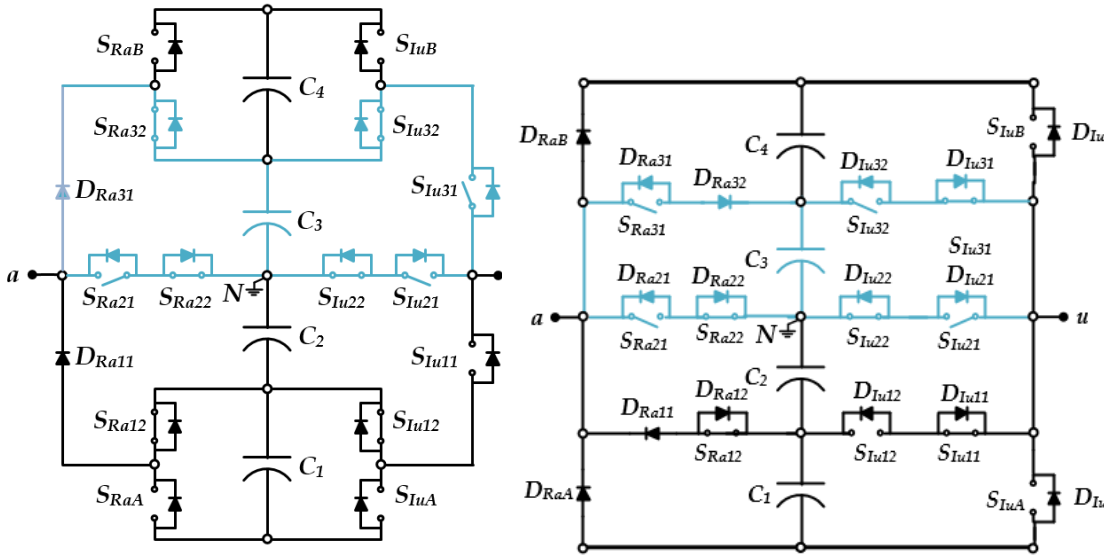
(a) (b)

Fig. 105. Current path Inverter: a) $u_{u(sw)}$=-¼V_{BUS} V, b) $u_{u(sw)}$=- ½V_{BUS} V. Area 1, $\pi+\alpha_1<\omega_{OUT}\leq 2\pi-\alpha_1$ and $-1\leq m_{Q,I}(t)<-0.5$.

6.6 Comparison of the Commutation Loops

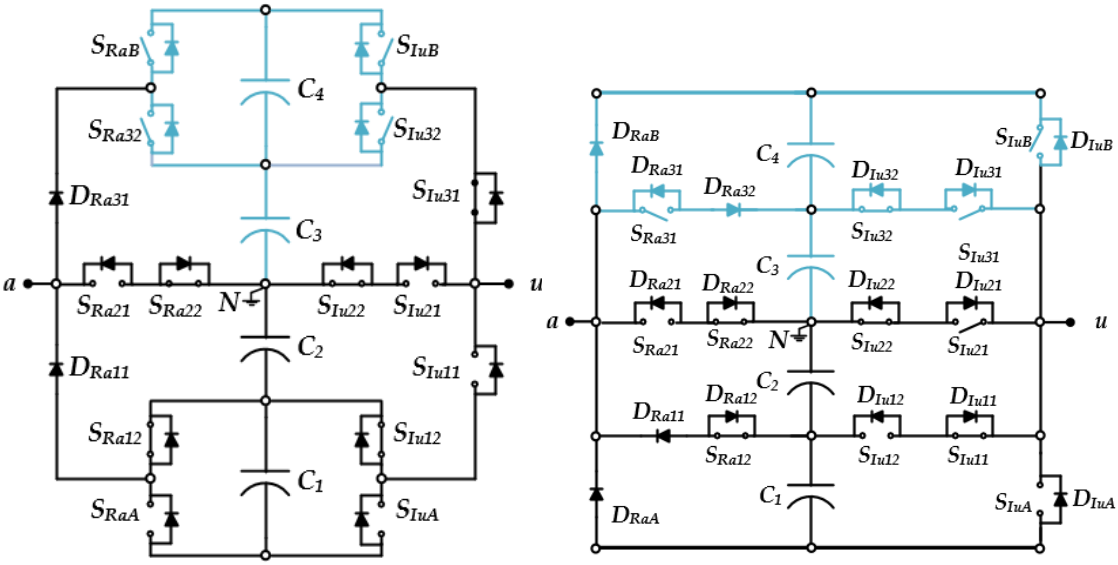
The New 5L BTB E-Type Topology shows benefits in the voltage rating, as well it achieves the commutation loop improvements. When the rectifier and the inverter modulation indexes are $0\leq m_{P,R}(t)\leq 0.5$, $0\leq m_{Q,I}(t)\leq 0.5$, $-0.5\leq m_{P,R}(t)<0$ and -

$0.5 \leq m_{Q,I}(t) < 0$, the commutation loop of the "New" 5L BTB E-Type Converter and the "Old" 5L BTB E-Type Converter are the same, as it can be seen from Fig. 106.



(a) (b)

Fig. 106. Commutation loop with $0 \leq m_{P,R}(t) \leq 0.5$ and $0 \leq m_{Q,I}(t) \leq 0.5$: a) New 5L BTB E-Type BTB Converter, b) Old 5L BTB E-Type BTB Converter.



(a) (b)

Fig. 107. Commutation loop with $0.5 < m_{P,R}(t) \leq 1$ and $0.5 < m_{Q,I}(t) \leq 1$: a) New single-phase 5L BTB E-Type BTB Converter, b) Old single-phase 5L BTB E-Type BTB Converter.

Fig. 107 shows the "New" 5L BTB E-Type Converter and the "Old" 5L BTB E-Type Converter when their modulation indexes are included between $0.5 < m_{P,R}(t) \leq 1$ and $0.5 < m_{Q,I}(t) \leq 1$ and $-1 \leq m_{P,R}(t) < -0.5$ and $-1 \leq m_{Q,I}(t) < -0.5$. It can be noticed that the commutation loop of the "New" 5L BTB E-Type Converter

involves two power devices in the rectifier side (S_{RaB}, S_{Ra32}) and two power devices in the inverter side (S_{IuB}, S_{Iu32}). On the contrary, the commutation loop of the "Old" 5L BTB E-Type Converter includes three power devices in the rectifier side (D_{RaB}, S_{Ra31}, D_{Ra32}) and three power devices in the inverter side (S_{IuB}, S_{Iu31}, S_{Iu32}). Thus, the "New" 5L BTB E-Type BTB Converter show a better commutation loop compared with the "Old" 5L BTB E-Type BTB Converter. Additionally, as explained in the previous section, some devices of the "New" topology present the better voltage rating compared to the "Old" topology. The "New" topology power devices located in the outer-leg S_{RaA}, S_{Ra12}, S_{RaB}, S_{Ra32}, and S_{IuA}, S_{Iu12}, S_{IuB}, S_{Iu32} have $¼V_{BUS}$ voltage ratings. On the other hand, the voltage rating of the "Old" topology power semiconductors located in the top-middle leg S_{Ra31}, S_{Iu31} and D_{Ra32}, S_{Iu32} are $¼V_{BUS}$ and $¾V_{BUS}$, respectively. The "Old" topology device located in the outer-leg S_{IuB} has V_{BUS} voltage rating. Given the symmetry of the 5L BTB E-Type Topology respect to the middle-leg, we can assert the same at bottom-side of the circuit. According to this analysis, the commutation inductance L_{ξ} of the "New" 5L BTB E-Type Converter is reduced.

6.7 Device Current Stress

In this section, the analytical approach is presented to calculate the average (AVG) and the RMS current flowing through the power semiconductors in the N5L E-Type BTB Converter. For the sake of simplicity, only the phase "*a*" of the N5L E-Type Rectifier and the phase "*u*" of the N5L E-Type Inverter have been considered. Let us assume the input and output current as in (77) and (78).

$$i_a(\mathrm{t}) = \sqrt{2} I_{IN} \sin\left(\omega_{IN} t - \rho \frac{2}{3} \pi \right) \tag{77}$$

$$i_u(\mathrm{t}) = \sqrt{2} I_{OUT} \sin\left(\omega_{OUT} t - \rho \frac{2}{3} \pi - \varphi_{OUT} \right) \tag{78}$$

The current flow through the switches has an pulsive waveform as depicted in Fig. 108. The AVG and RMS current over one fundamental period can be found

by equations (79) and (80), where T_{sw} is the switching period and $T_0=nT_{sw}$ is the fundamental period.

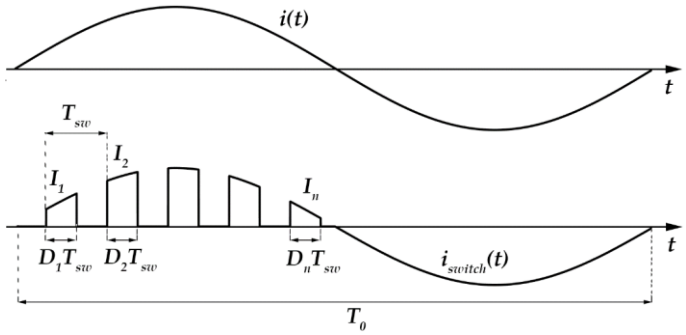


Fig. 108. Switching waveform through devices during one period T_0.

$$I_{RMS}=\sqrt{\frac{1}{T_0}\left(I_1^2D_1T_{sw}+I_2^2D_2T_{sw}+...+I_n^2D_nT_{sw}\right)}=\sqrt{\frac{I_1^2D_1+I_2^2D_2+...+I_n^2D_n}{n}} \tag{79}$$

$$I_{AVG}=\frac{1}{T_0}\left(I_1D_1T_{sw}+I_2D_2T_{sw}+...+I_nD_nT_{sw}\right)=\frac{I_1D_1+I_2D_2+...I_nD_n}{n} \tag{80}$$

The equations (79) and (80) can be written as follows in (81) and (82).

$$I_{RMS}=\sqrt{\frac{1}{n}\sum_{k=1}^{n}I_k^2(n)d_k(n)} \tag{81}$$

$$I_{AVG}=\frac{1}{n}\sum_{k=1}^{n}I_k(n)d_k(n) \tag{82}$$

The corresponding equations in time domain defined are defined in (83) and (84) with reference to the fundamental period, where d_d is the duty cycle of the power device.

$$I_{RMS}=\sqrt{\frac{1}{T_0}\int_0^{T_0}\left[i^2(t)\cdot d_d(t)\right]dt}=\sqrt{\frac{1}{2\pi}\int_0^{\pi}\left[i^2(t)\cdot d_d(t)\right]d(\omega t)} \tag{83}$$

$$I_{AVG}=\frac{1}{T_0}\int_0^{T_0}\left[i(t)\cdot d_d(t)\right]dt=\frac{1}{2\pi}\int_0^{\pi}\left[i(t)\cdot d_d(t)\right]d(\omega t) \tag{84}$$

When the switching frequency is high, the current shape in one switching interval is almost constant, and the error will be small [156]. Substituting the equations (77) and the rectifier duty cycles equation (61)-(66) into (83) and (84), the RMS and AVG current through the power devices of the 5L E-Type Rectifier can be obtained in (85)-(88), where $\theta_R=\omega_{IN}t$.

$$i_{D_{Ra11,RMS}}(t)=i_{D_{Ra31,RMS}}(t)=\left\{\frac{1}{2\pi}\int_{0}^{\alpha_1}\left[2M_{0,R}\sin(\theta_R)\right]\cdot\left[\sqrt{2}I_{IN}\sin(\theta_R)\right]^2 d\theta_R+\right.$$
$$+\frac{1}{2\pi}\int_{\alpha_1}^{\pi-\alpha_1}\left[\sqrt{2}I_{IN}\sin(\theta_R)\right]^2 d\theta_R+$$
$$\left.+\frac{1}{2\pi}\int_{\pi-\alpha_1}^{\pi}\left[2M_{0,R}\sin(\theta_R)\right]\cdot\left[\sqrt{2}I_{IN}\sin(\theta_R)\right]^2 d\theta_R\right\}^{\frac{1}{2}}$$
$$i_{D_{Ra11,AVG}}(t)=i_{D_{Ra31,AVG}}(t)=\left|\frac{1}{2\pi}\int_{0}^{\alpha_1}\left[2M_{0,R}\sin(\theta_R)\right]\cdot\sqrt{2}I_{IN}\sin(\theta_R)d\theta_R\right|+$$
$$+\left|\frac{1}{2\pi}\int_{\alpha_1}^{\pi-\alpha_1}\sqrt{2}I_{IN}\sin(\theta_R)d\theta_R\right|+$$
$$+\left|\frac{1}{2\pi}\int_{\pi-\alpha_1}^{\pi}\left[2M_{0,R}\sin(\theta_R)\right]\cdot\sqrt{2}I_{IN}\sin(\theta_R)d\theta_R\right| \quad (85)$$

$$i_{S_{RaA,RMS}}(t)=i_{S_{RaB,RMS}}(t)=\sqrt{\frac{1}{2\pi}\int_{\alpha_1}^{\pi-\alpha_1}\left[-1+2M_{0,R}\sin(\theta_R)\right]\cdot\left[\sqrt{2}I_{IN}\sin(\theta_R)\right]^2 d\theta_R}$$
$$i_{S_{RaA,AVG}}(t)=i_{S_{RaB,AVG}}(t)=\left|\frac{1}{2\pi}\int_{\alpha_1}^{\pi-\alpha_1}\left[-1+2M_{0,R}\sin(\theta_R)\right]\cdot\sqrt{2}I_{IN}\sin(\theta_R)d\theta_R\right| \quad (86)$$

$$i_{S_{Ra32,RMS}}(t)=i_{S_{Ra12,RMS}}(t)=\left\{\frac{1}{2\pi}\int_{0}^{\alpha_1}\left[2M_{0,R}\sin(\theta_R)\right]\cdot\left[I_{IN}\sin(\theta_R)\right]^2 d\theta_R+\right.$$
$$+\frac{1}{2\pi}\int_{\alpha_1}^{\pi-\alpha_1}2\left[1-M_{0,R}\sin(\theta_R)\right]\cdot\left[I_{IN}\sin(\theta_R)\right]^2 d\theta_R+$$
$$\left.+\frac{1}{2\pi}\int_{\pi-\alpha_1}^{\pi}\left[2M_{0,R}\sin(\theta_R)\right]\cdot\left[I_{IN}\sin(\theta_R)\right]^2 d\theta_R\right\}^{\frac{1}{2}}$$
$$i_{S_{Ra32,AVG}}(t)=i_{S_{Ra12},AVG}(t)=\left|\frac{1}{2\pi}\int_{0}^{\alpha_1}\left[2M_{0,R}\sin(\theta_R)\right]\cdot I_{IN}\sin(\theta_R)d\theta_R\right|+$$
$$+\left|\frac{1}{2\pi}\int_{\alpha_1}^{\pi-\alpha_1}2\left[1-M_{0,R}\sin(\theta_R)\right]\cdot I_{IN}\sin(\theta_R)d\theta_R\right|+$$
$$+\left|\frac{1}{2\pi}\int_{\pi-\alpha_1}^{\pi}\left[2M_{0,R}\sin(\theta_R)\right]\cdot I_{IN}\sin(\theta_R)d\theta_R\right| \quad (87)$$

$$i_{S_{Ra21,RMS}}(t)=i_{S_{Ra22,RMS}}(t)=\left|\frac{1}{2\pi}\int_{0}^{\alpha_1}\left[1-2M_{0,R}\sin(\theta_R)\right]\cdot\left[\sqrt{2}I_{IN}\sin(\theta_R)\right]^2 d\theta_R\right|+$$
$$+\left|\frac{1}{2\pi}\int_{\pi-\alpha_1}^{\pi}\left[1-2M_{0,R}\sin(\theta_R)\right]\cdot\left[\sqrt{2}I_{IN}\sin(\theta_R)\right]^2 d\theta_R\right| \quad (88)$$

$$i_{S_{Ra21,AVG}}(t)=i_{S_{Ra22,AVG}}(t)=\left|\frac{1}{2\pi}\int_{0}^{\alpha_1}\left[1-2M_{0,R}\sin(\theta_R)\right]\cdot\sqrt{2}I_{IN}\sin(\theta_R)d\theta_R\right|+$$
$$+\left|\frac{1}{2\pi}\int_{\pi-\alpha_1}^{\pi}\left[1-2M_{0,R}\sin(\theta_R)\right]\cdot\sqrt{2}I_{IN}\sin(\theta_R)d\theta_R\right|$$

In the same manner replacing the equations (78) and the inverter duty cycles equations (67)-(74) into (83) and (84), the RMS and AVG current through the power devices of the 5L E-Type Inverter are reported in (89)-(92), where $\theta_I=\omega_{OUT}t$.

$$\begin{aligned}i_{S_{Iu11,RMS}}(t)=i_{S_{Iu31,RMS}}(t)=\Bigg\{&\frac{1}{2\pi}\int_{\varphi}^{\alpha_1}\left[2M_{0,I}\sin(\theta_I)\right]\cdot\left[\sqrt{2}I_{OUT}\sin(\theta_I-\varphi_{OUT})\right]^2d\theta_I+\\&+\frac{1}{2\pi}\int_{\alpha_1}^{\pi-\alpha_1}\left[\sqrt{2}I_{OUT}\sin(\theta_I-\varphi_{OUT})\right]^2d\theta_I+\\&+\frac{1}{2\pi}\int_{\pi-\alpha_1}^{\pi}\left[2M_{0,I}\sin(\theta_I)\right]\cdot\left[\sqrt{2}I_{OUT}\sin(\theta_I-\varphi_{OUT})\right]^2d\theta_I\Bigg\}^{\frac{1}{2}}\end{aligned}$$
$$\begin{aligned}i_{S_{Iu11,AVG}}(t)=i_{S_{Iu31,AVG}}(t)=&\left|\frac{1}{2\pi}\int_{\varphi}^{\alpha_1}\left[2M_{0,I}\sin(\theta_I)\right]\cdot\sqrt{2}I_{OUT}\sin(\theta_I-\varphi_{OUT})d\theta_I\right|+\\&+\left|\frac{1}{2\pi}\int_{\alpha_1}^{\pi-\alpha_1}\sqrt{2}I_{OUT}\sin(\theta_I-\varphi_{OUT})d\theta_I\right|+\\&+\left|\frac{1}{2\pi}\int_{\pi-\alpha_1}^{\pi}\left[2M_{0,I}\sin(\theta_I)\right]\cdot\sqrt{2}I_{OUT}\sin(\theta_I-\varphi_{OUT})d\theta_I\right|\end{aligned}\qquad(89)$$

$$i_{S_{IuA,RMS}}(t)=i_{S_{IuB,RMS}}(t)=\sqrt{\frac{1}{2\pi}\int_{\alpha_1}^{\pi-\alpha_1}\left[-1+2M_{0,I}\sin(\theta_I)\right]\cdot\left[\sqrt{2}I_{OUT}\sin(\theta_I-\varphi_{OUT})\right]^2d\theta_I}$$
$$i_{S_{IuA,AVG}}(t)=i_{S_{IuB,AVG}}(t)=\left|\frac{1}{2\pi}\int_{\alpha_1}^{\pi-\alpha_1}\left[-1+2M_{0,I}\sin(\theta_I)\right]\cdot\sqrt{2}I_{OUT}\sin(\theta_I-\varphi_{OUT})d\theta_I\right|\qquad(90)$$

$$\begin{aligned}i_{S_{Iu12,RMS}}(t)=i_{S_{Iu32,RMS}}(t)=\Bigg\{&\frac{1}{2\pi}\int_{\varphi}^{\alpha_1}\left[2M_{0,I}\sin(\theta_I)\right]\cdot\left[\sqrt{2}I_{OUT}\sin(\theta_I-\varphi_{OUT})\right]^2d\theta_I+\\&+\frac{1}{2\pi}\int_{\alpha_1}^{\pi-\alpha_1}2\left[1-M_{0,I}\sin(\theta_I)\right]\cdot\left[\sqrt{2}I_{OUT}\sin(\theta_I-\varphi_{OUT})\right]^2d\theta_I+\\&+\frac{1}{2\pi}\int_{\pi-\alpha_1}^{\pi}\left[2M_{0,I}\sin(\theta_I)\right]\cdot\left[\sqrt{2}I_{OUT}\sin(\theta_I-\varphi_{OUT})\right]^2d\theta_I\Bigg\}^{\frac{1}{2}}\end{aligned}\qquad(91)$$

$$
\begin{aligned}
i_{S_{lu12,AVG}}(t) = i_{S_{lu32,AVG}}(t) = &\left| \frac{1}{2\pi} \int_{\varphi}^{\alpha_1} \left[2M_{0,I} \sin(\theta_I) \right] \cdot \sqrt{2} I_{OUT} \sin(\theta_I - \varphi_{OUT}) d\theta_I \right| + \\
&+ \left| \frac{1}{2\pi} \int_{\alpha_1}^{\pi-\alpha_1} 2\left[1 - M_{0,I} \sin(\theta_I) \right] \cdot \sqrt{2} I_{OUT} \sin(\theta_I - \varphi_{OUT}) d\theta_I \right| + \\
&+ \left| \frac{1}{2\pi} \int_{\pi-\alpha_1}^{\pi} \left[2M_{0,I} \sin(\theta_I) \right] \cdot \sqrt{2} I_{OUT} \sin(\theta_I - \varphi_{OUT}) d\theta_I \right|
\end{aligned}
$$

$$
\begin{aligned}
i_{S_{la21,RMS}}(t) = i_{S_{la22,RMS}}(t) = &\left\{ \frac{1}{2\pi} \int_{\varphi}^{\alpha_1} \left[1 - 2M_{0,R} \sin(\theta_I) \right] \cdot \left[\sqrt{2} I_{OUT} \sin(\theta_I - \varphi_{OUT}) \right]^2 d\theta_I + \right. \\
&+ \frac{1}{2\pi} \int_{\pi-\alpha_1}^{\pi} \left[1 - 2M_{0,R} \sin(\theta_I) \right] \cdot \left[\sqrt{2} I_{OUT} \sin(\theta_I - \varphi_{OUT}) \right]^2 d\theta_I + \\
&\left. + \frac{1}{2\pi} \int_{\pi}^{\pi+\varphi} \left[1 + 2M_{0,R} \sin(\theta_I) \right] \cdot \left[\sqrt{2} I_{OUT} \sin(\theta_I - \varphi_{OUT}) \right]^2 d\theta_I \right\}^{\frac{1}{2}}
\end{aligned}
\tag{92}
$$

$$
\begin{aligned}
i_{S_{la21,AVG}}(t) = i_{S_{la22,AVG}}(t) = &\left| \frac{1}{2\pi} \int_{\varphi}^{\alpha_1} \left[1 - 2M_{0,R} \sin(\theta_I) \right] \cdot \sqrt{2} I_{OUT} \sin(\theta_I - \varphi_{OUT}) d\theta_I \right| + \\
&+ \left| \frac{1}{2\pi} \int_{\pi-\alpha_1}^{\pi} \left[1 - 2M_{0,R} \sin(\theta_I) \right] \cdot \sqrt{2} I_{OUT} \sin(\theta_I - \varphi_{OUT}) d\theta_I \right| + \\
&+ \left| \frac{1}{2\pi} \int_{\pi}^{\pi+\varphi} \left[1 + 2M_{0,R} \sin(\theta_I) \right] \cdot \sqrt{2} I_{OUT} \sin(\theta_I - \varphi_{OUT}) d\theta_I \right|
\end{aligned}
$$

It can be noticed the current symmetry into power semiconductors compared to the middle leg. Performing some algebraic operations, the AVG and RMS current analytical expression related to the devices of the N5L E-Type BTB Converter can be written as in (93).

$$
\begin{aligned}
i_{RMS,i}(t) &= \sqrt{\frac{\left(\sqrt{2} I_{IN} \right)^2 M_{0,R}}{12\pi} \left(\frac{a_{RMS,i}}{M_{0,R}} + b_{RMS,i} \right)} \\
\left| i_{AVG,i}(t) \right| &= \frac{\sqrt{2} I_{IN} M_{0,R}}{2\pi} \left(\frac{a_{AVG,i}}{M_{0,R}} + b_{AVG,i} \right) \\
i_{RMS,j}(t) &= \sqrt{\frac{\left(\sqrt{2} I_{OUT} \right)^2 M_{0,I}}{12\pi} \left(\frac{a_{RMS,j}}{M_{0,I}} + b_{RMS,j} \right)} \\
\left| i_{RMS,j}(t) \right| &= \frac{\sqrt{2} I_{OUT} M_{0,I}}{2\pi} \left(\frac{a_{RMS,j}}{M_{0,I}} + b_{RMS,j} \right)
\end{aligned}
\tag{93}
$$

In (93) the index "*i*" is related to devices located in the 3ΦN5L E-Type Rectifier

and "*j*" is linked to devices placed in the 3ΦN5L E-Type Inverter. The coefficients of the AVG and RMS current ($a_{RMS,i}$, $b_{RMS,i}$, $a_{AVG,i}$, $b_{AVG,i}$, $a_{RMS,j}$, $b_{RMS,j}$, $a_{AVG,j}$, $b_{AVG,j}$) are reported in Table 15 and Table 16.

Table 15. RMS and AVG Current Coefficients of the 3ΦN5L E-Type Rectifier

i	Devices	Coefficient
1	D_{RP11}, D_{RP31}	$a_{RMS,1} = 3\pi - 6\alpha_1 - 3\sin(2\alpha_1)$ $b_{RMS,1} = 8(\cos(\alpha_1)+2)(\cos(\alpha_1)-1)^2$ $a_{AVG,1} = 2\cos(\alpha_1)$ $b_{AVG,1} = 2\alpha_1 - \sin(2\alpha_1)$
2	S_{RPA}, S_{RPB},	$a_{RMS,2} = 3\pi - 6\alpha_1 + 3\sin(2\alpha_1)$ $b_{RMS,2} = -4\cos(\alpha_1)(\cos^2(\alpha_1)-3)$ $a_{AVG,2} = -2\cos(\alpha_1)$ $b_{AVG,2} = \sin(2\alpha_1) - 2\alpha_1 + \pi$
3	S_{RP12}, S_{RP32}	$a_{RMS,3} = \frac{3}{2}(\pi - 2\alpha_1 + \sin(2\alpha_1))$ $b_{RMS,3} = 2\left[\cos(\alpha_1)(\cos^2(\alpha_1)-3)+(\cos(\alpha_1)+2)(\cos(\alpha_1)-1)^2\right]$ $a_{AVG,3} = 4\cos(\alpha_1)$ $b_{AVG,3} = 4\alpha_1 - 2\sin(2\alpha_1) - \pi$
4	S_{RP21}, S_{RP22}	$a_{RMS,4} = \frac{1}{2}\left[2\alpha_1 - \sin(2\alpha_1)\right]$ $b_{RMS,4} = 2(\cos(\alpha_1)-1)^2(-\cos(\alpha_1)-2)$ $a_{AVG,4} = 2(1-\cos(\alpha_1))$ $b_{AVG,4} = \sin(2\alpha_1) - 2\alpha_1$

Table 16. RMS and AVG Current Coefficients of the 3ΦN5L E-Type Inverter

j	Devices	Coefficient
1	S_{IQ31}, S_{IQ11}	$a_{RMS,1} = 3\pi - 6\alpha_1 - 3\sin(2\alpha_1) + 6\sin(2\alpha_1)\cos^2(\varphi_{OUT})$ $b_{RMS,1} = -4\sin(\varphi_{OUT})^2 + 6\sin\left(\frac{\alpha_1}{2} + \varphi_{OUT}\right)^2 - 2\sin\left(\frac{3\alpha_1}{2} + \varphi_{OUT}\right)^2 +$ $+ \sin(3\alpha_1 - \varphi_{OUT}) - 6\cos(\alpha_1) + 8\cos(\varphi_{OUT}) - 3\cos(\alpha_1 - 2\varphi_{OUT})$ $a_{AVG,1} = 4\cos(\alpha_1)\cos(\varphi_{OUT})$ $b_{AVG,1} = 2\sin(\alpha_1) + \cos(\varphi_{OUT})[4\alpha_1 - 2\sin(2\alpha_1) - 2\varphi_{OUT}]$
2	S_{IQA}, S_{IQB}	$a_{RMS,2} = 6\alpha_1 - 3\pi + 3\sin(2\alpha_1) - 3(1 + \cos(2\varphi_{OUT}))\sin(2\alpha_1)$ $b_{RMS,2} = 8\cos^3(\alpha_1) + 24\cos^2(\varphi_{OUT})\cos(\alpha_1) - 12\cos^3(\alpha_1)\cos(\varphi_{OUT})$ $a_{AVG,2} = -2\cos(\varphi_{OUT})\cos(\alpha_1)$ $b_{AVG,2} = \cos(\varphi_{OUT})[\sin(2\alpha_1) - 2\alpha_1 + \pi]$
3	S_{IQ12}, S_{IQ32}	$a_{RMS,3} = \frac{3}{2}[\pi - 2\alpha_1 + \sin(2\alpha_1)\cos(2\varphi_{OUT})]$ $b_{RMS,3} = \frac{1}{2}[3 - 12\cos(\alpha_1) + 4\cos(\varphi_{OUT}) + \cos(2\varphi_{OUT}) +$ $-6\cos(2\varphi_{OUT})\cos(\alpha_1) + 2\cos(3\alpha_1)\cos(2\varphi_{OUT})]$ $a_{AVG,3} = 8\cos(\alpha_1)\cos(\varphi_{OUT})$ $b_{AVG,3} = 2\sin(\varphi_{OUT}) + 2\alpha_1\cos(\varphi_{OUT}) - 2\varphi_{OUT}\cos(\varphi_{OUT}) +$ $-3\sin(2\alpha_1)\cos(\varphi_{OUT}) - \pi\cos(\varphi_{OUT})$
4	S_{IQ21}, S_{IQ22}	$a_{RMS,4} = 3\alpha_1 - 3\cos(2\varphi_{OUT})\cos(\alpha_1)\sin(\alpha_1)$ $b_{RMS,4} = -6 + 6\cos(\alpha_1) - 2\cos(2\varphi_{OUT}) + 6\cos(2\varphi_{OUT})\cos(\alpha_1) +$ $-4\cos(2\varphi_{OUT})\cos^3(\alpha_1)$ $a_{AVG,4} = 2 - 2\cos(\varphi_{OUT})\cos(\alpha_1)$ $b_{AVG,4} = -2\cos(\varphi_{OUT}) + \sin(2\alpha_1)\cos(\varphi_{OUT}) - 2\alpha_1\cos(\varphi_{OUT}) +$ $+2\varphi_{OUT}\cos(\varphi_{OUT})$

Finally, we can estimate the current stress for each device of the N5L E-Type BTB Converter from the numerical point of view. Considering $V_{IN)}$=V_{OUT}=*230* V,

V_{BUS}=700 V, $M_{0,R}$=$M_{0,I}$=0.93, $cos\varphi_{OUT}$=1, Table 17 shows the AVG and RMS current value for each power semiconductor as a function of the output power. It can be noticed as the most stressed devices are D_{RP11}, D_{RP31} and S_{IQ11}, S_{IQ31}. Having defined the voltage rating and the current stress for each device, it is possible to choose the potential discrete components of the N5L E-Type BTB Converter. After that, AVG and RMS equations will be used to evaluate both the conduction and the switching loss in the N5L E-Type BTB Converter.

Table 17. RMS and Average current for the N5L E-Type BTB Converter.

Operating Parameters: $V_{IN(rms)}$= $V_{OUT(rms)}$=230 V, V_{BUS}=700 V, $M_{0,R}$=$M_{0,I}$=0.93, cosφ_{OUT}=1.										
	P_{out}=3kW		P_{out}=5kW		P_{out}=10kW		P_{out}=15kW		P_{out}=20kW	
	$I_{OUT(rms)}$=4.35 A		$I_{OUT(rms)}$=7.25 A		$I_{OUT(rms)}$=14.49 A		$I_{OUT(rms)}$=21.74 A		$I_{OUT(rms)}$=28.99A	
	AVG [A]	RMS [A]	AVG [A]	RMS [A]	AVG [A]	RMS [A]	AVG [A]	RMS [A]	AVG [A]	RMS [A]
5L E-Type Rectifier										
D_{RP11}, D_{RP31}	1.85	3.04	3.08	5.07	6.15	10.14	9.23	15.21	12.31	20.28
$S_{RPA,}$ S_{RPB}	0.84	2.20	1.43	3.67	2.86	7.34	4.28	11.01	5.71	14.69
S_{RP12}, S_{RP32}	0.99	2.10	1.65	3.50	3.30	6.99	4.95	10.49	6.59	13.99
S_{RP21}, S_{RP22}	0.11	0.45	0.19	0.74	0.37	1.48	0.56	2.23	0.74	2.97
5L E-Type Inverter										
S_{IQ11}, S_{IQ31}	1.85	3.04	3.08	5.07	6.15	10.14	9.23	15.21	12.31	20.28
S_{IQA}, S_{IQB}	0.86	2.20	1.43	3.67	2.86	7.34	4.28	11.01	5.71	14.69
S_{IQ12}, S_{IQ32}	0.99	2.10	1.65	3.50	3.30	6.99	4.95	10.49	6.59	13.99
S_{IQ21}, S_{IQ22}	0.11	0.45	0.19	0.74	0.37	1.48	0.56	2.23	0.74	2.97

7 LOSSES ANALYSIS

7.1 Loss Mechanism: General Case

In this section, the losses mechanism for the power semiconductor devices will be explained. The criteria that seriously affect the power semiconductor selection and the reasonable design of the power electronic converter are the conduction and switching losses calculation and the heat transfer issues for the power devices. An ideal switch is a two-terminal device in which the input is the control terminal and the output is the power terminal, Fig. 109a. The voltage v_{sw} and current i_{sw} across the switch can be both positive and negative; thus, the switch can work in one of four quadrants, Fig. 109b. When the control signal is 0 the switch is open (OFF-state); the switch voltage is unlimited and the switch leakage current is zero. On the contrary when the control signal is 1 the switch is close (ON-state); the switch current is unlimited and the switch-on-state voltage is zero.

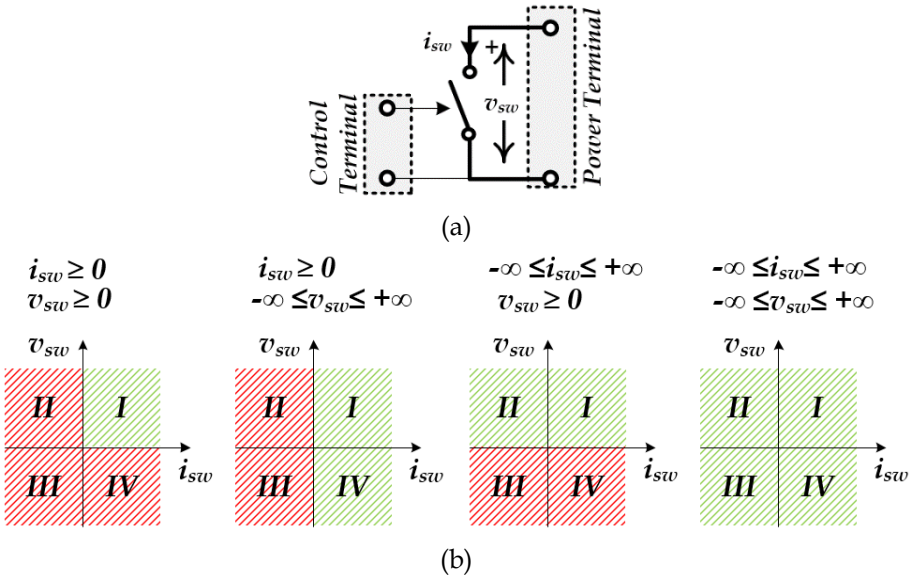


Fig. 109. a) Ideal switch, b) polarity of the voltage and current.

Additionally, the transition from to ON-state to OFF-state and OFF-state to ON-state is instantaneous, which means that the slope di_{sw}/dt and slope dv_{sw}/dt are unlimited. Consequently, there are no conduction and switching losses in the ideal switch. As mentioned in the previous chapter, an ideal switch does not

exist. Due to non-ideal switches, the power semiconductor devices suffer from conduction and switching losses.

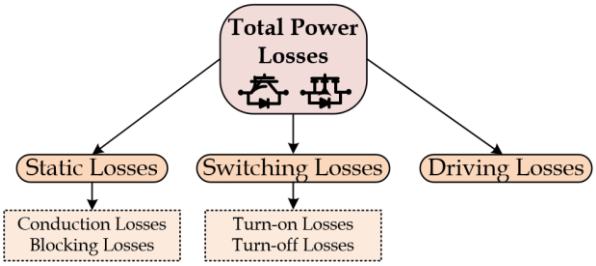


Fig. 110. Total losses in a switching device.

For the sake of clarity, the total losses in a switching device can be divided in three main categories and then in some other sub-categories, Fig. 110.

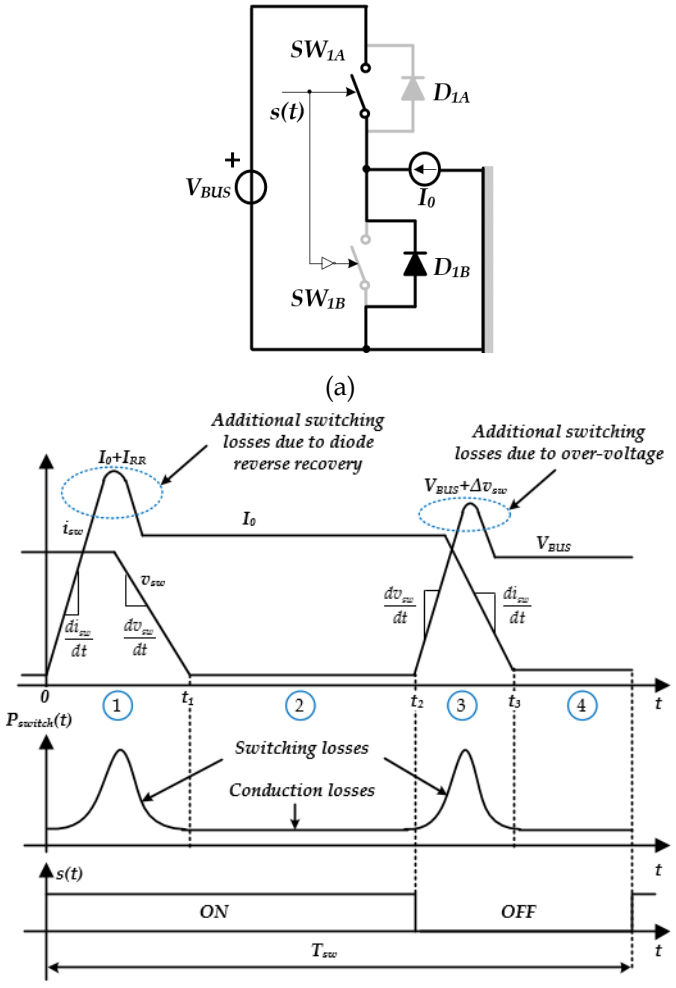


Fig. 111. a) Basic switching cell of power electronics, b) Voltage, current and losses of the power semiconductor over one switching period.

Driving losses is a minimal part of the total power losses and their contribution

will be evaluated in the next step. Let us consider the basic switching cell of a power converter composed of two switches and two freewheeling diodes, Fig. 111a. The switching cell load current is I_0. We can recognize two different commutation scenarios; in the first one, the load current commutes from the D_{1B} to the opposite switch SW_{1A}, in the second one the load current commutes from the switch SW_{1B} to the opposite diode D_{1A}. In the first commutation scenario, when the control signal of SW_{1a} is ON (s(t)=ON), the switching current flow in SW_{1a} rises with slope di_{sw}/dt and the diode reverse voltage elevates with a rate that strongly depends on the performance of the diode and the opposite switch gate driver, Fig. 111b. The diode returns current flows as additional current in the switch (but not within the load) which increases the turn-on losses in the switch. During the turn-off of SW_{1a}, when the control signal is OFF (s(t)=OFF), the switching voltage v_{sw} rises with slope dv_{sw}/dt that is determined by the gate driver [166]. Fig. 111b shows the voltage $v_{sw}(t)$, current $i_{sw}(t)$ and power loss $p_{switch}(t)$ across the power semiconductor SW_{1A} over one switching period T_{sw}. It can be seen that the power loss is composed by four areas along to one switching period T_{sw}: 1) $0 \le t < t_1$, turn-on, 2) $t_1 \le t < t_2$, conduction state, 3) $t_2 \le t < t_3$, turn-off and 4) $t \ge t_3$, blocking state. The total power dissipated through one device along the switching period can be obtained as in the equation (94).

$$P_{switch}(t) = \frac{1}{T_{sw}} \left(\overbrace{\int_0^{t_1} (v_{sw} \cdot i_{sw}) dt}^{1)Turn-on} + \overbrace{\int_{t_1}^{t_2} (v_{sw} \cdot i_{sw}) dt}^{2)conduction\ state} + \overbrace{\int_{t_2}^{t_3} (v_{sw} \cdot i_{sw}) dt}^{3)Turn-off} + \overbrace{\int_{t_3}^{T_0} (v_{sw} \cdot i_{sw}) dt}^{4)Blocking\ state} \right) \quad (94)$$

7.2 Conduction Losses

Conduction losses occur while the power device is in the on-state and is conducting the current. Therefore, the power loss during conduction is computed by multiplying the device voltage drop with the flowing current in the on-state.

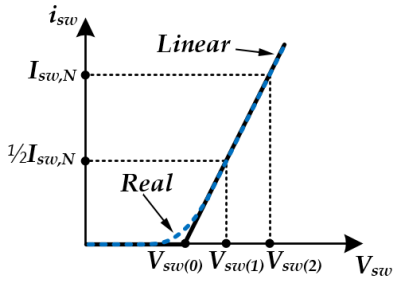


Fig. 112. Power semiconductor output characteristic: real curve (blue line) and linear curve (black line).

Since the first-order approximation of the real curve data (I_C-V_{CE}, I_F-V_F and I_D-V_{DS}) from the device datasheet in some cases [156] has almost the same accuracy of the second or third approximation, the conduction power losses can be reasonably obtained from the first-order approximation. Fig. 112 shows a linear approximation of the power semiconductor output characteristic. $V_{sw(1)}$ and $V_{sw(2)}$ are the voltage across the devices at rated $I_{sw,N}$ and half rated ½$I_{sw,N}$ current, respectively. Thus, the forward on-state properties in semiconductors can be approximated by the series of the forward voltage drop $V_{sw(0)}$ ($V_{CE(0)}$ and $V_{D(0)}$ for respectively IGBTs and diodes, obviously $V_{DC(0)}$ is zero) and the ohmic resistance r_{sw} (r_{CE}, r_D and r_{DS} for respectively IGBTs, diodes and MOSFETs), according to the expression (95), where the forward voltage drop $V_{sw(0)}$ and the ohmic resistance r_{sw} can be expressed as in (96).

$$v_{sw}(t) = V_{sw(0)} + r_{sw} i_{sw}(t) \tag{95}$$

$$V_{sw(0)} = 2V_{sw(1)} - V_{sw(2)}, \quad r_{sw} = 2\frac{V_{sw(2)} - V_{\mathrm{sw}(1)}}{I_{sw,N}} \tag{96}$$

Both value $V_{sw(0)}$ and r_{sw} have been obtained directly from the IGBTs, MOSFETs and diodes datasheet. The achieved parameters consider the effects of the temperature on the power semiconductors. Since the switching period is much smaller than the period of the fundamental component, the conduction losses of the power devices can be calculated as in (97), where I_{AVG} and I_{RMS} are the average and RMS current flowing through the power semiconductors over one fundamental period T_0, respectively (see equation (83) and (84)).

$$P_c = \frac{1}{T_{sw}}\int_{t_1}^{t_2}\left[v_{sw}(t)\cdot i_{sw}(t)\right]dt = \frac{1}{T_{sw}}\int_{t_1}^{t_2}\left\{\left[V_{sw0}+r_{sw}i_{sw}(t)\right]\cdot i_{sw}(t)\right\}dt =$$
$$= V_{sw0}\underbrace{\frac{1}{T_{sw}}\int_{t_1}^{t_2} i_{sw}(t)dt}_{I_{AVG}} + r_{sw}\underbrace{\frac{1}{T_{sw}}\int_{t_1}^{t_2} i_{sw}^2(t)dt}_{I_{RMS}^2} \cong V_{sw0}I_{AVG} + r_{sw}I_{RMS}^2 \quad (97)$$

7.3 Switching Losses

In order to calculate the switching losses, it is essential to estimate the turn-on and turn-off energy losses at the operating point for each device, as IGBT, MOSFET and diode. To this purpose, we can use the turn-on and turn-off energy loss data corresponding to the phase voltage and current waveforms test points provided in the device datasheet. Investigation of analytical expressions for both switching and conduction losses have been developed in [64], [156]. Turn-on and turn-off losses have been computed using equations (98) and (99) respectively.

$$P_{on} = \frac{1}{T_{sw}}\cdot\int_0^{t_1} v_{sw}(t)\cdot i_{sw}(t)dt \quad (98)$$

$$P_{off} = \frac{1}{T_{sw}}\cdot\int_{t_2}^{t_3} v_{sw}(t)\cdot i_{sw}(t)dt \quad (99)$$

At the rated conditions, the expression for the average switching losses in the device can be written as in (100), where E_{AVG} is the average switching energy over fundamental period T_0. The average switching energy E_{AVG} is defined as in (101), where $i_0(t)$ is the switch commutation current, $V_{BUS}(t)$ is the voltage across the switch (V_{BUS} or a fraction of V_{BUS}), $E_{on}(T_j, V_{CE}, I_C)$, $E_{off}(T_j, V_{CE}, I_C)$, are the turn-on and turn-off energy at the rated condition and I_N and V_N are the current and voltage at the rated condition, respectively.

$$P_{sw} = f_{sw}\cdot E_{AVG} \quad (100)$$

$$E_{AVG} = \left[E_{on}\left(T_j, V_{CE}, I_C\right) + E_{off}\left(T_j, V_{CE}, I_C\right)\right]\frac{1}{V_N I_N}\frac{1}{T_0}\int_0^{T_0} V_{BUS}(t)i_0(t)dt \quad (101)$$

Using data-sheet of switching energy supplied by the manufacturers, the turn-on $E_{on}(T_j, V_{CE}, I_C)$ and turn-off energy $E_{off}(T_j, V_{CE}, I_C)$ of IGBTs can be obtained (see APPENDIX). Differently, the turn-on energy and turn-off energy of

MOSFETs are not reported on data-sheet. To this purpose, the turn-on and the turn-off switching time have been estimated according to application note [170]. Thus, the average switching energy E_{AVG} for MOSFETs can be written as in (102), where ton and toff are the turn-on and the turn-off switching time (see APPENDIX).

$$E_T = E_{on}\left(T_j, V_{DS}, I_D\right) + E_{off}\left(T_j, V_{DS}, I_D\right) \cong \frac{\left(t_{on} + t_{off}\right)}{2} V_{DS} I_D$$

7.4 Diode reverse recovery

The recovery losses in the freewheeling diodes have been approximated through the first order equation (103), where $E_{rr,AVG}$ is the average switching energy over fundamental period T_0. The average switching energy $E_{rr,AVG}$ is defined as in (104), where $E_{rr}(T_j, V_{CE})$ is the reverse recovery energy.

$$P_{sw} = f_{sw} \cdot E_{rr,AVG} \tag{103}$$

$$E_{rr,AVG} = \frac{E_{rr}\left(T_j, V_{sw}\right)}{I_N} \int_0^{T_0} V_{BUS}(t) i_0(t) dt \tag{104}$$

7.5 Blocking losses

The blocking losses can be computed from equation (105), where d_{sw} is the duty cycle of the switches and $I_{sw(\zeta)}$ is the switch leakage current. The blocking losses are significantly lower than the conduction and switching losses. As a result, the blocking losses are usually neglected.

$$P_{off} = \frac{1}{T_{sw}} \cdot \int_{t_3}^{T_{sw}} v_{sw}(t) \cdot i_{sw}(t) dt \cong \left(1 - d_{sw}\right) \frac{V_{BUS}}{4} I_{sw(\zeta)} \tag{105}$$

However, in some cases, such as in high voltage and high temperature applications, the blocking losses may become significant. In this case, if the switch cooling system is not properly designed taking into account also the blocking losses, the device may fail due to the thermal run-away phenomena.

8 INPUT-OUTPUT FILTER CONFIGURATION

8.1.1 Filters Design Objective

The input and output filters requirements are the input current THD_i less than 3% and output voltage THD_v less than 1%, respectively. The THD_i and THD_v limit must not be exceeded in the worst case of minimum filter capacitance and maximum input voltage. The input and output filters design objectives are:

- Minimized cost, size and losses of the filters passive components (capacitors and magnetics).
- Minimized current stress of the filter capacitors under condition of maximum input and output voltages.

8.1.2 Concept of Interleaving

The interleaving is a form of paralleling technique where a single converter is replaced by N_C converters connected in parallel, with their switching instants to be phase shifted equally or interleaved over a switching period. The interleaved topology has been recently gaining popularity [157] for different power applications such as electric and hybrid electric vehicles [158], communication power supplies, power factor correction for small handheld tools [159], and power boost circuit for photovoltaic systems [160]. Why do we need interleaved topology in power conversion? Most of the double conversion systems AC-DC/DC-AC employ LC filters or LCL filters [161], [162]. As the converter power level increases the switching frequency tends to decrease in order to limit the switching losses. Consequently, high-power electronic converters present large filter components. The main drawbacks of having large filter components are the slow-down of the system's dynamic response, resulting from the use of large inductors as well the system's output power factor reduction [163]. Additionally, large capacitors provide both high currents that

reduce the system's output power factor and produce an easy path for harmonic currents caused by grid voltage harmonics, which increases the output current total harmonic distortion [164].

As mentioned in the part one of this dissertation, the need to improve the efficiency, power density and reduce cost of both the AC-DC/DC-AC systems and input/output filter more and more multi-level topologies have been proposed in literature. In order to further improve the efficiency and to reduce the size and cost of the input/output filters, interleaving topology has been introduced. Using interleaving topology each parallel converter is modulated with $2\pi/N_C$ shifted signal, where N_C is the number of the interleaved cells. By introducing a phase shift between the switching instants of the parallel converters of each phase, the amplitude of the total ripple current is reduced, as shown in Fig. 113.

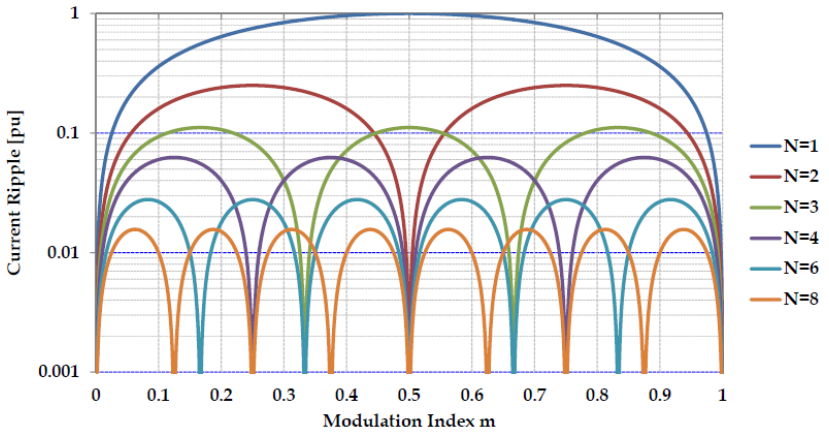


Fig. 113. Current ripple versus modulation index m.

Additionally, the harmonics content of the voltage improves due to the elimination of harmonics below $f_{sw}N_C$. If the current ripple is reduced and the voltage harmonics content improves, the interleaved topology allows to reduce considerably the size of the required filter capacitance. Besides, sharing the current among a number of channels enables the use of smaller lower current power devices than those used in a conventional converter; the smaller devices can switch at a significantly higher frequency than the larger ones, thus allowing a reduction in inductor size.

The DC-bus capacitors are not an ideal loss-free device. The losses are a function of the Equivalent Series Resistance, ESR. We know that ESR decreases inversely with frequency. In general, using the interleaved topology, the frequency is N_C times greater than that of a single converter; thus, the ESR in the DC-bus capacitors of the interleaved converter should be less than the single converter. Consequently, the losses in the DC-bus capacitors of the interleaved converter are reduced. As just mentioned is not true. In this case, DC-bus capacitors losses mainly depend on the fundamental frequency current. The interleaved topology has effect only on high frequency current not on fundamental frequency current.

8.2 N5L E-Type BTB Interleaved with Inter-Cell Transformer

The interleaved topology can be realized with the Inter-Cell Transformer (ICT), which is a magnetic coupling device ideally able to equally distribute the phase current in paralleled legs. The ICT is nothing else than a transformer without leakage inductance. The main advantage of using interleaving topology with ICT is the elimination of the harmonics up to $f_{sw}N_C$, where N_C is the number of the interleaved cells, from the input and/or output voltage. In this case, we have two-cell structure in interleaving. Fig. 114 shows the simplified single-phase circuit diagram of the input and output filters using two-cell structure in interleaving coupling through an ICT device. Accordingly, if the switching frequency of converter is 24 kHz, the voltage harmonics are eliminated up to 48 kHz. Which means that the ICT offers the advantage of reduction of size and cost of the input and output filters.

The input filter is composed by the input filter inductance $L_{IN(P)}$, the input filter capacitance $C_{IN(P)}$ and the Inter-Cell Transformer $ICT_{IN(P)}$ connected between leg 1 and leg 2 of the single-phase N5L E-Type Rectifier. The output filter consists of the output filter inductance $L_{OUT(Q)}$, the output filter capacitance $C_{OUT(Q)}$, and the Inter-Cell Transformers $ICT_{OUT(Q)}$ connected between leg 1 and leg 2 of the single-phase N5L E-Type Inverter. Fig. 115 shows the complete circuit diagram of the

New 5L E-Type BTB Converter including the input/output filters.

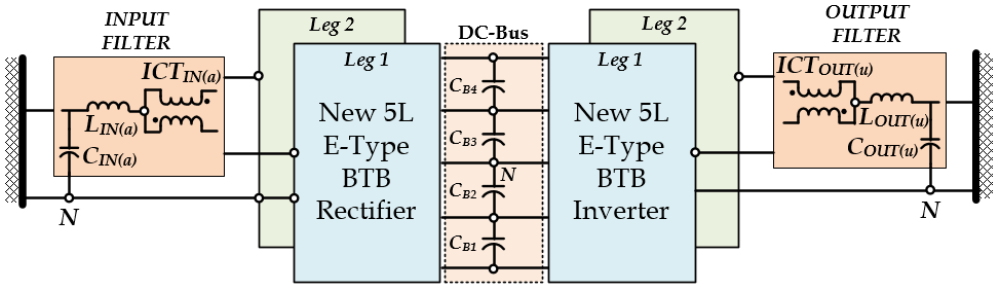


Fig. 114. Simplified single-phase circuit diagram of the input and output filters with two-cell interleaved with ICT.

The first advantage of using the ICT is that the phase current is equally distributed in each leg. Sharing the current among a number of channels enables the use of smaller lower current power devices than those used in a conventional converter. Table 18 illustrates the AVG and RMS current linked to the power semiconductors of one leg N5L E-Type BTB Converter with a number of interlaced cells N_C equal to 2. As it can be seen, the AVG and RMS current values are half of the current value shown in Table 17. The power devices with a reduced current rating can be chosen, and smaller devices can switch at a significantly higher frequency than the larger ones.

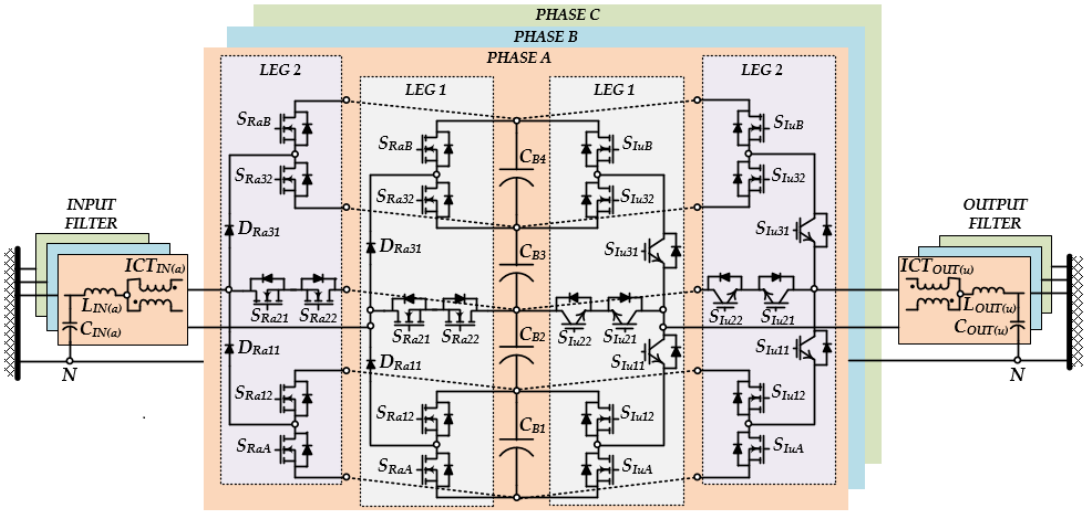


Fig. 115. Complete circuit diagram of the New 5L E-Type BTB Converter.

Table 18. RMS and Average current for the N5L E-Type BTB Converter.

Operating Parameters: $V_{IN(rms)}$= $V_{OUT(rms)}$=230 V, V_{BUS}=700 V, $M_{0,R}$=$M_{0,I}$=0.93, cosφ_{OUT}=1, N_C=2.										
	P_{out}=3kW		P_{out}=5kW		P_{out}=10kW		P_{out}=15kW		P_{out}=20kW	
	$I_{OUT(rms)}$=4.35 A		$I_{OUT(rms)}$=7.25 A		$I_{OUT(rms)}$=14.49 A		$I_{OUT(rms)}$=21.74 A		$I_{OUT(rms)}$=28.99A	
	AVG [A]	RMS [A]	AVG [A]	RMS [A]	AVG [A]	RMS [A]	AVG [A]	RMS [A]	AVG [A]	RMS [A]
5L E-Type Rectifier										
D_{RP11}, D_{RP31}	0.92	1.52	1.54	2.53	3.08	5.07	4.61	7.60	6.15	10.14
S_{RPA}, S_{RPB}	0.43	1.10	0.71	1.84	1.43	3.67	2.14	5.51	2.86	7.34
S_{RP12}, S_{RP32}	0.49	1.05	0.82	1.75	1.65	3.50	2.47	5.24	3.30	6.99
S_{RP21}, S_{RP22}	0.06	0.22	0.09	0.37	0.19	0.74	0.28	1.11	0.37	1.48
5L E-Type Inverter										
S_{IQ11}, S_{IQ31}	0.92	1.52	1.54	2.53	3.08	5.07	4.61	7.60	6.15	10.14
S_{IQA}, S_{IQB}	0.43	1.10	0.71	1.84	1.43	3.67	2.14	5.51	2.86	7.34
S_{IQ12}, S_{IQ32}	0.49	1.05	0.82	1.75	1.65	3.50	2.47	5.24	3.30	6.99
S_{IQ21}, S_{IQ22}	0.06	0.22	0.09	0.37	0.19	0.74	0.28	1.11	0.37	1.48

8.3 Input Rectifier Analysis

Let's consider a single-phase of the N5L E-Type Rectifier and input filter, as depicted in Fig. 116. The switches located in the leg 1, $\mathbf{S_{Ra}} \in \{S_{RaA}, S_{Ra12}, S_{Ra21}, S_{Ra22}, S_{Ra32}, S_{RaB}\}$ are driven by the switching functions $\mathbf{s_{Ra}(t)} \in \{s_{RaA}, s_{Ra12}, s_{Ra21}, s_{Ra22}, s_{Ra32}, s_{RaB}\}$. Using the duty cycles obtained in the section 6.5.1, the switching functions $\mathbf{s_{Ra}(t)}$ are defined over a switching period as in (106), where $T_{sw}=1/f_{sw}$ is the basic switching period. The switches arranged in the leg 2, $\mathbf{S'_{Ra}} \in \{S'_{RaA}, S'_{Ra12}, S'_{Ra21}, S'_{Ra22}, S'_{Ra32}, S'_{RaB}\}$, are driven by the switching function $\mathbf{s'_{Ra}}(t)= \mathbf{s_{Ra}}(t-½T_{SW})$. The switching functions $\mathbf{s_{Ra}(t)}$ and $\mathbf{s'_{Ra}(t)}$ are generated by the pulse width modulators PWM_{R1} and PWM_{R2}, Fig. 116. The modulation scheme of the interleaved N5L E-Type Rectifier is depicted in Fig. 117.

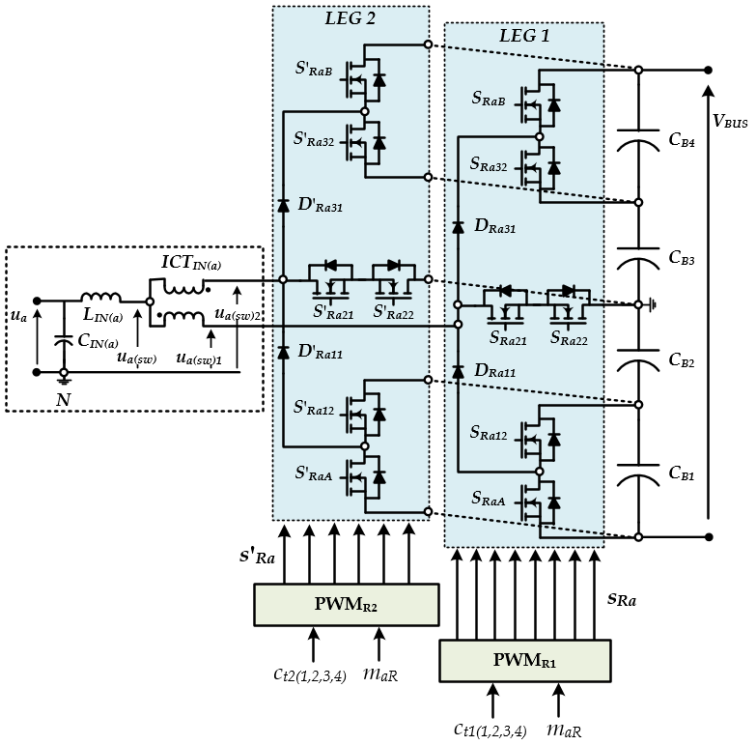


Fig. 116. Single-phase circuit diagram of the N5L E-Type Rectifier and input filter.

The carrier signals, c_{t11}, c_{t12}, c_{t13} and c_{t14} (solid line), are related to the leg 1 and the carrier signals c_{t21}, c_{t22}, c_{t23} and c_{t24} (dashed line), are linked to the leg 2.

$$
\begin{aligned}
s_{RaA}(\mathrm{t}) &= \begin{cases} 1 & 0 \le t \le d_{S_{RaA}}(t)\,\mathrm{T}_{SW} \\ 0 & d_{S_{RaA}}(t)\,\mathrm{T}_{SW} < t \le \mathrm{T}_{SW} \end{cases} \\
s_{Ra12}(\mathrm{t}) &= \begin{cases} 1 & 0 \le t \le d_{S_{Ra12}}(t)\,\mathrm{T}_{SW} \\ 0 & d_{S_{Ra12}}(t)\,\mathrm{T}_{SW} < t \le \mathrm{T}_{SW} \end{cases} \\
s_{Ra21}(\mathrm{t}) &= \begin{cases} 1 & 0 \le t \le d_{S_{Ra21}}(t)\,\mathrm{T}_{SW} \\ 0 & d_{S_{Ra21}}(t)\,\mathrm{T}_{SW} < t \le \mathrm{T}_{SW} \end{cases} \\
s_{Ra22}(\mathrm{t}) &= \begin{cases} 1 & 0 \le t \le d_{S_{Ra22}}(t)\,\mathrm{T}_{SW} \\ 0 & d_{S_{Ra22}}(t)\,\mathrm{T}_{SW} < t \le \mathrm{T}_{SW} \end{cases} \\
s_{Ra32}(\mathrm{t}) &= \begin{cases} 1 & 0 \le t \le d_{S_{Ra32}}(t)\,\mathrm{T}_{SW} \\ 0 & d_{S_{Ra32}}(t)\,\mathrm{T}_{SW} < t \le \mathrm{T}_{SW} \end{cases} \\
s_{RaB}(\mathrm{t}) &= \begin{cases} 1 & 0 \le t \le d_{S_{RaB}}(t)\,\mathrm{T}_{SW} \\ 0 & d_{S_{RaB}}(t)\,\mathrm{T}_{SW} < t \le \mathrm{T}_{SW} \end{cases}
\end{aligned}
\tag{106}
$$

Each carrier controls two different power devices in opposite phase as listed in Table 19. The input-to-neutral switching voltage of the leg 1 and leg 2, $u_{a(sw),1}$ and

$u_{a(sw),2}$, can be written as in (107), where $\theta(i_a)$ is the threshold function defined in (11). The equivalent input voltage $u_{a(sw)}$ is given by equation (108).

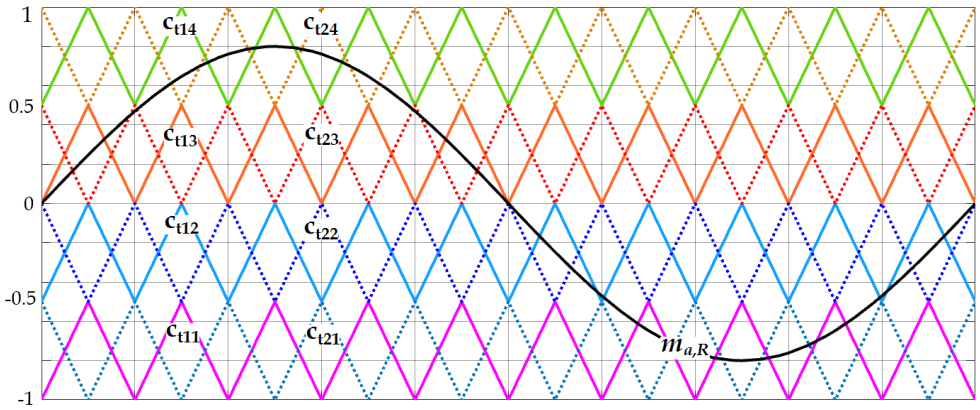


Fig. 117. Modulating scheme of the interleaved N5L E-Type Rectifier.

Table 19. Carriers versus power devices of the N5L E-Type Rectifier.								
Carriers	c_{t11}	c_{t12}	c_{t13}	c_{t14}	c_{t21}	c_{t22}	c_{t23}	c_{t24}
	Leg 1				Leg 2			
	S_{RPA}, S_{RP12}	S_{RP22}	S_{RP21}	S_{RPB}, S_{RP32}	S'_{RPA}, S'_{RP12}	S'_{RP22}	S'_{RP21}	S'_{RPB}, S'_{RP32}

It can be seen that the equivalent input voltage $u_{a(sw)}$ is composed by nine-level voltage.

$$u_{a(sw),1}(t)=\frac{V_{BUS}}{4}\left(1-s_{Ra21}(t)\right)\left(1-s_{Ra22}(t)\right)\left[\theta(i_a)\left(2s_{RaB}(t)+s_{Ra32}(t)-3s_{RaB}(t)s_{Ra32}(t)\right)+\right.$$
$$\left.-\bar{\theta}(i_a)\left(2s_{RaA}(t)+s_{Ra12}(t)-3s_{RaA}(t)s_{Ra12}(t)\right)\right]=\frac{V_{BUS}}{4}s_{Ra,IN1}(t) \quad (107)$$

$$u_{a(sw),2}(t)=u_{a(sw),1}\left(t-\frac{T_{sw}}{2}\right)=\frac{V_{BUS}}{4}s_{Ra,IN1}\left(t-\frac{T_{sw}}{2}\right)=\frac{V_{BUS}}{4}s_{Ra,IN2}(t)$$
$$u_{a(sw)}(t)=\frac{u_{a(sw),1}(t)+u_{a(sw),2}(t)}{2}=\frac{V_{BUS}}{8}\left[s_{Ra,IN1}(t)+s_{Ra,IN2}(t)\right] \quad (108)$$

In general case, using interleaved topology, the number of the output voltage levels, $N_{L(OUT)}$, is given by the equation (109), where N_L is number of the level of the converter and N_C is the number of the interleaved cells.

$$N_{L(OUT)}=\left(N_L-1\right)\cdot N_C+1 \quad (109)$$

8.4 Output Inverter Analysis

The analysis carried out for the rectifier stage is valid even for the inverter stage. Fig. 118 shows the single-phase N5L E-Type Inverter and output filter. The

switches located in the leg 1, $\mathbf{S_{Iu}} \in \{S_{IuA}, S_{Iu11}, S_{Iu12}, S_{Iu21}, S_{Iu22}, S_{Iu31}, S_{Iu32}, S_{IuB}\}$ are driven by the switching functions $\mathbf{s_{Iu}(t)} \in \{s_{IuA}, s_{Iu11}, s_{Iu12}, s_{Iu21}, s_{Iu22}, s_{Iu31}, s_{Iu32}, s_{IuB}\}$.

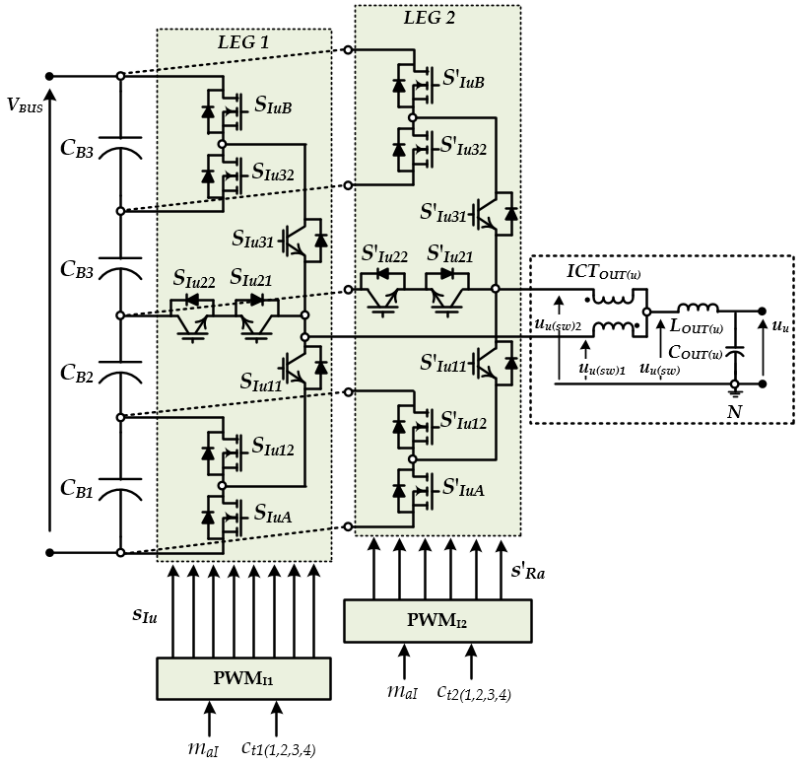


Fig. 118. Single-phase N5L E-Type Inverter and output filter.

The switching functions $\mathbf{s_{Iu}(t)}$ are defined over a switching period T_{sw} as in (110), where the duty cycles have been obtained in section 6.5.1. The switches organized in the leg 2, $\mathbf{S'_{Iu}} \in \{s'_{IuA}, s'_{Iu11}, s'_{Iu12}, s'_{Iu21}, s'_{Iu22}, s'_{Iu31}, s'_{Iu32}, s'_{IuB}\}$, are driven by the switching function $\mathbf{s'_{Iu}}(t) = \mathbf{s_{Iu}}(t - \frac{1}{2}T_{SW})$. The switching functions $\mathbf{s_{Iu}(t)}$ and $\mathbf{s'_{Iu}(t)}$ are generated by the pulse width modulators PWM_{I1} and PWM_{I2}, Fig. 118. The modulation scheme of the interleaved N5L E-Type Inverter is equal to the one we shown in Fig. 117. Each carrier controls two different power devices in opposite phase as listed in Table 20.

Table 20. Carriers versus power devices of the N5L E-Type Inverter.

Carriers	c_{t11}	c_{t12}	c_{t13}	c_{t14}	c_{t21}	c_{t22}	c_{t23}	c_{t24}
	Leg 1				Leg 2			
	S_{IuA}, S_{Iu12}	S_{Iu22}	S_{Iu21}	S_{IuB}, S_{Iu32}	S'_{IuA}, S'_{Iu12}	S'_{Iu22}	S'_{Iu21}	S'_{IuB}, S'_{Iu32}

$$
\begin{aligned}
s_{IuA}(\mathrm{t}) &= \begin{cases} 1 & 0 \le t \le d_{S_{IuA}}(t)\,\mathrm{T}_{SW} \\ 0 & d_{S_{IuA}}(t)\,\mathrm{T}_{SW} < t \le \mathrm{T}_{SW} \end{cases} \\
s_{Iu11}(\mathrm{t}) &= \begin{cases} 1 & 0 \le t \le d_{S_{Iu11}}(t)\,\mathrm{T}_{SW} \\ 0 & d_{S_{Iu11}}(t)\,\mathrm{T}_{SW} < t \le \mathrm{T}_{SW} \end{cases} \\
s_{Iu12}(\mathrm{t}) &= \begin{cases} 1 & 0 \le t \le d_{S_{Iu12}}(t)\,\mathrm{T}_{SW} \\ 0 & d_{S_{Iu12}}(t)\,\mathrm{T}_{SW} < t \le \mathrm{T}_{SW} \end{cases} \\
s_{Iu21}(\mathrm{t}) &= \begin{cases} 1 & 0 \le t \le d_{S_{Iu21}}(t)\,\mathrm{T}_{SW} \\ 0 & d_{S_{Iu21}}(t)\,\mathrm{T}_{SW} < t \le \mathrm{T}_{SW} \end{cases} \\
s_{Iu22}(\mathrm{t}) &= \begin{cases} 1 & 0 \le t \le d_{S_{Iu22}}(t)\,\mathrm{T}_{SW} \\ 0 & d_{S_{Iu22}}(t)\,\mathrm{T}_{SW} < t \le \mathrm{T}_{SW} \end{cases} \\
s_{Iu31}(\mathrm{t}) &= \begin{cases} 1 & 0 \le t \le d_{S_{Iu31}}(t)\,\mathrm{T}_{SW} \\ 0 & d_{S_{Iu31}}(t)\,\mathrm{T}_{SW} < t \le \mathrm{T}_{SW} \end{cases} \\
s_{Iu32}(\mathrm{t}) &= \begin{cases} 1 & 0 \le t \le d_{S_{Iu32}}(t)\,\mathrm{T}_{SW} \\ 0 & d_{S_{Iu32}}(t)\,\mathrm{T}_{SW} < t \le \mathrm{T}_{SW} \end{cases} \\
s_{IuB}(\mathrm{t}) &= \begin{cases} 1 & 0 \le t \le d_{S_{IuB}}(t)\,\mathrm{T}_{SW} \\ 0 & d_{S_{IuB}}(t)\,\mathrm{T}_{SW} < t \le \mathrm{T}_{SW} \end{cases}
\end{aligned}
\tag{110}
$$

The output-to-neutral switching voltage of the leg 1 and leg 2, $v_{u(sw),1}$ and $v_{u(sw),2}$, are given in (111). The equivalent output voltage $v_{u(sw)}$ is reported in (112). As well as for the input-to-neutral switching voltage, even the equivalent output voltage $u_{u(sw)}$ is composed by nine-level voltage.

$$
\begin{aligned}
u_{u(sw),1} = \frac{V_{BUS}}{4}(1-s_{Iu21})(1-s_{Iu22})\left[s_{Iu31}s_{Iu32} + 2s_{Iu31}s_{IuB} - 3s_{Iu31}s_{Iu32}s_{IuB}\right] + \\
-\left[s_{Iu11}s_{Iu12} + 2s_{Iu11}s_{IuA} - 3s_{Iu11}s_{Iu12}s_{IuA}\right] = \frac{V_{BUS}}{4}s_{Iu,\mathrm{OUT}1}(t)
\end{aligned}
\tag{111}
$$

$$
\begin{aligned}
u_{u(sw),2}(t) = u_{u(sw),1}\left(t - \frac{T_{sw}}{2}\right) = \frac{V_{BUS}}{4}s_{Iu,\mathrm{OUT}1}\left(t - \frac{T_{sw}}{2}\right) = \frac{V_{BUS}}{4}s_{Iu,\mathrm{OUT}2}(t) \\
u_{u(sw)}(t) = \frac{u_{u(sw),1}(t) + u_{u(sw),2}(t)}{2} = \frac{V_{BUS}}{8}\left[s_{Iu,\mathrm{OUT}1}(t) + s_{Iu,\mathrm{OUT}2}(t)\right]
\end{aligned}
\tag{112}
$$

Input Filter Analysis

The input inductor current is defined as in (113), where I_{IN} is the fundamental

current and $\Delta i_{La}(t)$ is high frequency current ripple.

$$i_{La}(\mathrm{t}) = \sqrt{2} I_{IN} \sin(\omega_{IN} t) + \Delta i_{La}(t) \tag{113}$$

Let's assume an ideal ICT. In this condition, all flux generated by the primary winding and/or the secondary winding links all the turns of every windings, including itself. Thus, considering the ICT as fully symmetrical and the switching cells as identical, the output inductor current is shared equally between leg 1 and leg 2, $i_{a1}=i_{a2}$ (see Fig. 119).

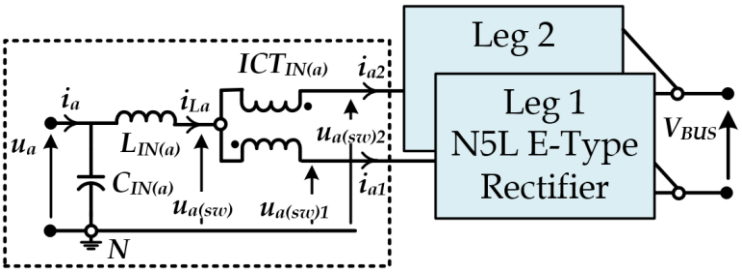


Fig. 119. Single-phase equivalent circuit diagram of the input filter.

The input cell (or leg) current can be written as in (114), where I_{IN} is the fundamental current and $\Delta i_{La}(t)$ is high frequency current ripple.

$$i_{a1}(t) = i_{a2}(t) = \frac{i_{La}(\mathrm{t})}{2} = \frac{\sqrt{2}}{2} I_{IN} \sin(\omega_{IN} t) + \frac{1}{2} \Delta i_{La}(t) \tag{114}$$

It can be noted from the equation (114) that the current ripple of each transformer winding is ½ of the output inductor current ripple. The equivalent circuit diagram of the input rectifier is depicted in Fig. 120. The circuit consists of the grid voltage source v_a, the grid equivalent impedance Z_{Grid}, the input filter inductance $L_{IN(a)}$, the input filter capacitance $C_{IN(a)}$ and the rectifier equivalent input voltage $v_{a(sw)}$ (108).

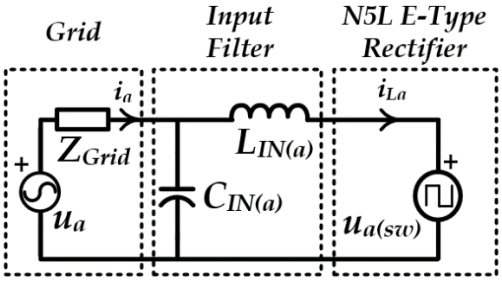


Fig. 120. Equivalent circuit diagram of the input filter.

Maximum peak-to-peak current ripple [165], $\Delta i_{La,max}$, is given in (115).

$$\Delta i_{La,\max} = \left(\frac{V_{BUS}}{4}\right)\frac{1}{16 f_{sw} L_{IN(a)}} \tag{115}$$

The selection of the input inductance and capacitance values are based on several criteria.

8.4.1 RMS current ripple

The RMS current ripple over a fundamental period has been expressed in (116).

$$\Delta i_{La,RMS} = \sqrt{\frac{1}{T}\int_0^T \left(\frac{\Delta i_{La,pp}(t)}{2\sqrt{3}}\right)^2 dt} \cong \frac{\Delta i_{La,\max}}{2\sqrt{3}} 0.9 \tag{116}$$

Substituting (115) into (116), yields the filter minimum inductance (117).

$$L_{IN,a} \geq \frac{V_{BUS}}{4}\frac{1}{16 f_{sw}}\frac{0.9}{2\sqrt{3}\Delta i_{La,RMS}} \tag{117}$$

8.4.2 The input current THD

The input current total harmonic distortion THD_i is defined in (118), where $I_{a(k)}$ is the harmonic RMS current of order k and $I_{a(1)}$ is the first harmonic (fundamental) RMS current.

$$THD_i = 100\frac{\sqrt{\sum_{k=2}^{\infty} I_{a(k)}^2}}{I_{a(1)}} \tag{118}$$

Assuming the rectifier input (grid) current is properly controlled in a way to eliminate all the harmonics up to fundamental frequency, the THD_i is defined by the switching frequency current ripple only, (119), where $I_{N,RMS}$ is the nominal RMS current.

$$THD_i = 100\frac{\Delta i_{La,RMS}}{I_{N,RMS}} \tag{119}$$

The current ripple Δi_{La} is a periodic function of period $\frac{1}{2}T_{sw}$ (where $T_{sw}=1/f_{sw}$) and it can be expanded in Fourier series. It could be proven, the current ripple can be

approximated by an equivalent first harmonic (120), where $\Delta i_{La,RMS}$ is the RMS current ripple (116).

$$\Delta i_{La}(t) \cong \sqrt{2}\Delta i_{La,RMS} \sin(2\omega_{sw} t) \tag{120}$$

The grid RMS current ripple can be approximated by equation (121), where *A(1)* is the filter attenuation at the first harmonic. Substituting (119) into (121) yields the filter desired attenuation (122). Substituting (115) and the filter attenuation function into (122) yields the filter parameters (123).

$$\Delta i_{La,RMS}(t) \cong \frac{0.9 \cdot A(1)}{2\sqrt{3}} \Delta i_{La,\max} \tag{121}$$

$$A(1) = \frac{2\sqrt{3} \cdot THD_i \cdot I_{N,RMS}}{90 \cdot \Delta i_{La,\max}} \tag{122}$$

$$L_{Grid} C_{IN(a)} L_{IN(a)} = \frac{V_{BUS}}{4^4 2\pi^2 f_{sw}^3} \frac{1}{2\sqrt{3}} \frac{100}{THD_i} \frac{0.9}{I_{N,RMS}} \tag{123}$$

8.4.3 The capacitor current stress

The capacitor current is composed of two components, namely the fundamental frequency current and the equivalent switching frequency current ripple. Total RMS current is (124), where V_{IN} is the RMS input voltage. Substituting (115) and (116) into (124), yields minimum required filter inductance (125).

$$I_{C_{IN(a),RMS}} = \sqrt{\left(\frac{0.9}{2\sqrt{3}} \Delta i_{La,\max}\right)^2 + \left(V_{IN} C_{IN(a)} \omega_{IN}\right)^2} \tag{124}$$

$$L_{IN(a)} \geq \frac{0.9}{2\sqrt{3}} \frac{V_{BUS}}{4} \frac{1}{16 f_{sw}} \frac{1}{\sqrt{\left(I_{C_{IN(a),RMS}}\right)^2 - \left(V_{IN} C_{IN(a)} \omega_{IN}\right)^2}} \tag{125}$$

8.4.4 The inductor current

The inductor current is defined in (126). The fundamental frequency RMS current is given in (127).

$$i_{LIN(a)}(t) = \sqrt{2} I_{IN} \sin(\omega_{IN} t) + \sqrt{2} \frac{0.9}{2\sqrt{3}} \Delta i_{La,\max} \sin(2\omega_{sw} t) + \\ + \sqrt{2} V_{IN} C_{IN(a)} \omega_{IN} \cos(\omega_{IN} t) \tag{126}$$

Substituting (126) into (117), yields (128), where the minimum filter inductance satisfies the maximum allowed RMS current for the filter inductor.

$$I_{La,RMS} = \sqrt{(I_{IN})^2 + (V_{IN} C_{IN(a)} \omega_{IN})^2 + (\Delta i_{La,RMS})^2} \tag{127}$$

$$L_{IN,A} \geq \frac{0.9}{2\sqrt{3}} \frac{V_{BUS}}{4} \frac{1}{16 f_{sw}} \frac{1}{\sqrt{I_{La,RMS}^2 - I_{IN}^2 - (V_{IN} C_{IN(a)} \omega_{IN})^2}} \tag{128}$$

8.5 The Input Capacitor and Inductor Selection

From the above analysis, the initial value for the calculations of the input filter is the maximum allowed current ripple on the filter inductor and filter capacitors. The capacitance $C_{IN(a)}$ is chosen starting from the acceptable reactive power of the filter. The capacitance value is calculated in order to limit the capacitor reactive power at 1% of the full load power. This value allows maintaining high power factor even in the case of light load.

$$C_{IN(a)} = 0.01 \frac{I_{IN}}{2\pi f_{IN} V_{IN}} \tag{129}$$

The grid inductance L_{Grid} is given as the system parameter and we have no influence on it. The inductance $L_{IN(a)}$ can be selected considering the maximum value obtained by the equation (117) and (123).

$$L_{IN,A} = \max \begin{cases} \frac{V_{BUS}}{4} \frac{1}{16 f_{sw}} \frac{0.9}{2\sqrt{3} \Delta i_{La,RMS}} \\ \frac{V_{BUS}}{4^4 2\pi^2 f_{sw}^3 L_{Grid} C_{IN(a)}} \frac{1}{2\sqrt{3}} \frac{100}{THD_i} \frac{0.9}{I_{N,RMS}} \end{cases} \tag{130}$$

The inductance $L_{IN(a)}$ has to be selected for maximum peak-to-peak current ripple given as the inductor design parameter.

Table 21. Input parameters of the three-phase N5L E-Type BTB Converter

Input RMS Voltage V_{IN}	[V]	230
Input RMS Current I_{IN}	[A]	28.99
Input Frequency f_{IN}	[Hz]	50
Input Current THD_i	[%]	3
Grid Inductance L_{Grid}	[µH]	50
Power Factor	-	1
Maximum peak-to-peak current ripple, $\Delta i_{La,max}$	[A]	8.7
RMS current ripple $\Delta i_{La,RMS}$	[A]	2.26

Considering the input parameters shows in Table 21 and equation (129) and (130) the design results are summarized in the table below.

Table 22. Input Filter capacitor and inductance selection.

Criteria	Equation	Value
Acceptable reactive power	$C_{IN(a)} = 0.01\frac{I_{IN}}{2\pi f_{IN} V_{IN}}$	4.01 µF
RMS current ripple, $L_{IN(a)}$	$L_{IN,A} = \frac{V_{BUS}}{4}\frac{1}{16 f_{sw}}\frac{0.9}{2\sqrt{3}\Delta i_{La,RMS}}$	55.40 µH
Input Current THD_i, $L_{IN(a)}$	$L_{IN,A} = \frac{V_{BUS}}{4^4 2\pi^2 f_{sw}^3 L_{Grid} C_{IN(a)}}\frac{1}{2\sqrt{3}}\frac{100}{THD_i}\frac{0.9}{I_{N,RMS}}$	15.79 µH

According to this analysis, the input inductance $L_{IN(a)}$ and the input capacitor $C_{IN(a)}$ are chosen equal to 60 µH and 4.7 µF, respectively.

8.6 Output Filter Analysis

In Section 8.4 the structure of the output inverter has been analyzed. Let's consider an equivalent circuit of the 1ΦN5L E-Type Inverter and output filter, Fig. 121.

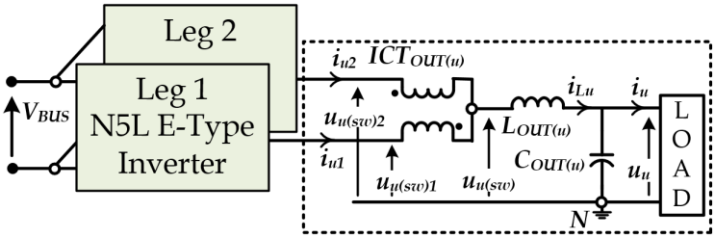


Fig. 121. Equivalent circuit of the 1ΦN5L E-Type Inverter and output filter.

The output inductor current is defined as in (131), where I_{OUT} is the fundamental

current and $\Delta i_{Lu}(t)$ is high frequency current ripple.

$$i_{Lu}(\mathrm{t}) = \sqrt{2} I_{OUT} \sin(\omega_{OUT} t) + \Delta i_{Lu}(t) \tag{131}$$

Assuming an ideal ICT and identical switching cells, the output cell (or leg) current can be written as in (132).

$$i_{u1}(t) = i_{u2}(t) = \frac{i_{Lu}(\mathrm{t})}{2} = \frac{\sqrt{2}}{2} I_{OUT} \sin(\omega_{OUT} t) + \frac{1}{2} \Delta i_{Lu}(t) \tag{132}$$

For sake of simplicity let's consider the equivalent circuit diagram of the output filter, Fig. 122. The equivalent output filter circuit consists of the equivalent voltage source of the inverter $v_{u(sw)}$ (see equation (112)), the output inductance $L_{OUT(u)}$ and the output capacitor $C_{OUT(u)}$.

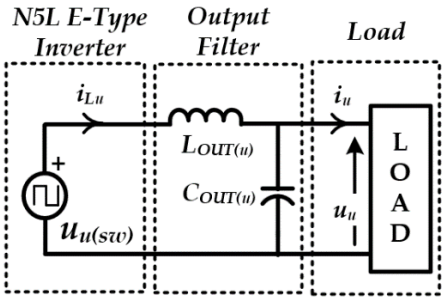


Fig. 122. Equivalent circuit diagram of the output filter.

The equation (115) is valid also for the output stage; thus, the peak-to-peak maximum current ripple, $\Delta i_{Lu,max}$, can be written in (133).

$$\Delta i_{Lu,\max} = \left(\frac{V_{BUS}}{4}\right) \frac{1}{16 f_{sw} L_{OUT(\mathrm{u})}} \tag{133}$$

The main design objective is to select the inductance $L_{OUT(a)}$ and capacitance $C_{OUT(a)}$ to achieve the output voltage THD_v required. To do this, several criteria have been considered.

8.6.1 RMS current ripple, capacitor current stress and inductor current

The equations (117),(125) and (128) can also be obtained for the output stage filter. Therefore, the output equivalent inductance as a function of the RMS current ripple, the capacitor current stress and inductor current have been

obtained in (134), (135) and (136), where V_{OUT} is the RMS output voltage, I_{OUT} is the RMS output current and ω_{OUT} is the output frequency.

$$L_{OUT(a)} \geq \frac{V_{BUS}}{4} \frac{1}{16 f_{sw}} \frac{0.9}{2\sqrt{3}\Delta i_{Lu,\mathrm{RMS}}} \tag{134}$$

$$L_{OUT(u)} \geq \frac{0.9}{2\sqrt{3}} \frac{V_{BUS}}{4} \frac{1}{16 f_{sw}} \frac{1}{\sqrt{I^2_{C_{OUT(u)},RMS} - \left(V_{OUT} C_{OUT(u)} \omega_{OUT}\right)^2}} \tag{135}$$

$$L_{OUT(a)} \geq \frac{0.9}{2\sqrt{3}} \frac{V_{BUS}}{4} \frac{1}{16 f_{sw}} \frac{1}{\sqrt{\left(I_{Lu,RMS}\right)^2 - \left(I_{OUT}\right)^2 - \left(V_{OUT} C_{OUT(u)} \omega_{OUT}\right)^2}} \tag{136}$$

8.6.2 The output voltage THD

The output voltage total harmonic distortion THD_v is defined by (137), where $U_{u(k)}$, is a harmonic RMS of order k and $U_{u(1)}$ is the first fundamental RMS voltage.

$$THD_v = 100 \frac{\sqrt{\sum_{k=2}^{\infty} U^2_{u(k)}}}{U_{u(1)}} \tag{137}$$

$$THD_v = 100 \frac{\Delta u_{u,RMS}}{U_{N,\mathrm{RMS}}} \tag{138}$$

Let's assume the output voltage is properly controlled and all the harmonics of the fundamental frequency are eliminated by the control. In that case, the THD_v is defined by the equivalent switching frequency voltage ripple (138), where $\Delta v_{u,RMS}(t)$ is the output voltage RMS ripple and $U_{N,RMS}$ is the nominal RMS voltage.

If the switching frequency is sufficiently higher than the fundamental frequency, the expression (139) can be obtained.

$$\Delta u_{u,RMS}(t) = \frac{0.9}{2\sqrt{3}4\omega_{sw} C_{OUT(u)}} \Delta i_{Lu,\max}(t) \tag{139}$$

Substituting (133) into (139) yields the inductor/capacitor pair (140) for given THD_v criteria.

$$C_{OUT(u)}L_{OUT(u)} \geq \frac{V_{BUS}}{4}\frac{1}{2^7\sqrt{3}\pi f_{sw}^2}\frac{100}{THD_v}\frac{0.9}{U_{N,\mathrm{RMS}}} \tag{140}$$

8.6.3 Peak to peak output voltage ripple

The output voltage peak to peak ripple is given by (141). From (141), the maximum allowed peak to peak current ripple for given output voltage peak to peak ripple and filter capacitor $C_{OUT(u)}$ has been computed (142). Substituting (133) into (142), yields the capacitor/inductor pair (143).

$$\Delta u_{u,pp} = \frac{1}{16}\frac{\Delta i_{u,pp}}{f_{sw}C_{OUT(u)}} \tag{141}$$

$$\Delta i_{u,\max} \leq \Delta u_{u,pp} 16 f_{sw} C_{OUT(u)} \tag{142}$$

$$C_{OUT(u)}L_{OUT(u)} \geq \frac{V_{BUS}}{4}\frac{1}{2^8 f_{sw}^2 \Delta u_{u,pp}} \tag{143}$$

8.7 The Output Capacitor and Inductor Selection

The maximum capacitance $C_{OUT(u)}$ is selected according to the criterion of maximum reactive power of the filter. The filter capacitor is selected according to reactive power value of 1% of the full load power.

$$C_{OUT(u)} = 0.01\frac{I_{OUT}}{2\pi f_0 V_{OUT}} \tag{144}$$

The inductance $L_{OUT(u)}$ has to be selected for maximum peak-to-peak current ripple given as the inductor design parameter. The inductance $L_{OUT(u)}$ can be selected considering the maximum value obtained by the equation (134), (140) and (143). Considering the input parameters shows in Table 23and equation (144) and (145) the design results filter capacitor and inductance of the are summarized in Table 24.

$$L_{OUT(u)} = \max\begin{cases} \dfrac{V_{BUS}}{4}\dfrac{1}{16 f_{sw}}\dfrac{0.9}{2\sqrt{3}\Delta i_{Lu,\mathrm{RMS}}} \\ \dfrac{V_{BUS}}{4}\dfrac{1}{2^7\sqrt{3}\pi f_{sw}^2 C_{OUT(u)}}\dfrac{100}{THD_v}\dfrac{0.9}{U_{N,\mathrm{RMS}}} \\ \dfrac{V_{BUS}}{4}\dfrac{1}{2^8 f_{sw}^2 \Delta u_{u,pp} C_{OUT(u)}} \end{cases} \tag{145}$$

Table 23. Output parameters of the three-phase N5L E-Type BTB Converter

Output RMS Voltage V_{OUT}	[V]	230
Output RMS Current I_{OUT}	[A]	28.99
Output Frequency f_{OUT}	[Hz]	50
Output Voltage THD_v	[%]	1
Output Power P_{out}	[kW]	20
Power Factor	-	1
Maximum peak-to-peak current ripple, $\Delta i_{Lu,max}$	[A]	8.7
RMS current ripple $\Delta i_{Lu,RMS}$	[A]	2.26

Table 24. Input Filter capacitor and inductance selection.

Criteria	Equation	Value
Acceptable reactive power	$C_{OUT(u)} = 0.01\dfrac{I_{OUT}}{2\pi f_{sw} V_{OUT}}$	4.01 µF
RMS current ripple, $L_{OUT(u)}$	$L_{OUT(a)} = \dfrac{V_{BUS}}{4}\dfrac{1}{16 f_{sw}}\dfrac{0.9}{2\sqrt{3}\Delta i_{Lu,\mathrm{RMS}}}$	55.40 µH
Output Voltage THD_v, $L_{OUT(u)}$	$L_{OUT(u)} = \dfrac{V_{BUS}}{4}\dfrac{1}{2^7\sqrt{3}\pi f_{sw}^2 C_{OUT(u)}}\dfrac{100}{THD_v}\dfrac{0.9}{U_{N,\mathrm{RMS}}}$	44.98 µH
Peak to peak output voltage ripple, $L_{OUT(u)}$	$L_{OUT(u)} = \dfrac{V_{BUS}}{4}\dfrac{1}{2^8 f_{sw}^2 \Delta u_{u,pp} C_{OUT(u)}}$	5.54 µH

According to this analysis, the output inductance $L_{OUT(u)}$ and the output capacitor $C_{OUT(u)}$ are chosen equal to 60 µH and 4.7 µF, respectively.

8.8 ICT Analysis

In this section we will address the analysis of the ICT. The key factor to select the ICT core is the area-product (AP) factor. The AP factor is given in (146), where A_E is the core effective cross-section area and A_W is the core winding

window area.

$$AP = A_E A_W \ \left[\mathrm{m}^4\right] \tag{146}$$

Considering the equivalent circuit of the 1ΦN5L E-Type Inverter and output filter and the equation (110), the ICT total flux can be written as in (147), where V_{BUS} is the DC-bus voltage, n is the number of turns, A_E is the core effective cross-section area (m^2), f_{sw} is the switching frequency (kHz) and k_d is a coefficient that depends on the duty cycle d.

$$\begin{aligned} B_{peak} &= \frac{\Delta\psi}{2nA_E} = \frac{V_{BUS}}{4}\frac{1}{4nA_E f_{sw}}\left[d + (1-2d)\,floor(2d)\right] = \\ &= B_{\max}\left[d + (1-2d)\,floor(2d)\right] \end{aligned} \tag{147}$$

Starting from the peak flux density B_{peak} we can obtain the core cross-section A_E as in (148).

$$A_E = \frac{V_{BUS}}{4}\frac{1}{4nB_{peak}\left(f_{sw}10^{-3}\right)}\left[d + (1-2d)\,floor(2d)\right]\ \left[\mathrm{m}^2\right] \tag{148}$$

In this case, the ICT works with a fraction of the DC-bus voltage (¼V_{BUS}) and having two cells interleaved the worst condition occurs when the duty cycle is 0.5. Thus, the cross-section area can be written as in (149).

$$A_E = \frac{V_{BUS}}{4}\frac{1}{8nB_{peak}\left(f_{sw}10^{-3}\right)}\bigg|_{d=0.5}\ \left[\mathrm{m}^2\right] \tag{149}$$

The core winding window is defined in (150), where I_{RMS} is the winding RMS current (A), J is the current density (A/m^2) and k_{FL} is the winding coefficient.

$$A_W = \frac{2nI_{RMS}}{Jk_{FL}} \tag{150}$$

The factor k_{FL} depends on the wire profile and winding technique. When the ICT winding is made with a flat wire k_{FL} is included in the range 0.6-0.8. On the other hand, when the ICT winding is made with a litz wire k_{FL} is included in the range 0.2-0.4. Substituting (149) and (150) into (148), we can obtain the AP factor as in (151).

$$AP = \frac{V_{BUS}/4}{8nB_{peak}f_{sw}}\frac{2nI_{RMS}}{Jk_{FL}}\ \left[\mathrm{m}^4\right] \tag{151}$$

Then, having the area-product we can pre-select the appropriate ICT core. After that, we can compute the number of turns and the cross-section of the winding wire as given in (152) and (153), respectively.

$$n = \frac{V_{BUS} \big/ 4}{8 A_E B_{peak} f_{sw}} \tag{152}$$

$$A_{cu} = \frac{A_W k_{FL}}{2n} \tag{153}$$

8.8.1 ICT losses

The ICT core losses $P_{ICT,C}$ can be defined by the Steinmetz's equation as in (154), where B_{peak} is the flux density peak, (T), k_p, a, and β are the coefficients given by the core manufacturer, f_{sw} is the switching frequency, (kHz) and m_C is the core mass, (kg).

$$P_{ICT,C} = m_C k_p B_{peak}^{\alpha} \left(f_{sw} \right)^{\beta} \tag{154}$$

The winding losses are given by the currents flowing through the windings. The winding resistance R_0 depends by the winding geometry and the number of turns. The winding resistance at low frequency $R_{0(DC)}$ can be obtained as in (155), where ρ is resistivity that depends on the material of the conductor and its temperature, L_W is the wire length of the winding and A_{cu} is cross-section of the winding wire.

$$R_{0(DC)} = \rho \frac{L_W}{A_{cu}} \tag{155}$$

Thus, the windings losses at steady state can been obtained as in (156), where I_{RMS} is the winding RMS current.

$$P_{CU,1} = P_{CU,2} = R_{0(DC)} I_{RMS}^2 \tag{156}$$

The total ICT losses are given in (157)

$$P_{ICT} = m_C k_p B_{peak}^{\alpha} \left(f_{sw} \right)^{\beta} + 2 R_{0(DC)} I_{RMS}^2 \tag{157}$$

In order to determine the best trade-off between total losses, cross section area as well as shape and the number of turns, the optimized ICT design procedure has

been carried out.

8.8.2 ICT Thermal Model

As shown in [157], the ICT core and winding temperatures at steady state can be obtained as in (158), where:

- P_C are the core losses,
- P_{CU1} are the first winding losses,
- P_{CU2} are the second winding losses,
- R_{CC} is the thermal resistance core to ambient (K/W),
- R_{W1W1} is the thermal resistance first winding to ambient (K/W),
- R_{W2W2} is the thermal resistance second winding to ambient (K/W),
- R_{W1C}, R_{W1W2}, R_{CW1}, R_{CW2}, R_{W2W1}, R_{W2C} are the mutual thermal impedances(K/W).

The thermal model of the ICT is shown in Fig. 123.

$$\begin{aligned}\theta_{W1} &= P_{CU1}R_{W1W1} + P_C R_{W1C} + P_{CU2}R_{W1W2} + \theta_{amb}\\ \theta_C &= P_{CU1}R_{CW1} + P_C R_{CC} + P_{CU2}R_{CW2} + \theta_{amb}\\ \theta_{W2} &= P_{CU1}R_{W2W1} + P_C R_{W2C} + P_{CU2}R_{W2W2} + \theta_{amb}\end{aligned} \tag{158}$$

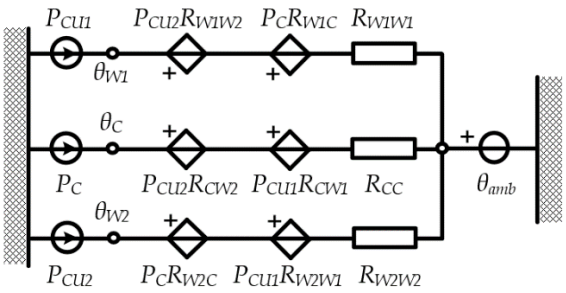


Fig. 123. Thermal model of the ICT.

The thermal resistances strongly depend on the ICT geometry core and winding geometry, cooling method, and temperature [157].

8.9 Inductor Analysis

The selection process of the inductors L_{IN} and L_{OUT} is the same as the design for the ICT. The inductance L_{IN} and L_{OUT} are designed in order to obtain 60 µH

at the nominal load, as analyzed in the previous sections (see Table 22 and Table 24). The core selection criteria are based on the AP factor. The core cross-section A_E are given in (159), where i_{0peak} is the peak current of the inductor, L_0 is the inductance at the peak current, n is the number of turns and B_{peak} is the core peak flux density.

$$A_E = \frac{L_0 i_{0peak}^2}{n B_{peak}} \tag{159}$$

The winding window is defined in (160), where $I_{L,RMS}$ is the winding RMS current, J is the current density and k_{FL} is the winding coefficient.

$$A_W = \frac{n I_{L,RMS}}{J k_{FL}} \tag{160}$$

If we consider the input inductance, from the equation (113) we can obtain the winding RMS current as (161), where I_{IN} is the input RMS current and $\Delta i_{La,RMS}$ is the input RMS current ripple over a fundamental period as defined in (116).

$$I_{L,RMS} = \sqrt{I_{IN}^2 + \Delta i_{La,RMS}^2} \tag{161}$$

considering the equation (131), similar expression of the winding RMS current can be achieved, as in (162) where I_{OUT} is the output RMS current and $\Delta i_{Lu,RMS}$ is the output RMS current ripple over a fundamental period.

$$I_{L,RMS} = \sqrt{I_{OUT}^2 + \Delta i_{Lu,RMS}^2} \tag{162}$$

Let's suppose that $I_{IN}=I_{OUT}=I_0$ and $\Delta i_{La,RMS}=\Delta i_{Lu,RMS}=\Delta i_{L0,RMS}$. Substituting (159), (160), (161) yields to the inductor AP factor, as in (163).

$$AP = \frac{L_0 i_{0peak}^2}{B_{peak}} \frac{\sqrt{I_0^2 + \Delta i_{L0,RMS}^2}}{J k_{FL}} \tag{163}$$

Starting from the choice of the peak flux density B_{peak}, the current density J, the inductance L_0 and the winding coefficient k_{FL}, we can compute the AP factor and select the inductor core. After that, we can calculate:

- the number of turns as in (164), where L_0 is the inductance at the peak current and A_L is the inductance factor (nH/n^2) provided by the manufacturer;

$$n = \sqrt{\frac{L_0}{A_L}} \tag{164}$$

- the cross-section of the winding wire as in (165).

$$A_{cu} = \frac{A_W k_{FL}}{n} \tag{165}$$

8.9.1 Inductor Losses

The inductor losses are split in core losses and copper losses. As well as for ICT core losses, the inductor losses are given by the Steinmetz's equation defined in (154). The copper losses are obtained in (166), where $R_{0L(DC}$ is the winding resistance at a low frequency given in (167) and I_0 is the RMS current flow through the inductor.

$$P_{CU} = R_{0L(DC)} I_0^2 \tag{166}$$

$$R_{0L(DC)} = \rho \frac{L_W}{A_{cu}} \tag{167}$$

In equation (167) ρ is the resistivity that depends on the material of the conductor and its temperature, L_W is the wire length of the windings and A_{cu} is cross-section of the winding wire. The total inductor losses are given in (168), where B_{peak} is the flux density peak, (T), k_p, a, and β are the coefficients given by the core manufacturer, f_{sw} is the switching frequency, (kHz) and m_C is the core mass, (kg).

$$P_L = m_C k_p B_{peak}^{\alpha} \left(f_{sw} \right)^{\beta} + R_{L0(DC)} I_0^2 \tag{168}$$

8.9.2 Inductor Thermal Model

As shown in [157], the inductor core and winding temperatures at steady state can be obtained as in (169), where P_C is the core losses, R_C is the thermal resistance core to ambient (K/W), R_W is the thermal resistance winding to ambient (K/W), and R_{CW} is the thermal resistance core to winding (K/W).

$$\theta_C = R_{CC} P_C + R_{CW} P_{CU} + \theta_{amb} \tag{169}$$

$$\theta_W = R_{CW} P_C + R_{WW} P_{CU} + \theta_{amb}$$

The thermal mode of the inductor is shown in Fig. 124. The thermal resistances strongly depend on the inductor geometry core and winding geometry, cooling method, and temperature [157].

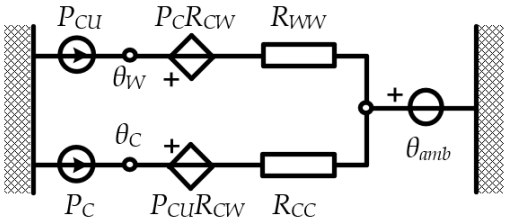


Fig. 124. Thermal model of the inductor.

9 DC-BUS ANALYSIS

9.1 Introduction

The DC-bus capacitor is selected on the basis of several criteria:

1. DC-bus capacitor RMS current
2. DC-bus voltage ripple

The analysis starts with the RMS current computation in the DC-bus capacitors. This current is determined by the modulation depth and by the amplitude and the phase angle of the inverter output, assuming a sinusoidal inverter output current and a constant DC-bus voltage. The DC-bus capacitors should be able to handle the voltage ripple under all N5L E-Type BTB Converter operating conditions. In this design, as well as in advanced design (such as active back-to-back topology), the transition time from the normal operation to the battery mode is in the order of hundreds of microseconds. Therefore, given the short transition time, the hold-up time is not considered as a critical requirement and it can be neglected in the design.

9.2 DC-Bus Capacitors Voltage Balancing

As mentioned in chapter I, the main issue of the E-Type and T-Type multilevel topologies and their variants is the unequal voltage sharing among the series connected capacitors that results in DC-bus capacitors unbalancing. The same thing happens in the N5L E-Type BTB Converter. Let's consider the equivalent circuit diagram of the DC-bus capacitors, Fig. 125. It is possible to identify three nodes:

1) Bottom-node,

2) Middle-node,

3) Top-node.

The rectifier and inverter inject currents i_1, i_2, and i_3 into the DC-bus, where the

injected currents are given in (170).

$$i_1(t) = i_{1R}(t) - i_{1I}(t),\ \ i_2(t) = i_{2R}(t) - i_{2I}(t),\ \ i_3(t) = i_{3R}(t) - i_{3I}(t) \tag{170}$$

In the 3-phase 3-wire converter, the middle-node average current $i_{2(AVG)}$ depends on the modulation offset m_0 [39] according to the equation (171), where T is the fundamental period and K_0 is a coefficient that is related to the rectifier and inverter currents.

$$\langle i_2 \rangle = \frac{1}{T}\int_0^T (i_{2R} - i_{2I})dt = m_0 K_0 \tag{171}$$

The N5L E-Type BTB Converter is composed of 3-phase and 4-wire. Thus, the modulation index offset m_0 is zero. Consequently, the condition (172) can be achieved.

$$v_{CB1} + v_{CB2} = v_{CB3} + v_{CB4} \tag{172}$$

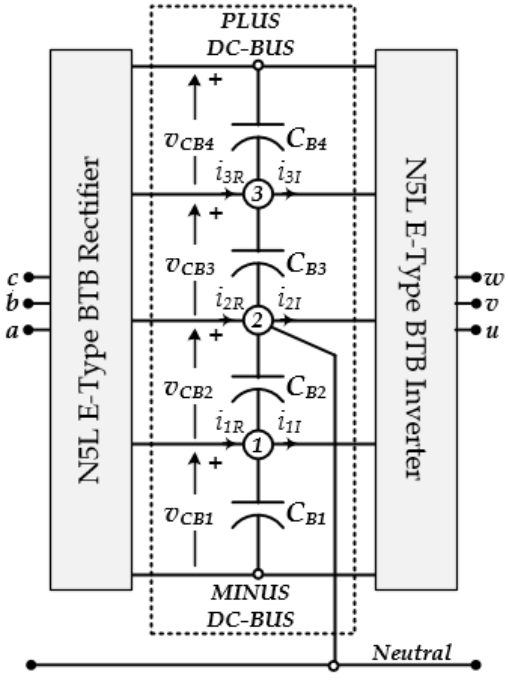


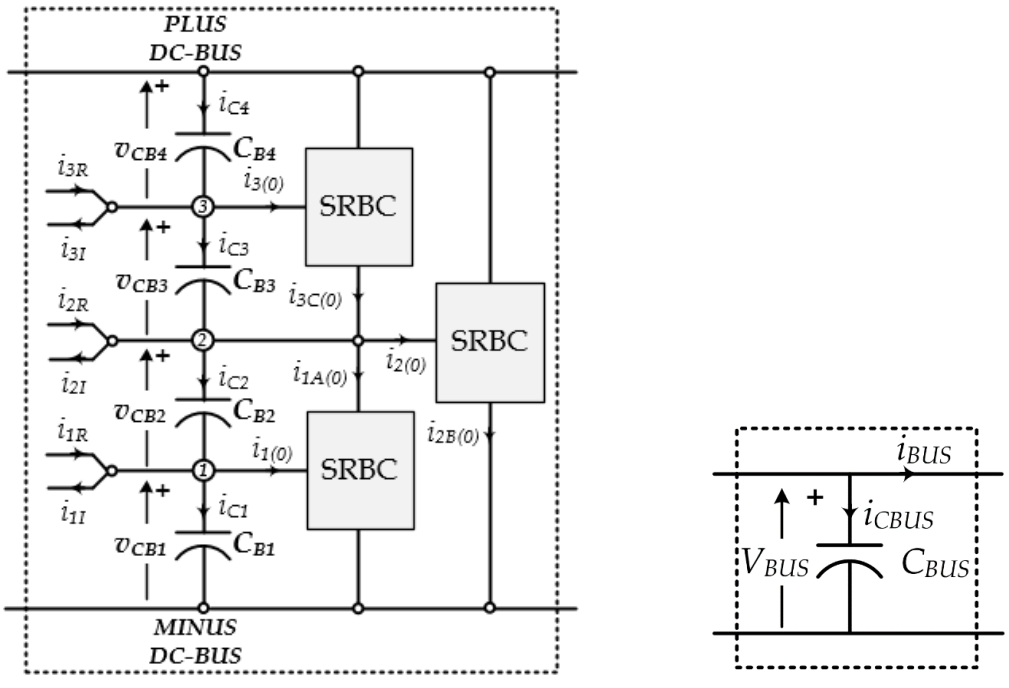
Fig. 125. Equivalent circuit of the converter DC Bus capacitors.

The equation (172) does not guarantee that the voltages across C_{B1} (C_{B3}) and C_{B2} (C_{B4}) are equal. The average values of the bottom-node current i_1 and the top-node average current i_3 are zero only in an ideal case when the rectifier and inverter modulation depths are identical. Therefore, it is not possible to control the top-

node and bottom-node currents, $i_{1(AVG)}$ and $i_{3(AVG)}$ through the modulation offset. The currents $i_{1(AVG)}$ and $i_{3(AVG)}$ must be controlled using an additional circuit. For this reason, the Series Resonant Balancing Circuit (SRBC) [63] can be used to balance the bottom and the top side partial DC-bus voltages v_{CB1}=v_{CB2} and v_{CB3}=v_{CB4}.

9.3 DC-bus instantaneous current

Let's assume that three SRBC are connected across the DC-bus capacitors, as shown in Fig. 126a. Two SRBC rejects the currents $i_1(t)$ and $i_3(t)$ (SRBC 1 and SRBC 3) and the third SRBC (SRBC 2) is used to balance the neutral current. In this condition, we can achieve four equal currents in the DC-bus capacitors, i_{CB1}= i_{CB2}= i_{CB3}=i_{CB4}=i_{BUS}. As a consequence, we have an equal distribution of the partial node voltage across C_{B1}, C_{B2}, C_{B3}, C_{B4}, namely v_{CB1}=v_{CB2} =v_{CB3}=v_{CB4}. Fig. 126b shows the simplified circuit of the DC-bus capacitors.



(a) (b)

Fig. 126. a) Equivalent circuit diagram of the converter DC-bus capacitors, b) simplified circuit of the DC-bus capacitors.

Let's assume that one current load flows through only one phase, as shown in (173).

$$\begin{cases} i_u(\mathrm{t}) = \sqrt{2} I_{OUT} \sin\left(\omega_{OUT} t - \varphi_{OUT}\right) \\ i_v(\mathrm{t}) = 0 \\ i_w(\mathrm{t}) = 0 \end{cases} \quad (173)$$

The DC-bus instantaneous current $i_{BUS}(t)$ over a fundamental period T_0 is depicted in Fig. 127.

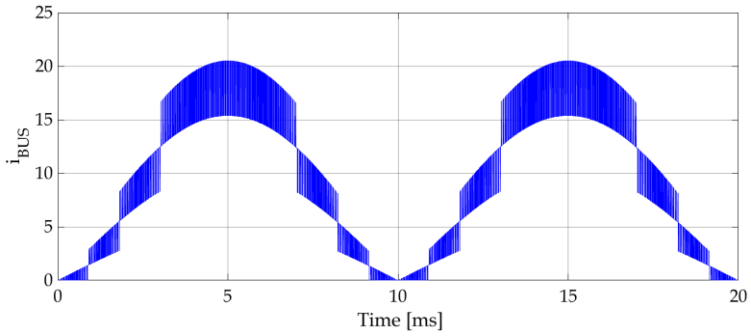


Fig. 127. DC-bus instantaneous current $i_{BUS}(t)$ waveform, with V_{OUT}=230V, cosφ_{OUT} =1 and V_{BUS}=700V, M_0=0.93, f_{OUT}=50 Hz, f_{sw}=24 kHz, I_{OUT}=28.99 A.

DC-bus instantaneous current is composed by two terms: low frequency current i_{LF}, related to the fundamental frequency and its harmonics, and high frequency current i_{HF} linked to the switching frequency current and its harmonics.

9.3.1 Low frequency current

The relationship between the instantaneous DC-bus and the load power is given in (174).

$$V_{BUS} i_{BUS}(t) = P_{out} = v_u(\mathrm{t}) i_u(\mathrm{t}) + v_v(\mathrm{t}) i_v(\mathrm{t}) + v_w(\mathrm{t}) i_w(\mathrm{t}) \quad (174)$$

Substituting the (173) into (174), the instantaneous output power delivered to an asymmetrical load is given in (175).

$$V_{BUS} i_{BUS}(t) = P_{out}(t) = v_u(t) i_u(t) = V_{OUT} I_{OUT} \left[\cos\varphi_{OUT} - \cos\left(2\omega_{OUT} t\right)\right] \quad (175)$$

It can be seen from (175) that the instantaneous output power is the well known to be a DC component plus a second harmonic component. Accordingly, from the equation (175), the DC-bus instantaneous current can be obtained as in (176), where I_{OUT} is the RMS output current, ω_{OUT} is the output frequency and φ_{OUT} is the phase displacement between the output voltage and the corresponding output current at the fundamental frequency.

$$i_{BUS}(t) = i_{BUS,LF}(t) = \frac{V_{OUT} I_{OUT}}{V_{BUS}} \left[\cos\varphi_{OUT} - \cos\left(2\omega_{OUT} t\right) \right] \tag{176}$$

From equation (176) it possible to identify two main components: average component and double fundamental frequency.

9.3.2 Switching frequency current

The expression compact of the instantaneous current depends on the switching function $s_k(t)$ and output current $I_{OUT,k}$ as shown in (177), where k is the index of the kth converter. In this case k=1,2.

$$i_{BUS}(t) = \sum_{k=1}^{N_C} s_k(t) i_{OUT,k}(t), \tag{177}$$

In general, the switching function defined in (106) and (110) can be expended in Fourier Series as in (178), where p is the index of the pth harmonic order and d is the duty cycles.

$$s_k(t) = d + \frac{2}{\pi} \sum_{p=1}^{\infty} \frac{1}{p} \sin\left(pd\pi\right) \cos\left[p2\pi f_{sw} t + \frac{2\pi}{N_C}\left(k-1\right) \right], \text{k=1, 2,} \tag{178}$$

The output current of the kth converter is defined in (179), where φ_{OUT} is the phase displacement between the output voltage and the corresponding output current at the fundamental frequency.

$$i_{OUT,k}(t) = \sqrt{2} I_{OUT} \sin\left(\omega_{OUT} t - \varphi_{OUT}\right) \tag{179}$$

Substituting the equation (178) and (179) into (177) and assuming the same inductor and switches of the converter cells, it possible to obtain the compact form of the DC-bus instantaneous current. However, the analytical determination of the high frequency DC-bus current is quite difficult; consequently, we will only give one of the most significant expressions. Fig. 128 shows the harmonic content of the DC-bus instantaneous current $i_{BUS}(t)$. In this condition, the high frequency DC-bus current can be written as in (180).

$$i_{BUS,HF}(t) = \sqrt{2} \cdot 1.8 \cdot \sin\left(2\pi 48000 t\right) \tag{180}$$

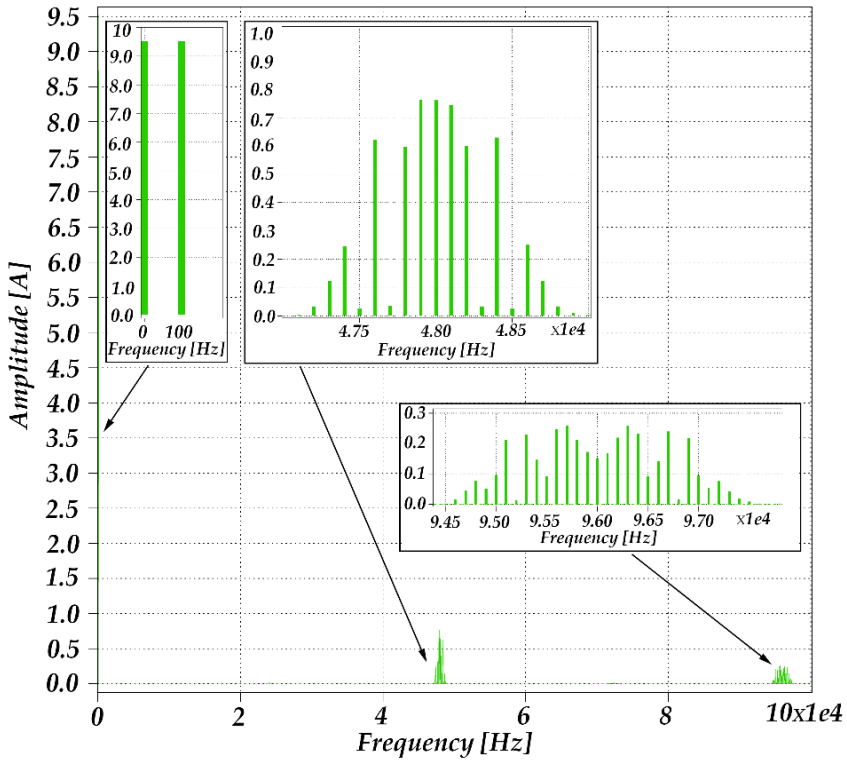


Fig. 128. Harmonic content of the DC-bus capacitors current $i_{BUS}(t)$, with M_0=0.93, f_{OUT}=50 Hz, f_{sw}=24 kHz, I_{OUT}=28.99 A, ξ=2, N_C=2..

9.3.3 DC-bus Capacitors Current

The low frequency current has strong impact on the capacitor losses, size, life time and cost. In order to optimize the system design (size and cost), low frequency current has to be reduced as much as possible. Let's assume that the SRBC compensates all the DC-bus current harmonics except 100 Hz component. From the equation (176), the low frequency DC-bus capacitors current $i_{CBUS,LF}(t)$ can be obtained in (181).

$$i_{CBUS,LF}(t) = \frac{V_{OUT} I_{OUT}}{V_{BUS}} \cos(2\omega_{OUT} t) \tag{181}$$

The RMS value of the double fundamental frequency is written in (182).

$$I_{CBUS,(RMS)}\Big|_{100Hz} = \frac{V_{OUT} I_{OUT}}{\sqrt{2} V_{BUS}} \tag{182}$$

Considering the V_{OUT}=230V, $\cos\varphi_{OUT}$ =1 and V_{BUS}=700V, the DC-bus capacitors RMS current versus output power is listed in Table 25.

Table 25. DC-bus capacitors RMS current versus output power.		
P_{out} [kW]	RMS output current I_{OUT} [A]	$I_{CBUS,(RMS)}\big\|_{100\,Hz}$ [A]
6.67	28,99	6,73
5	21,74	5,05
3.34	14,49	3,37
1.67	7,25	1,68
1	4,35	1,01

9.3.4 The capacitor RMS current scaled to the base frequency

The capacitor composite RMS current is computed as in (183), where I_n is n^{th} harmonic RMS current and k_n is a coefficient given by the capacitor manufacturer.

$$I_{CS,BUS(RMS)} = \sqrt{\sum_{n=1}^{\infty}\left(\frac{I_n}{k_n}\right)^2} \tag{183}$$

In this case, considering the coefficient $k_{100Hz}=1$, the capacitor equivalent RMS current is given in (184).

$$I_{CS,BUS(RMS)} = \sqrt{\left(\frac{I_{CBUS,(RMS)}\big|_{100\,Hz}}{k_{100\,Hz}}\right)^2} = I_{CBUS,(RMS)}\big|_{100\,Hz} \tag{184}$$

9.3.5 Capacitor current requirements

The DC-bus capacitors can be composed by N_P parallel capacitors and four series connected capacitors (N_S=4). Consequently, from the equation (184), we can obtain the requirement current per single capacitor

$$I_{C1,BUS(RMS)} = \frac{I_{CBUS,(RMS)}}{N_p} \tag{185}$$

Table 26. Requirement current per single capacitor versus output power.	
P_{out} [kW]	Requirement current per a capacitor $I_{C1,BUS(RMS)}$ [A]
6.67	1,12
5	0,84
3.34	0,56
1.67	0,28
1	0,17

Table 26 shows the requirement current per single capacitor versus output power.

9.4 DC-bus Capacitors selection

Low frequency voltage ripple is caused by the low frequency capacitor current. The dominant low frequency current is 2nd harmonic which flows to the DC-bus capacitors. Peak to peak voltage ripple can be approximated as in (186), where C_{BUS} is the partial DC-bus capacitor (C_{BUS}=C_{B1}=C_{B2}=C_{B3}=C_{B4}).

$$\Delta V_{BUS} = \frac{2\sqrt{2}}{(2\pi 100)C_{BUS}} N_P N_S I_{C1,BUS(RMS)} \quad (186)$$

From equation (186), we can compute the required minimum partial DC-bus capacitor, as shown in (187).

$$C_{BUS} = \frac{2\sqrt{2}}{(2\pi 100)\Delta V_{BUS}} N_P N_S I_{C1,BUS(RMS)} \quad (187)$$

Considering peak to peak voltage ripple ΔV_{BUS} equal to 100 V, the minimum partial DC-bus capacitor value C_{BUS} versus output power is listed in Table 27.

Table 27. Minimum total capacitance value C_{BUS} versus output power.

P_{out} [kW]	Requirement current per single capacitor $I_{C1,BUS(RMS)}$ [A]	Minimum partial DC-bus capacitor C_{BUS} [µF]
6.67	1,12	1212,61
5	0,84	909,46
3.34	0,56	606,30
1.67	0,28	303,15
1	0,17	181,89

According to this analysis, the manufacturer, part number and parameters of the selected capacitor are listed in Table 28.

Table 28. Main parameters of the selected capacitor.

Manufacturer	United Chemi-Con
Part number	EKXJ221ELL221MUP1S
Working Voltage	220 V
Cap Value	220 µF
Case size	14.5×35.5 mm
Dissipation Factor, tanδ (at 120 Hz)	0.2
Rated ripple current	1.095 A

9.5 The DC-bus capacitor losses and temperature

The DC-bus capacitor losses can also be computed as in (188), where $R_{ESR(100Hz)}$ is the capacitor ESR at the base frequency of 100Hz and $I_{C1,BUS(RMS)}$ is the capacitor composite current.

$$P_{BUS} = R_{ESR(100Hz)} \cdot I^2_{C1,BUS(RMS)} \tag{188}$$

The total loss of the DC-bus capacitors is reported in (189). The capacitor ESR, R_{ESR}, at 100 Hz is given in (190), where X_c is the reactance of the capacitor in ohms.

$$P_{BUS(TOTAL)} = N_P N_S R_{ESR(100Hz)} \cdot I^2_{C1,BUS(RMS)} \tag{189}$$

$$R_{ESR} = \tan\delta \cdot X_c \tag{190}$$

In Table 29 are listed the total losses of DC-bus capacitors versus output power.

Table 29. Total losses DC-bus capacitors versus P_{out} with tanδ=0.22 (at 100Hz and 20°C).

P_{out} [kW]	Requirement current per single capacitor $I_{C1,BUS(RMS)}$ [A]	Caps total losses [W]
6.67	1,12	40,10
5	0,84	22,56
3.34	0,56	10,02
1.67	0,28	2,51
1	0,17	0,90

The temperature is important for the working life of the DC-bus. The case temperature, T_c, is given from equation (191), where T_a is the ambient temperature, and $R_{th,c\text{-}a}$ is the case to ambient thermal resistance.

$$T_c = T_a + R_{th,c-a}\left(R_{ESR(100Hz)} \cdot I^2_{C1,BUS(RMS)}\right) \tag{191}$$

The case to ambient thermal resistance, $R_{th,c\text{-}a}$, can be obtained from equation (192), where A is the capacitor active surface [m²] and v is the cooling air velocity [m/s].

$$R_{th,c-a} = \frac{1}{A\left(5 + 17\left(v + 0.1\right)^{0.66}\right)} \tag{192}$$

From datasheet, we can obtain the capacitor active surface as

$$A = A_L + A_B = 2\pi l\left(\frac{d}{2}\right) + \pi\left(\frac{d}{2}\right)^2 = 2\pi \cdot 35.5 \cdot \left(\frac{14.5}{2}\right) + \pi\left(\frac{14.5}{2}\right)^2 = 1781.36\ [\text{mm}^2]$$

If we set the case temperature, we can obtain the thermal resistance $R_{th,c\text{-}a}$ and the cooling air velocity of the cooling system.

9.6 Capacitors Life-time

Electrolytic capacitors are characterized by operating life time that strongly depends on the operating RMS current, applied voltage and operating temperature [167]. The life time is defined as in (193), where λ_{T0} is the life time at manufacturer given conditions, T_0 is the maximum rated temperature, T_a is the capacitor ambient temperature, ΔT_0 is the capacitor core temperature rise, A is a coefficient that takes into account the load current effect, U_C is the capacitor operating voltage and U_{CN} is the capacitor rated voltage.

$$\lambda_T = \lambda_{T0} 2^{\frac{T_0 - T_a}{10K}} A^{\left(1-K_L^2\right)\frac{\Delta T_0}{10K}} \left(\frac{U_C}{U_{CN}}\right)^{-n} \tag{193}$$

From equivalent current (194) and the selected capacitor nominal current we compute the capacitor load factor as in (194).

$$K_L = \frac{I_{C1,BUS(RMS)}}{I_{CN(RMS)}} \tag{194}$$

where $I_{CN(RMS)}$ is the capacitor nominal current at given conditions. The capacitor life-time characteristic is usually given as plot of the loading coefficient versus the capacitor temperature and life time expectancy. As can be seen from the datasheet of the KXJ Series capacitor, the rated endurance of the capacitors results in 12000 hours at the temperature of 105°C.

PART FOUR

CONCEPT DESIGN OF THE PROPOSED TOPOLOGY

10 PERFORMANCE ASSESSMENT OF THE CONVERTER

The N5L E-Type BTB Converter has been designed on the basis of analytical relationships. Analytical equations expressing the power losses associated to the switching devices in the N5L E-Type BTB Converter are very advantageous in the design procedure. In this section, we will present the performance of the three-phase N5L E-Type BTB Converter (3ΦN5L E-Type BTB Converter) using two-cell interleaved

10.1 N5L E-Type BTB Converter Devices Selection

The devices conduction and switching losses for the 3ΦN5L E-Type BTB Converter using two-cell interleaved are evaluated considering a mixed combination of both IGBT and MOSFET, as depicted in Fig. 129. Part number, voltage rating, current rating, technology and manufacturers of the 3ΦN5L E-Type BTB Converter devices are listed in Table 30.

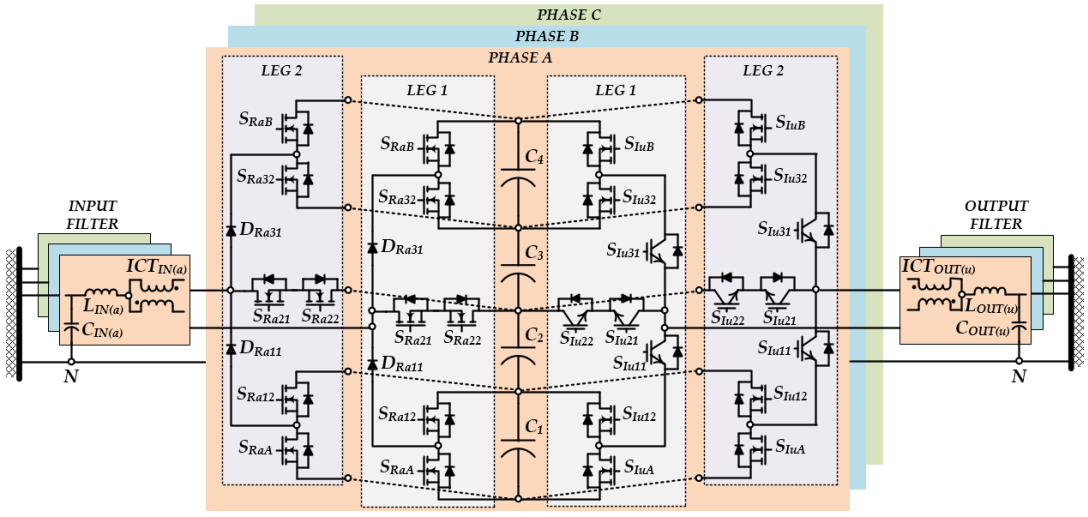


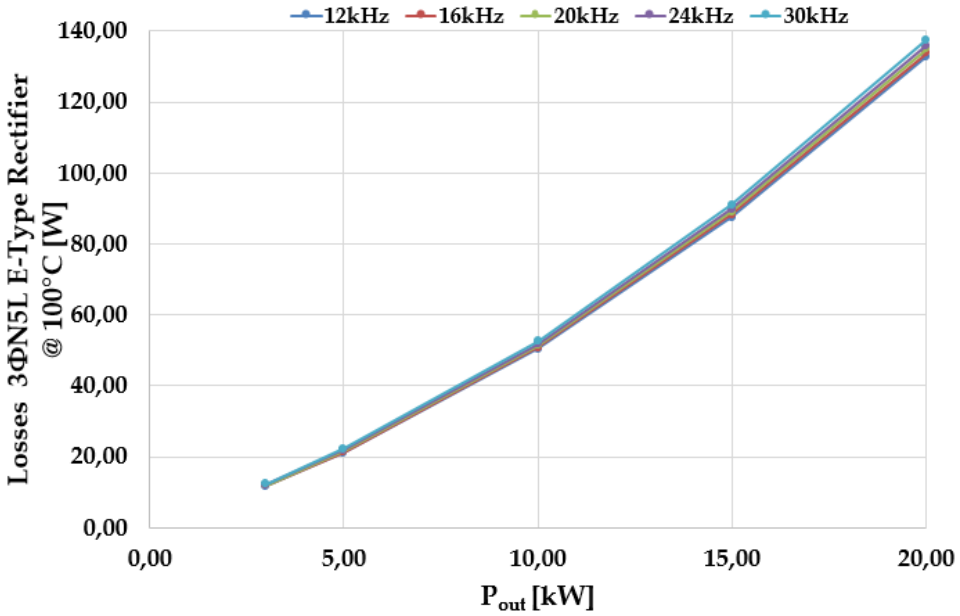
Fig. 129. 3ΦN5L E-Type BTB Converter using two-cell interleaved.

Using the previously achieved analytical equations for the calculation of RMS and average currents and the datasheet provided by manufacturers, the conduction and switching losses in each device have been obtained.

Table 30. 3ΦN5L E-Type BTB Converter configuration						
3ΦN5L E-Type Rectifier						
Device	**Part Number**	**Rated Voltage [V]**	**Rated Current [A]**	**$R_{DS(on),max}$ [mΩ]**	**Technology**	**Manufacturers**
S_{RPA}, S_{RPB}, S_{RP12}, S_{RP32}	IPT210N25NFD	250 V	69 A	21	OptiMOS™ 3	Infineon
D_{RP31}, D_{RP11}	STPSC40065C	650 V	40 A	-	Schottky SiC Diode	STMicroelectronics
S_{RP21}, S_{RP22}	IPL60R104C7	650 V	20 A	104	CoolMOS™C7	Infineon
3ΦN5L E-Type Inverter						
S_{IQA}, S_{IQB}, S_{IQ12}, S_{IQ32}	IPT210N25NFD	250 V	69 A	21	OptiMOS™ 3	Infineon
S_{IQ31}, S_{IQ11}	IKW75N65EL5	650 V	75 A	-	Si-IGBT	Infineon
S_{IQ21}, S_{IQ22}	IKW20N60T	600 V	20 A	-	Si-IGBT	Infineon

10.2 Semiconductor Devices Losses

The operating point of the converter are: V_{in}=230V, V_{out}=230V, $\cos\varphi_{OUT}$=1, V_{BUS}=700V, T_j=100°C. Additionally, neglecting the voltage drop of the power devices the modulation depth of the 5L E-Type Rectifier $M_{0,R}$ is approximately equal to the modulation depth of the 5L E-Type Inverter $M_{0,I}$, namely $M_{0,R}$=$M_{0,I}$=M_0=0.93. The losses related to the power devices (filters, DC-bus and additional losses are excluded) of the 3ΦN5L E-Type Rectifier and 3ΦN5L E-Type Rectifier versus output power for different value of switching frequency, 12 kHz,16 kHz, 20 kHz, 24 kHz and 30 kHz are depicted in Fig. 130.



(a)

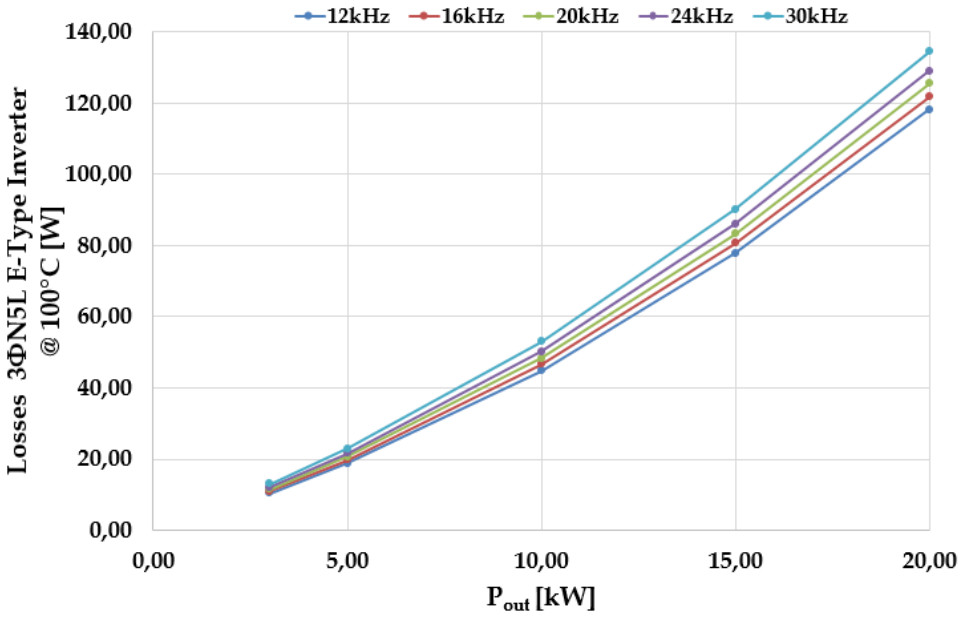


Fig. 130. a) Losses versus output power related to the power devices at 12 kHz,16 kHz, 20 kHz, 24kHz and 30 kHz. a) 3ΦN5L E-Type Rectifier, b) 3ΦN5L E-Type Inverter.

Losses number values of the N5L E-Type Rectifier and inverter are reported in Table 31.

Table 31. Power devices losses number values.						
P_{out} [kW]	Phase-leg Output Current [RMS]	Losses [W]				
		f_{sw}=12 kHz	f_{sw} =16 kHz	f_{sw} =20 kHz	fsw =24 kHz	f_{sw} =30kHz
3ΦN5L E-Type Rectifier						
20	14,49	132,88	133,90	134,93	135,95	137,49
15	10,87	87,57	88,34	89,11	89,88	91,04
10	7,25	50,33	50,84	51,35	51,87	52,64
5	3.62	21,14	21,39	21,65	21,91	22,29
3	2,17	11,72	11,87	12,02	12,18	12,41
3ΦN5L E-Type Inverter						
20	14,49	118,13	121,75	125,37	128,99	134,41
15	10,87	77,84	80,56	83,28	86,00	90,08
10	7,25	44,73	46,55	48,38	50,20	52,93
5	3.62	18,80	19,72	20,64	21,57	22,95
3	2,17	10,44	11,00	11,56	12,11	12,95

Fig. 131 and Fig. 132 shows the power devices efficiency of the 3ΦN5L E-Type Rectifier and 3ΦN5L E-Type Inverter versus output power at 12 kHz, 16 kHz, 20 kHz, 24kHz and 30 kHz respectively.

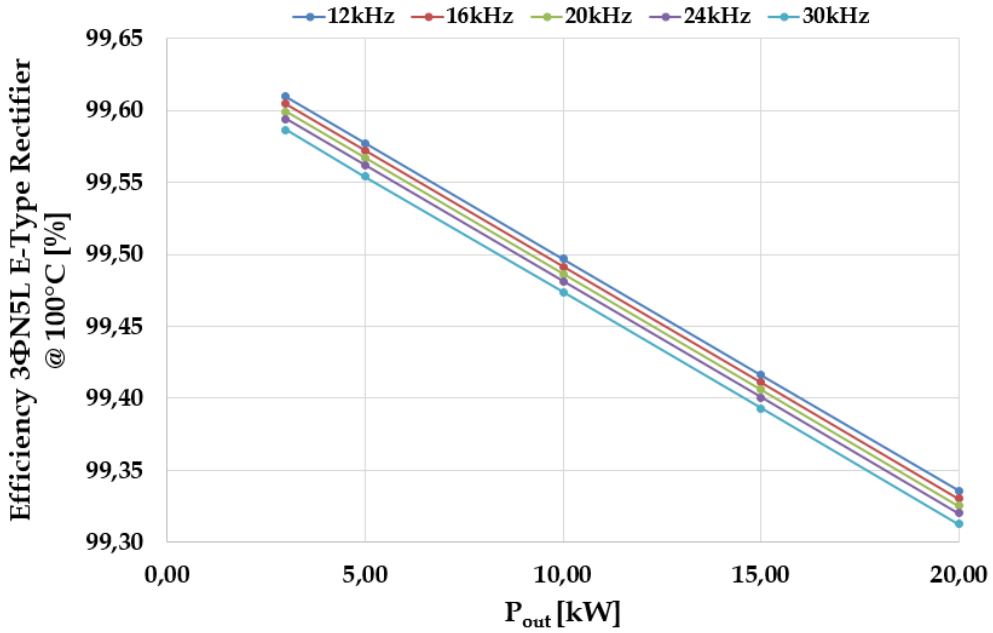


Fig. 131. Power devices efficiency 3ΦN5L E-Type Rectifier versus output power at 12 kHz,16 kHz, 20 kHz, 24kHz and 30 kHz.

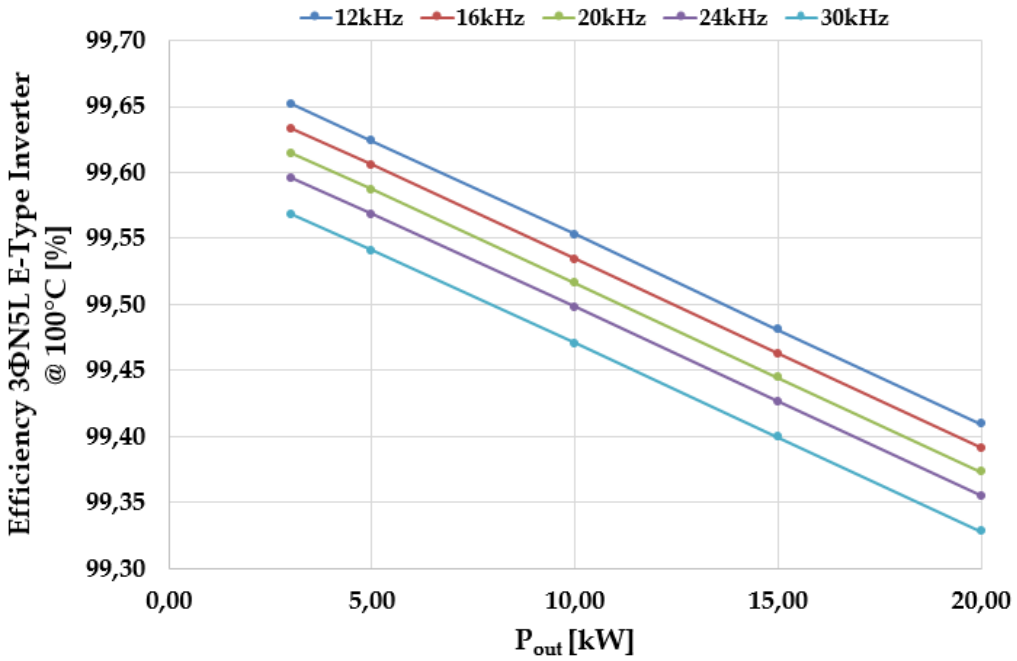


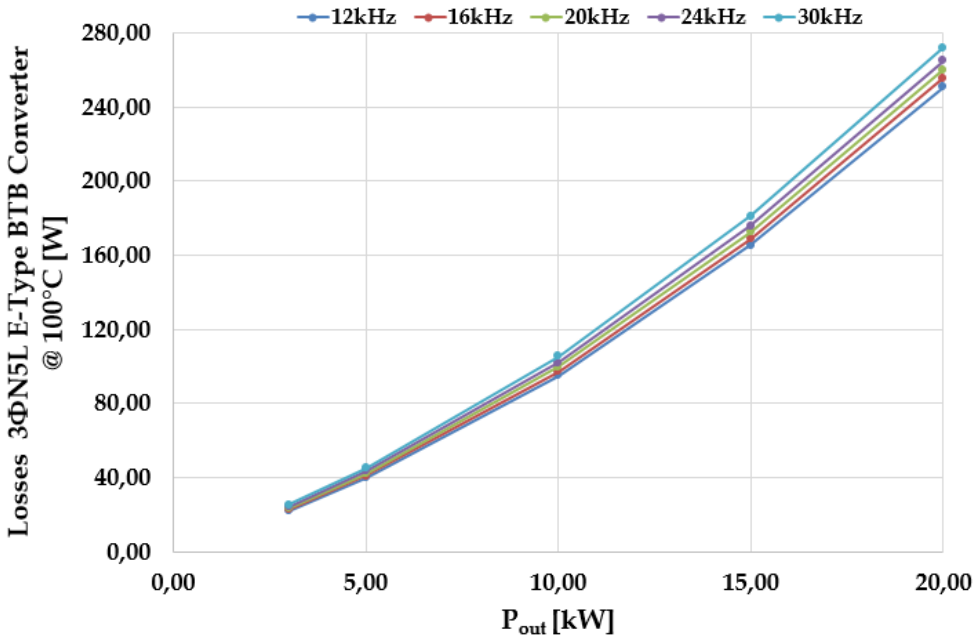
Fig. 132. Power devices efficiency 3ΦN5L E-Type Inverter versus output power at 12 kHz,16 kHz, 20 kHz, 24kHz and 30 kHz.

Table 36 shows the efficiency values of the rectifier and inverter.

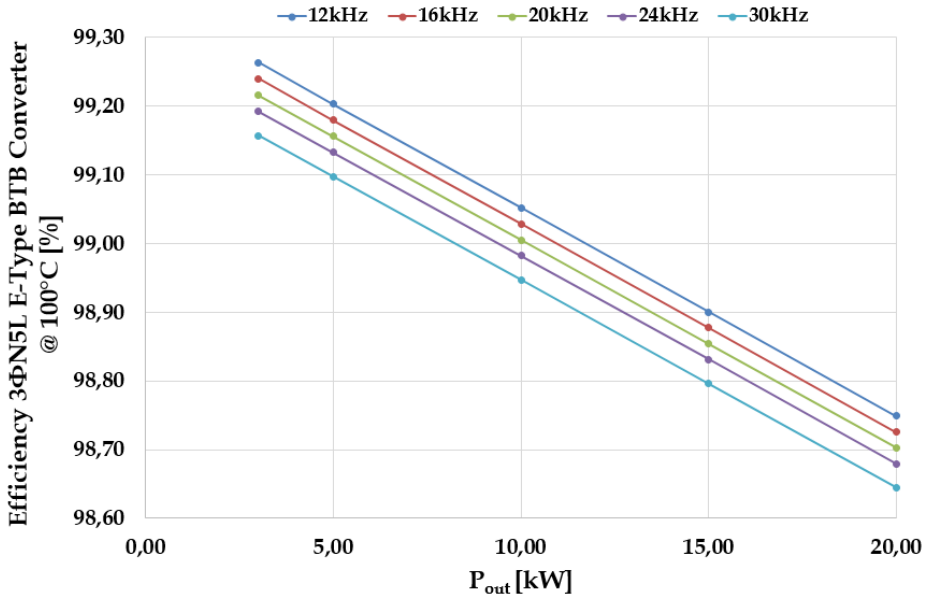
Table 32. Power devices efficiency number values (without filters, DC-bus and additional losses).

P_{out} [kW]	Phase-leg Output Current [RMS]	Efficiency [%]				
		f_{sw}=12 kHz	f_{sw} =16 kHz	f_{sw} =20 kHz	fsw =24 kHz	f_{sw} =30kHz
3ΦN5L E-Type Rectifier						
20	14,49	99,34	99,33	99,33	99,32	99,31
15	10,87	99,42	99,41	99,41	99,40	99,39
10	7,25	99,50	99,49	99,49	99,48	99,47
5	3.62	99,58	99,57	99,57	99,56	99,55
3	2,17	99,61	99,60	99,60	99,59	99,59
3ΦN5L E-Type Inverter						
20	14,49	99,41	99,39	99,37	99,36	99,33
15	10,87	99,48	99,46	99,44	99,43	99,40
10	7,25	99,55	99,53	99,52	99,50	99,47
5	3.62	99,62	99,61	99,59	99,57	99,54
3	2,17	99,65	99,63	99,61	99,60	99,57

Fig. 133 depicts the losses and power devices efficiency (excluding filters, DC-bus and additional losses) of the 3ΦN5L E-Type BTB Converter versus output power at 12 kHz,16 kHz, 20 kHz, 24kHz and 30 kHz, respectively. Numeric values of losses and efficiency are listed in Table 36.



(a)



(b)

Fig. 133. a) Power devices losses and efficiency versus output power at 12 kHz,16 kHz, 20 kHz, 24kHz and 30 kHz of the 3ΦN5L E-Type BTB Converter. a) Losses, b) Efficiency.

Table 33. Power devices losses and efficiency number values of the 3ΦN5L E-Type BTB Converter, (without filters, DC-bus and additional losses)						
P_{out} [kW]	Phase-leg Output Current [RMS]	Losses [W]				
		f_{sw}=12 kHz	f_{sw} =16 kHz	f_{sw} =20 kHz	fsw =24 kHz	f_{sw} =30kHz
20	14,49	251,01	255,65	260,29	264,94	271,90
15	10,87	165,41	168,90	172,39	175,88	181,12
10	7,25	95,06	97,39	99,73	102,07	105,57
5	3.62	39,94	41,11	42,29	43,47	45,24
3	2,17	22,15	22,86	23,58	24,29	25,36
		Efficiency [%]				
20	14,49	98,75	98,73	98,70	98,68	98,65
15	10,87	98,90	98,88	98,85	98,83	98,80
10	7,25	99,05	99,03	99,01	98,98	98,95
5	3.62	99,20	99,18	99,16	99,13	99,10
3	2,17	99,26	99,24	99,22	99,19	99,16

Finally, Fig. 134 and Fig. 135 shows the losses and efficiency versus switching frequency of the 3ΦN5L E-Type BTB Converter at 3 kW, 5 kW, 10 kW, 15 kW and 20 kW, respectively.

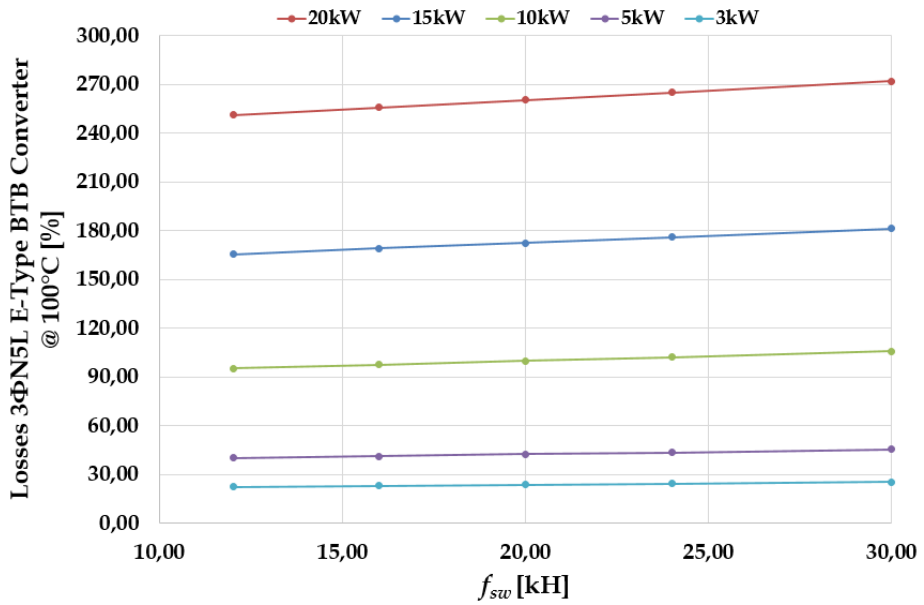


Fig. 134. Losses versus switching frequency at 3 kW, 5 kW, 10 kW, 15 kW, 20 kW of the 3ΦN5L E-Type BTB Converter.

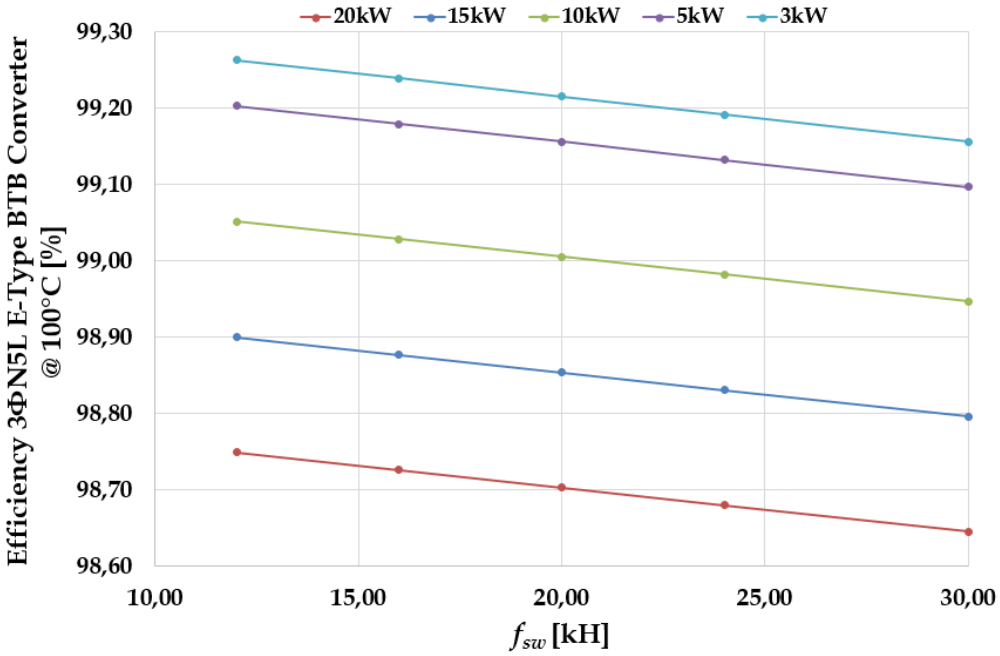


Fig. 135. a) Efficiency versus switching frequency at 3 kW, 5 kW, 10 kW, 15 kW, 20 kW of the 3ΦN5L E-Type BTB Converter.

10.2.1 Remarks on the Efficiency Results

Let's analyze the trend of the rectifier and inverter efficiency curves. The analytical efficiency is given in (195). The efficiency trend versus output power of the 3ΦN5L E-Type Rectifier depicted in Fig. 131 is almost linear. Why this linear trend? 3ΦN5L E-Type BTB Rectifier is only formed by power MOSFETs. MOSFETs conduction losses are due to the ohmic resistance (r_{sw}) behavior of the devices; therefore, the term $V_{sw(0)}I_{AVG}$ is zero in the equation (195), where EAVG are the average of the switching losses.

$$\eta = \frac{1}{1+\frac{P_{switch}}{P_{out}}} = \frac{1}{1+\frac{\overbrace{V_{sw0}I_{AVG}+r_{sw}I_{RMS}^2}^{Cunduction\ Losses}+\overbrace{f_{sw}E_{AVG}}^{Switching\ Losses}+\overbrace{f_{sw}E_{rr,AVG}}^{Recovery\ Losses}}{P_{out}}} \tag{195}$$

When the output power is increasing the switching and recovery losses are minority over the value of the conduction losses. As can be seen from Table 34, the switching and recovery losses of the 3ΦN5L E-Type Rectifier are less than 10% compared to the conduction losses when the output power is higher than 3 kW.

Table 34. Conduction, switching and recovery losses of the 3ΦN5L E-Type BTB Rectifier at 24 kHz.			
P_{out} [kW]	Conduction losses [W]	Switching and recovery losses [W]	Percentage Report
20	129,80	6,16	6,16 is 4.75% of 129,80
15	85,27	4,62	4,62 is 5.42% of 85,27
10	48,79	3,08	3,08 is 6.31% of 48,79
5	20,37	1,54	1,54 is 7.56% of 20,37
3	11,25	0,92	0,92 is 8.18% of 11,25

Thus, the efficiency can be written approximately as in (196), there exists a linear relationship between the efficiency of the Rectifier and the output power. When the output power increases, keeping constant the output voltage, the output current is increased and the efficiency is reduced.

$$\eta \cong \frac{1}{1+\frac{r_{sw} I_{RMS}^2}{P_{out}}} \cong \frac{1}{1+\frac{r_{sw}}{V_{OUT(rms)}} I_{RMS}} \tag{196}$$

The 3ΦN5L E-Type Inverter is composed by IGBTs and MOSFETs. It can be notated that the efficiency curves of the inverter show a full linear trend with output power as the rectifier, as depicted in Fig. 132. The reason is the same as a previously case.

Table 35. Conduction, switching and recovery losses of the 3ΦN5L E-Type BTB Inverter at 24 kHz.			
P_{out} [kW]	Conduction losses [W]	Switching and recovery losses [W]	Percentage Report
20	107,28	21,71	21,71 is 20.24% of 107,28
15	69,67	16,33	16,33 is 23.44% of 69,67
10	39,26	10,94	10,94 is 24.44% of 39,26
5	16,03	5,53	5,53 is 27.87% of 16,03
3	8,76	3,36	3,36 is 38.36% of 8,76

The switching and recovery losses are not negligible compared to the conduction losses. As can be seen from Table 35, when the output power is 3 kW the switching and recovery losses are 38.36% of conduction losses, whereas at 20 kW the switching and recovery losses are 20.24% of conduction losses. Consequently,

it does exist a full linear relationship between the efficiency of the Inverter and the output power.

10.3 Thermal Stress

After losses have been calculated, temperatures during stationary operation can be calculated with the aid of the thermal resistances R_{th}. Temperature calculation is performed starting with the ambient temperature from the outside to the inside, as shown in Fig. 136.

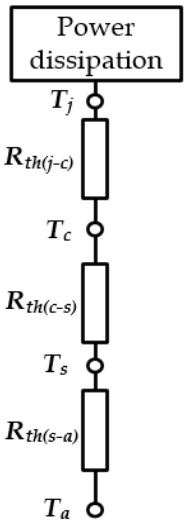


Fig. 136. Temperature calculation under stationary conditions.

The ambient air temperature T_a for cooling electronic equipment depends on the operating environment in which the component is expected to be used. Typically, it ranges from 35 to 45°C, if the external air is used, and from 50 to 60°C, if the component is enclosed or is placed in a wake of another heat generating equipment. In this project, T_a has been chosen equal to 40°C. If we set the heatsink temperature approximately equal to 95°C, we can obtain the heat sink thermal resistance $R_{th(s-a)}$, as given in equation (197), where P_T is the total power losses or rate of heat dissipation in watt. The total power, P_T, represents the rate of heat dissipated by the electronic component during operation. The sink temperature represents the maximum temperature of the heat sink at the location closest to the device.

$$R_{th(s-a)} = \frac{T_{s-a}}{P_T} = \frac{T_s - T_a}{P_T} \tag{197}$$

From equation (198) has been obtained the case temperature, where the $R_{th(c-s)}$ represents the thermal resistance across the interface between the case and the heat sink and is often called the interface resistance.

$$T_c = R_{th(c-s)}\left[P_{T-trans} + P_{T-diode}\right] + T_s \tag{198}$$

This value can be improved substantially depending on the quality of mating surface finish and/or the choice of interface material. The interface resistance $R_{th(c-s)}$ is controlled in a variety of manners with different heat conducting materials. The interface resistance is dependent on four variables: the thermal resistivity ρ of the interface material (m·°C/W), the average material thickness t (m), the area of the thermal contact footprint A (m^2), and the ability to replace voids due to finish or flatness (sink or chip) with a better thermal conductor than air. The interface thermal resistance is then expressed as $R_{th(c-s)} = \rho \cdot t/A$. Precise value of this resistance, even for a given type of material and thickness, is difficult to obtain, since it may vary widely with the mounting pressure and other case dependent parameters. However, some useful data can be obtained directly from material manufacturers or from heat sink manufacturers. Considering Mica/grease as an interface material with a thickness equal to 0.003 inch, the thermal resistance value is equal to 0.1 °C/W.

Modules with base plate show good thermal coupling between their components and the thermal resistance $R_{th(c-s)}$ is specified for the entire module, which is why all sources of power loss in the module are added up to calculate the case temperature. The junction temperature is finally calculated from the losses of the single component by equation (199), where $R_{th(j-c)}$ is the thermal resistance between the junction and the case of the device.

$$T_j = P_T R_{th(j-c)} + T_c \tag{199}$$

The resistance $R_{th(j-c)}$ is specified by the device manufacturer. Although the $R_{th(j-c)}$ value of a given device depends on how and where the cooling mechanism is

employed over the package, it is usually given as a constant value. According to this analysis and considering an output power of about 20 kW, the Table 36 has been obtained.

Table 36. Steady-state thermal model 3ΦN5L E-Type Rectifier and 3ΦN5L E-Type Inverter.

T_a [°C]	40
T_s [°C]	95
3ΦN5L E-Type Rectifier	
$R_{ths(a-s)}$ [°C/W]	1.21
$T_{c(outer-leg)}$ [°C]	95.30
$T_{j(SRPA)}$, $T_{j(SRPB)}$ [°C]	95.70
$T_{j(DRPA)}$, $T_{j(DRPB)}$ [°C]	95.30
$T_{c(top\ middle-leg)}$ [°C]	95.80
$T_{j(DRP31)}$, $T_{j(DRP11)}$ [°C]	99.80
$T_{j(SRP32)}$, $T_{j(SRP12)}$ [°C]	96.10
$T_{c(middle-leg)}$ [°C]	95.00
$T_{j(SRP21)}$ [°C]	95.40
$T_{j(DRP22)}$ [°C]	95.24
3ΦN5L E-Type Inverter	
$R_{ths(a-s)}$ [°C/W]	1.28
$T_{c(outer-leg)}$ [°C]	95.25
$T_{j(SIQA)}$, $T_{j(SIQB)}$ [°C]	95.46
$T_{j(DIQA)}$, $T_{j(DIQB)}$ [°C]	95.29
$T_{c(top\ middle-leg)}$ [°C]	95.71
$T_{j(SIQ32)}$, $T_{j(SIQ12)}$ [°C]	96.14
$T_{j(DIQ32)}$), $T_{j(DIQ12)}$ [°C]	95.71
$T_{j(SIQ31)}$, $T_{j(SIQ11)}$ [°C]	96.77
$T_{j(DIQ31)}$, $T_{j(DIQ11)}$ [°C]	95.71
$T_{c(middle-leg)}$ [°C]	95.12
$T_{j(SIQ22)}$ [°C]	95.92
$T_{j(DIQ21)}$ [°C]	95.44

10.4 Losses and Efficiency Converter Power Stage

In this section, we will present the estimated losses connected to input and output filters, gate driver, fan and control board. Finally, the total losses and efficiency of the overall converter power stage have been obtained. System operating point is reported below:

- V_{IN}=230V,

- V_{OUT}=230V,
- $\cos\varphi_{OUT}$=1,
- V_{BUS}=700V,
- f_{sw}=24kHz,
- T_j=100°C,
- Symmetrical load condition.

As the load is symmetrical load, the currents in the DC-bus capacitors are zero. Accordingly, the capacitor losses are zero.

10.4.1 Input and Output Filter Losses

The losses related to the three-phase input and output filters are shown in Fig. 137. The losses value is listed in Table 37. These results have been carried out considering the input and output capacitance losses, $C_{IN(P)}$ and $C_{IN(Q)}$ with $P \in \{a, b, c\}$ and $Q \in \{u, v, w\}$, negligible.

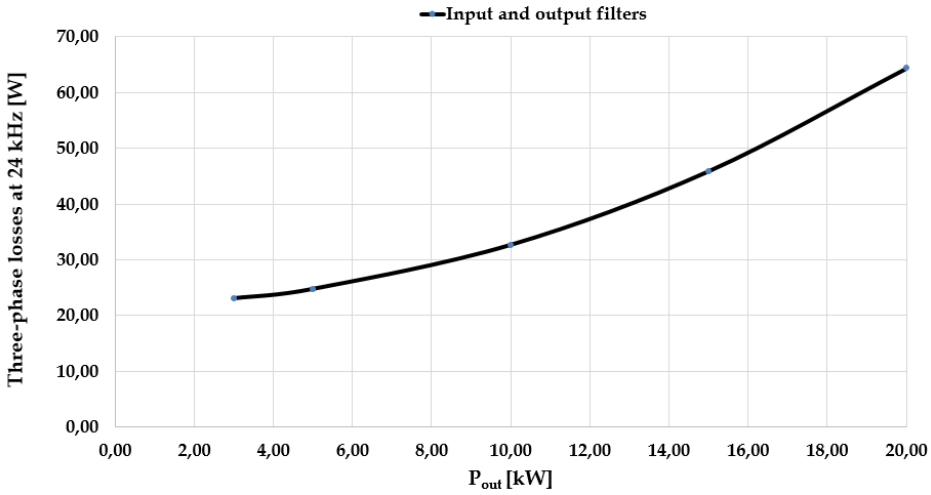


Fig. 137. Three-phase input and output filters losses at 24 kHz.

Table 37. Three-phase input and output filters losses value versus output power at 24 kHz.	
P_{out} [kW]	Losses [W]
20	64,33
15	45,85
10	32,66
5	24,74
3	23,05

10.4.2 Aux, Fan and Control Board Losses

In Table 38 are listed the fan estimation losses versus output power.

Table 38. Fan estimation losses value versus output power.	
P_{out} [kW]	Fan Losses [W]
20	40
15	30
10	20
5	10
3	6

Total aux losses have been estimated according to preliminary analysis and design. Table 39 shows the total aux losses computed under nominal load condition.

Table 39. Total Aux losses									
Switch	Device	Q_G [nC]	$V_{CC}+V_{EE}$ [V]	f_{sw} [kHz]	f_{swE} [kHz]	h_{PS}	P_{GD} [mW]	GD IC, P_{IC}	Total per GD $P_{GD,t}$ [W]
Rectifier Gate Driver									
S_{RPA}, S_{RPB}, S_{RP12}, S_{RP32}	IPT210N25NFD	65	15	24	7.2	0.7	10.03	35	45.03
S_{RP21}, S_{RP22}	IPL60R104C7	42	15	24	7.2	0.7	6.48	35	41.48
Inverter Gate Driver									
S_{IQA}, S_{IQB}, S_{IQ12}, S_{IQ32}	IPT210N25NFD	65	15	24	7.2	0.7	10.06	35	45.03
S_{IQ31}, S_{IQ11}	IKW75N65EL5	436	15	24	7.2	0.7	67.27	35	102.27
S_{IQ21}, S_{IQ22}	IKW20N60T	120	15	24	7.2	0.7	18.51	35	53.51
Total GD Consumption per cell and phase, $P_{GD,cell}$ [W]									0.75
Total GD Consumption per a 20kW converter, $P_{GD,tot}$ [W]									4.53
Control Board Losses [W]									
FPGA[W]									2.5
Signal Conditioning Circuit [W]									2
Rest of Circuit [W]									2.5
Total Aux Consumption per a 20kW Converter [W] (Aux. power supply 20W rated power, output voltage 15V, efficiency 90%)									12.81

The gate driver (GD) output power has been estimated as in (200), where h_{PS} is the efficiency of the power supply and f_{swE} is the equivalent switching frequency.

$$P_{GD} = \frac{Q_G \cdot f_{swE}}{h_{PS}} \cdot (V_{CC} + V_{EE}) \tag{200}$$

Total gate driver output power is defined as (201), where P_{IC} is the GD IC consumption. The preliminary design of the GD makes use of the IC 1EDI20N12AF-Infineon.

$$P_{GD,t} = P_{IC} + P_{GD,out} \tag{201}$$

Thus, the total GD consumption per cell and phase $P_{GD,cell}$ and total GD Consumption per a 20kW converter, $P_{GD,tot}$ have been obtained as in (202).

$$\begin{aligned} P_{GD,cell} &= \sum_i P_{GD,t(i)} \\ P_{GD,total} &= 6 \cdot P_{GD,cell} \end{aligned} \tag{202}$$

10.4.3 Total Losses and Efficiency

Losses and efficiency versus power load of the 3ΦN5L E-Type BTB Converter including the input and output filters, fan, control board and gate driver at 24 kHz have been obtained. The results are depicted in Fig. 138.

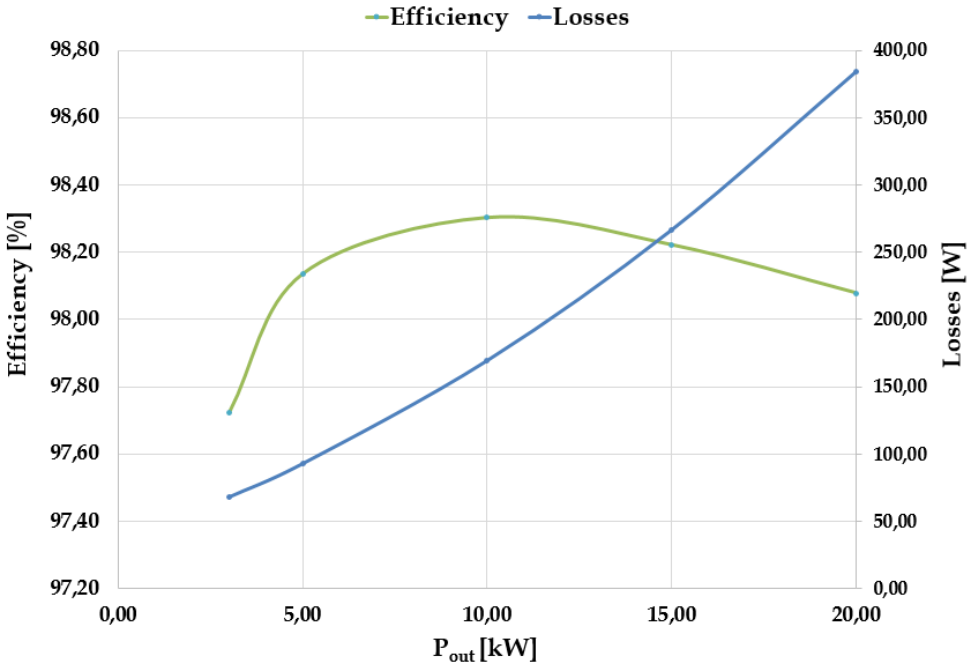


Fig. 138. Losses and Efficiency power stage versus output power at 24 kHz.

The green line is related to the efficiency, whereas the blue line is linked to the losses. Please notice the peak efficiency is 98.26%, while the full load efficiency is about 98.03%. Losses and efficiency number values of the power stage are reported in Table 40.

Table 40. Losses and Efficiency Power Stage versus output power value at 24 kHz.		
P_{out} [kW]	Losses [W]	Efficiency [%]
20	384,26	98,08
15	266,74	98,22
10	169,73	98,30
5	93,22	98,14
3	68,35	97,72

10.5 3D Model of the Converter Power Stage

3D Model of the overall Converter is depicted in Fig. 139

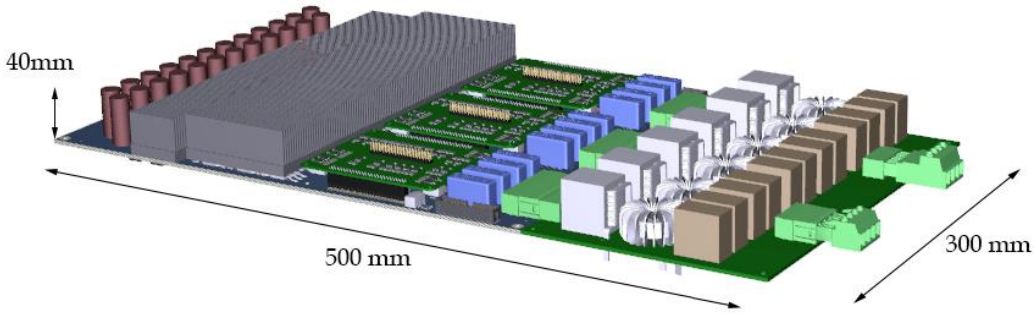


Fig. 139. 3D Model of the Converter Power Stage.

In this model, it possible to recognize the following components

- Three-phase 3ΦN5L E-Type BTB Converter
- Driver Circuit board
- Input and output filters board
- DC-bus capacitors
- Power Supply Unit
- Current and voltage Measure sensors
- Heat Sink

10.6 Volume and Weight Estimation

Other characteristics such as volume and weight for each part of the converter as well as specific power and power density of the converter can be relevant for the development of the new power conversion system. Fig. 140 shows the estimated volume and weight for each part of the 3ΦN5L E-Type BTB Converter as power semiconductors, DC-bus, input and output filter, heat sink, PCB and current sensors.

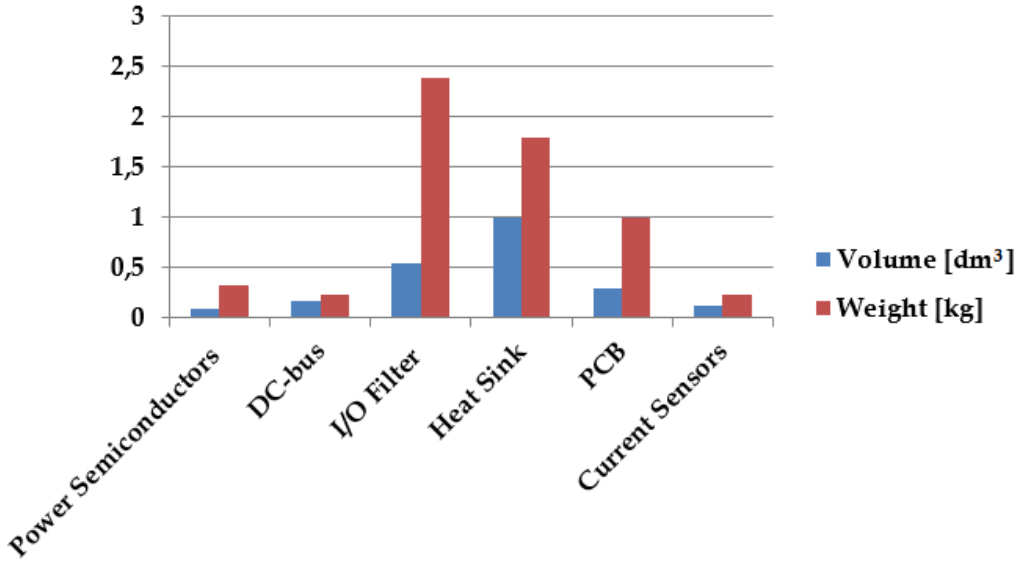


Fig. 140. Estimated volume and weight versus 3ΦN5L E-Type BTB Converter's part.

Volume and weight numeric values of the 3ΦN5L E-Type BTB Converter hardware sections are listed in Table 41.

Table 41. Volume and weight number values versus 3ΦN5L E-Type BTB Converter's part.

	Volume [dm³]	Weight [kg]
Power Semiconductors	0,098	0,32
DC-bus	0,17	0,24
I/O Filter	0,55	2,39
Heat Sink	0,99	1,8
PCB	0,3	1
Current Sensors	0,12	0,24

In order to provide a better measure of the technological advancement for 3ΦN5L E-Type BTB Converter, most important figures of merit such as total volume, power density, total weight and specific density have been obtained. The power

density, $\rho_{density}$, is defined as the nominal output power by the total volume *Vol*.

$$\rho_{density} = \frac{P_N}{Vol} \tag{203}$$

The total volume *Vol* is given by the sum of the single converter component, as in (204)

$$Vol = \sum_i Vol_i \tag{204}$$

Finally, the specific power density of the 3ΦN5L E-Type BTB Converter is evaluated as in (205), where G is total weight of converter.

$$\rho_{specific} = \frac{P_N}{G} \tag{205}$$

The estimated values for the figures of merit related to the overall 3ΦN5L E-Type BTB Converter are summarized in Table 42.

Table 42. Development trend of the 3ΦN5L E-Type BTB Converter.

Total Volume, *Vol*	dm^3	2,36
Power Density, $\rho_{density}$	kVA/dm^3	8,47
Total Weight, G	kg	6,18
Specific Power, $\rho_{specific}$	kVA/kg	3,24

10.7 Discussion on Power Losses and Efficiency

The achieved results in previously section show peak efficiency values for the overall system (98.30), go farther than the one indicated in the target of the project (98.25%). However, this is not the end of the design story and some solutions are under investigation to further improve the theoretical peak efficiency and full load efficiency as well.

The estimated efficiency strongly depends on the power semiconductor parameters obtained from datasheet (i.e. forward voltage drop $V_{sw(0)}$, ohmic resistance r_{sw} etc…). Additionally, the auxiliary losses take into account the controller, gate driver and measuring chain losses. As reported in Table 39, the estimated total auxiliary losses are about 12.81 W and a constant value of 15 W has been used in the efficiency calculation. However, this value could be significantly affected by several factors as ICs consumption and power supply

efficiency (currently estimated as 90%). As a result of the mentioned tolerances in the calculation process, experimental tests could lead to somehow different results, but in any case, very close to the envisaged targets. It is important to understand the losses distribution in each device, in order to conceive suitable strategies to be performed during the experimental activity, if needed. To this purpose, Fig. 141 shows the filters, auxiliary and fan losses versus the output power. Power semiconductors losses distribution versus output power is shown in Fig. 142a and Fig. 142b, respectively for conduction and switching losses.

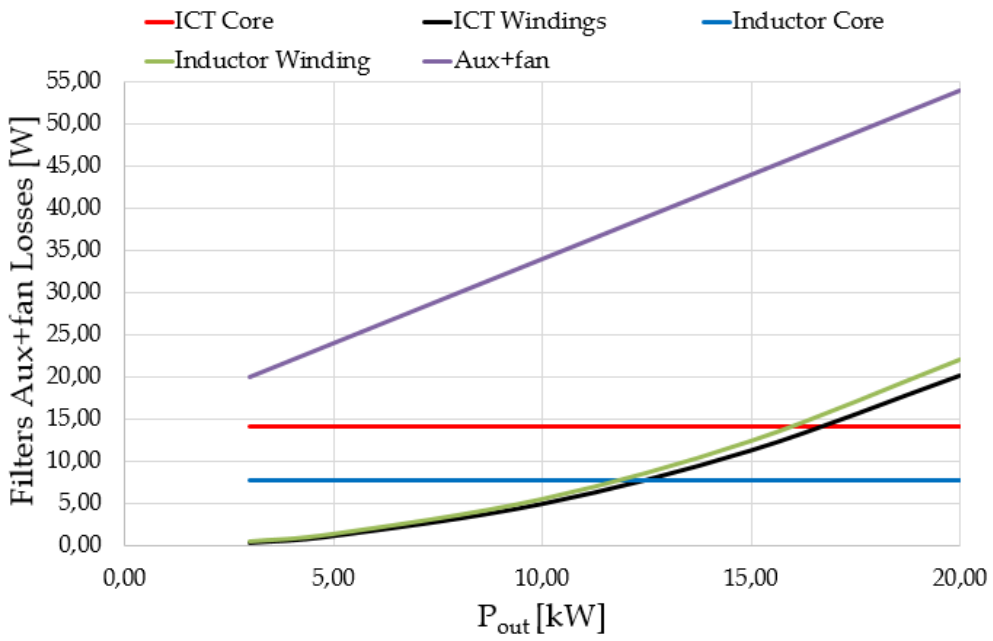
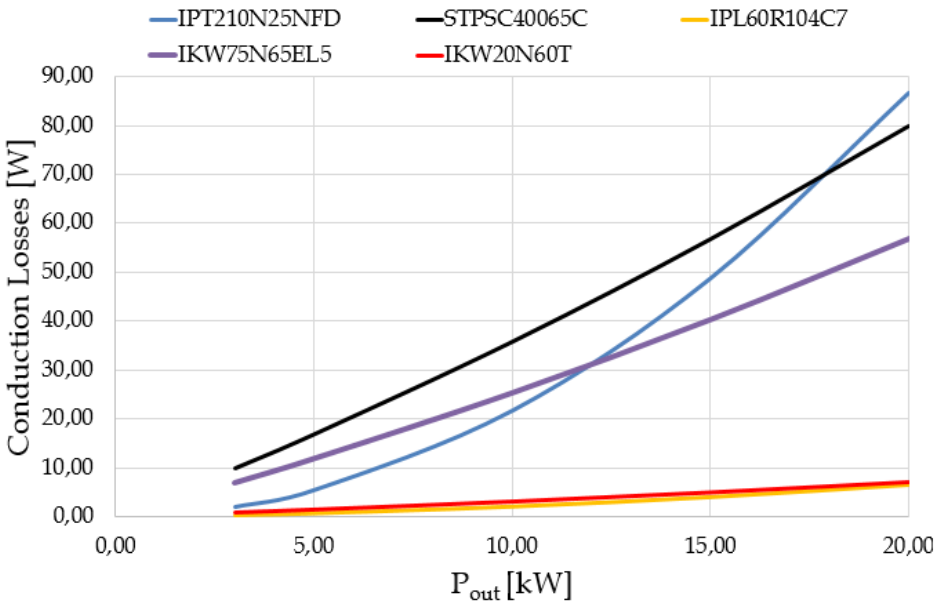
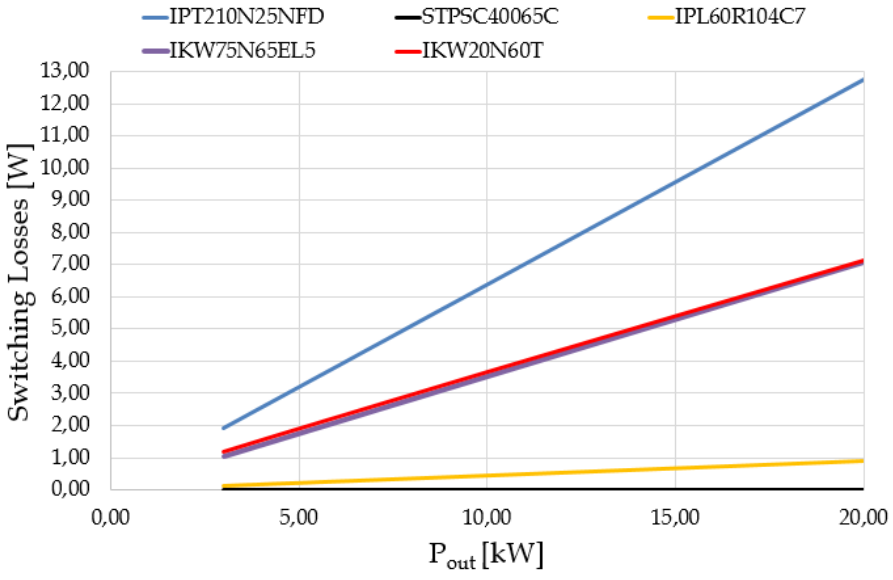


Fig. 141. Filters, auxiliary and fan losses vs. the output power.

It can be seen from Fig. 142a that on one side the IPT210N25NFD, STPSC40065C and IKW75N65EL5 devices show the dominant conduction losses, on the other side, the IPT210N25NFD, IKW20N60T and IKW75N65EL5 devices have the most significant switching losses, Fig. 142b. It must be noticed that the devices' losses take into account all the losses within the device package; then, the switches' losses take into account both body diode and antiparallel diode losses.



(a)



(b)

Fig. 142. Power Semiconductors Losses vs. output power: a) Conduction losses, b) Switching losses.

On the basis of the carried out investigation, we have the chance to operate on different factors in order to affect the efficiency value. Some of these are described in the following.

A. The devices S_{RP21}, S_{RP22}, S'_{RP21} and S'_{RP22}, with $P \in \{a, b, c\}$, are CoolMOS™C7 (IPL60R104C7), as highlighted in Fig. 143.

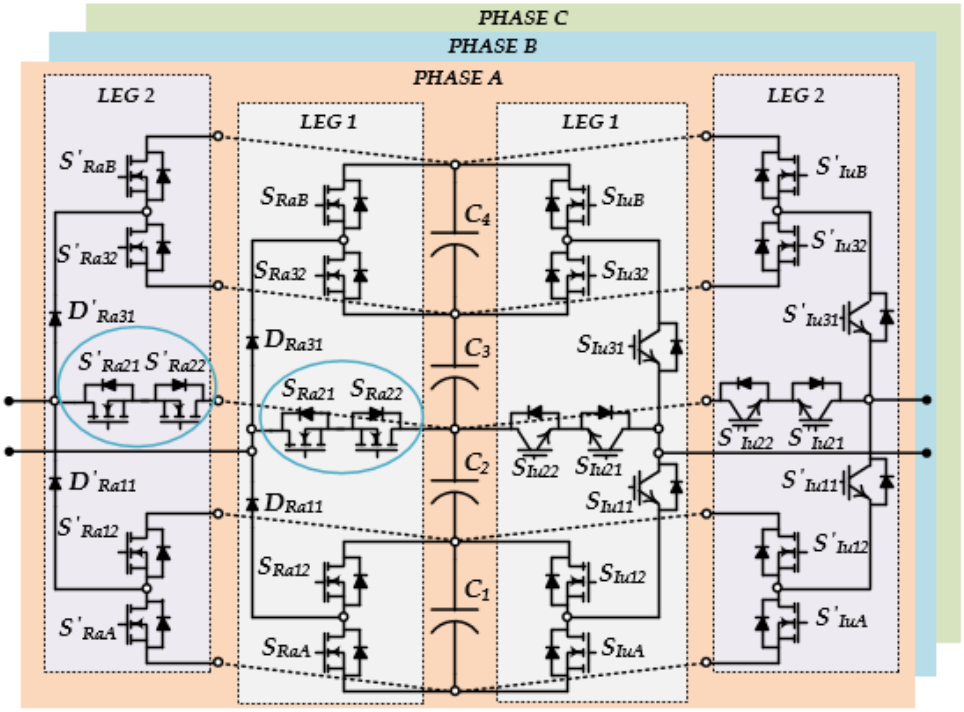


Fig. 143. 3ΦN5L E-Type BTB Converter.

The IPL60R104C7 CoolMOS™C7 devices could be replaced by IPL60R065C7 CoolMOS™C7 (650V, 65mΩ). The IPL60R065C7 device has the same footprint and it shows a better ohmic resistance r_{DS0} with respect to the IPL60R104C7 power semiconductor. As a result, the sum of the switching and the conduction losses related to the devices located in the middle-leg can be reduced at full load as shown in Table 43.

Table 43. Middle-leg losses into 3ΦN5L E-Type Rectifier.		
	IPL60R065C7	IPL60R104C7
S_{RP21}, S_{RP22}, S'_{RP21}, S'_{RP22}	5.74 W	7.5 W

B. The losses of the semiconductor devices in the Converter Power Stage have been estimated considering a junction temperature of 100°C, regardless of the loading conditions. However, the parameters of some devices strongly depend on the temperature. Particularly, the $R_{DS(on)}$ of the OptiMOS™3 and CoolMOS™C7 devices, S_{RPA}, S_{RPB}, S_{RP12}, S_{RP32}, S_{IQA}, S_{IQB}, S_{IQ12}, S_{IQ32} and S_{RP21}, S_{RP22} (switches are highlighted in red in Fig. 144), changes with the junction temperature. The MOS resistance $R_{DS(on)}$ increases when the junction temperature increases. As an example, Fig.

145 shows the peak and the full load efficiency of the Converter versus the junction temperature of only the OptiMOS™3 and CoolMOS™C7 devices (the other devices losses are still calculated at the fixed temperature of 100 °C).

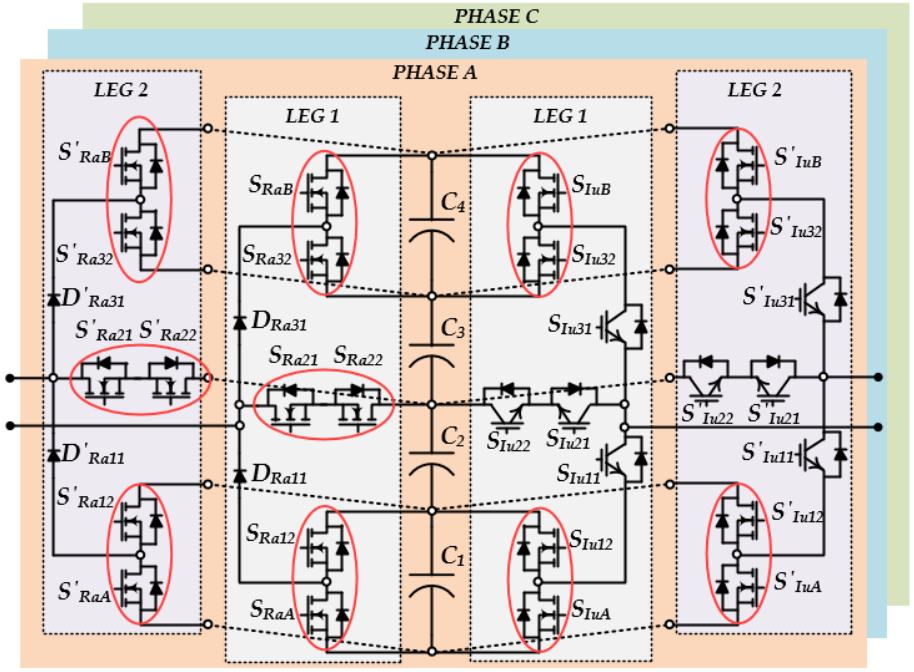


Fig. 144. 3ΦN5L E-Type BTB Converter: main temperature-dependent devices.

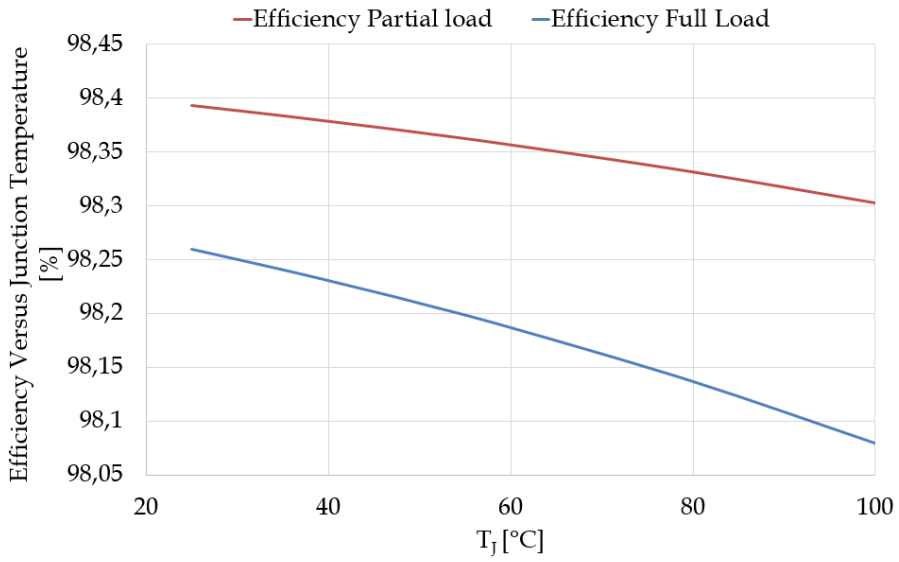


Fig. 145. Peak and full load efficiency versus junction temperature of the OptiMOSTM3 and CoolMOSTMC7 devices.

In general terms, the junction temperature is lower at partial load (it is fixed at half load in the example) compared to the full load operating

condition. Thus, an operating junction temperature below 100°C at partial load could reduce the conduction losses due to the smaller $R_{DS(on)}$ of the devices highlighted in red in Fig. 144. Further investigation is required to find the optimal solution between the heat-sink temperature and the needed fan speed (i.e. power consumption).

C. The switching frequency could be reduced if necessary. The filters have been designed in order to meet current ripple requirement even if the switching frequency slows down from 24kHz to 20kHz.

It is possible to combine the described options (A, B, C) in order to improve the efficiency. The peak efficiency and the full load efficiency versus the options are listed in Table 44.

Table 44. Peak Efficiency and Full Load Efficiency versus Improvement Option.

	System Condition	Peak Efficiency [%]	Full Load Efficiency [%]
1	DL1	98,30	98.08
2	Tj=80°C	98.33	98.14
3	f_{sw}=20 kHz	98.33	98.10
	1+2+3	98.36	98.16

As a result, during the experimental tests, the efficiency can be improved acting on two options, if needed. No hardware modifications are required as the options are implemented through the control system.

A. Junction temperature. The control system could act in order to have the heatsink temperature to the optimal value for the different operating conditions.

B. Switching frequency. The switching frequency can be reduced or even modulated in the range 24 kHz to 20 kHz at different load conditions in order to optimize the efficiency.

PART FIVE

CONTROL STRATEGY ASPECTS

11 3ΦN5L E-TYPE BTB CONVERTER CONTROL STRATEGY

11.1 Adaptive Control Strategy

Two different control strategies have been used to obtain the craved input and output waveforms.

11.1.1 3ΦN5L E-Type Rectifier Control Strategy

A control structure related to the entire feedback chain rectifier is shown in Fig. 146. In this case, the DC-bus voltage is regulated by external circuit. The only quantities to track are the input currents ($i_{ref,a}$, $i_{ref,b}$, $i_{ref,c}$).

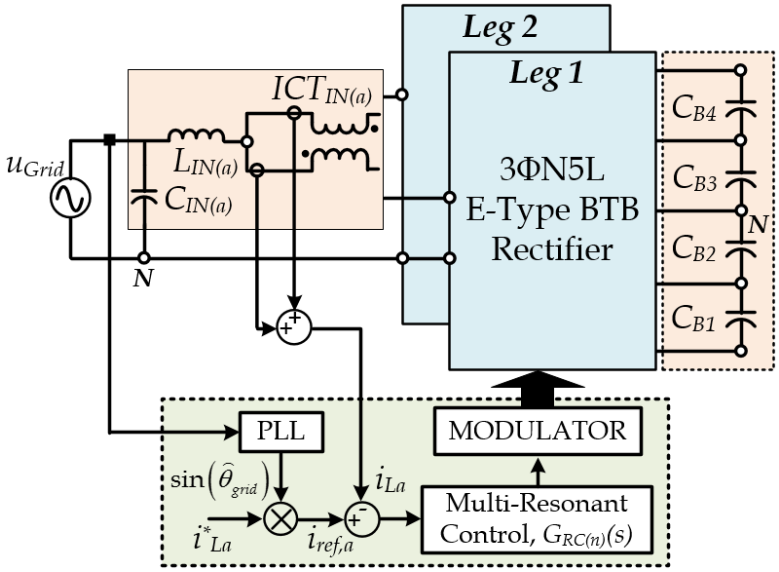


Fig. 146. Control loop structure 1ΦN5L E-Type Rectifier.

As it can be seen from Fig. 146, the regulator current is the 3-Degree of freedom multi-resonant controller (MRC) [168]. The transfer function $G_{RC(n)}(s)$ is defined in (206), where n is the number of harmonics, $k_{ir(n)}$, $\theta_{(n)}$, $\omega_{cr(n)}$, and $\omega_{0(n)}$ are the gain, phase, width and resonance frequency of the controller, respectively; h is intended as the maximum harmonic order that is included in the multi-resonant controller.

$$G_{RC(n)}(s) = \sum_{n=1}^{h} 2k_{ir(n)}\omega_{cr(n)} \frac{s\cos(\vartheta_{(n)}) + \omega_{cr(n)} - \omega_{0(n)}\sin(\vartheta_{(n)})}{s^2 + 2\omega_{cr(n)}s + \left(\omega_{cr(n)}^2 + \omega_{0(n)}^2\right)} \tag{206}$$

The multi- resonant controller is discretized on-line and the coefficients updated are downloaded on the FPGA. The single-phase phase-locked loop (PLL) system used to derive the grid phase $\hat{\theta}_{grid}$ has been implemented according the method shows in [169]. The block scheme of the single-phase PLL is depicted in Fig. 147.

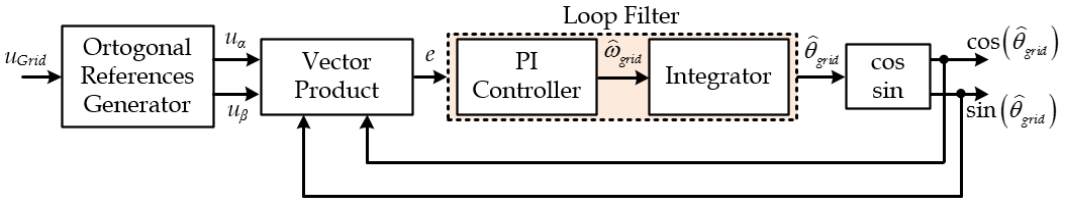


Fig. 147. Block scheme of the single-phase PLL.

The block orthogonal signal generator (OSG) provides the two-quadrature signals $u_\alpha = V_s cos(\theta_{grid})$ and $u_\beta = V_s sin(\theta_{grid})$, where V_s is the module of the grid voltage phasor. The signal error e, provides by the vector product block, is given in (207), where $\sin(\hat{\theta}_{grid})$ and $\cos(\hat{\theta}_{grid})$ are the sine and the cosine of estimated grid angle provided by the PLL system.

$$e = \frac{u_\beta \cos\left(\hat{\theta}_{grid}\right) - u_\alpha \sin\left(\hat{\theta}_{grid}\right)}{V_s} = \\ = \sin\left(\theta_{grid} - \hat{\theta}_{grid}\right) = \sin\left(\theta_{grid}\right)\cos\left(\hat{\theta}_{grid}\right) - \cos\left(\theta_{grid}\right)\sin\left(\hat{\theta}_{grid}\right) \cong \theta_{grid} - \hat{\theta}_{grid} \tag{207}$$

The loop filter block, composed by proportional integral regulator (PI) and integrator, performs the estimation of the phase angle of the grid voltage phasor $\hat{\theta}_{grid}$. Finally, the last block determines the values of the sine and cosine of phase angle which can be obtained through a numerical procedure or a look-up table.

11.1.1 3ΦN5L E-Type Inverter Control Strategy

The block scheme of the inverter control loop is depicted in Fig. 148. The inverter control strategy is called "Concurrent control". In this control strategy two reference signals are tracking: output voltage and current. This is particularly useful in UPS applications due to a potential short-circuit. In other words, the 3ΦN5L E-Type Converter must be able to withstand three times the

nominal current on the single phase per 60 milliseconds before shutdown the converter (turned-off switches).

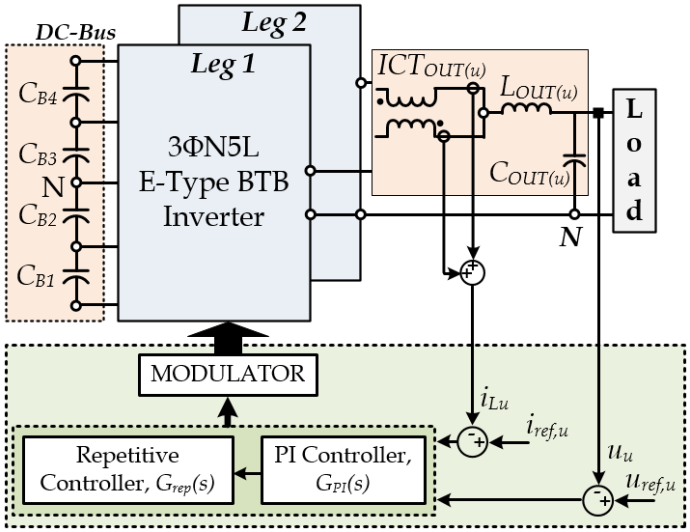


Fig. 148. Control loop structure Inverter.

Consequently, the control always adjusts the voltage reference. When an overcurrent is detected (with an overcurrent circuit) the control structure adjusts the current reference per 60 milliseconds before opening all the switches. The reference signals, $i_{ref,u}$ and $u_{ref,u}$ are defined in (208), where V^*_{OUT} and I^*_{OUT} are the output RMS voltage and RMS current.

$$u_{ref,u} = \sqrt{2}V^*_{OUT}\sin(\omega_{OUT}t),\quad i_{ref,u} = 3I^*_{OUT}\,\mathrm{sgn}\left[sin(\omega_{OUT}t)\right] \tag{208}$$

The control algorithm has been implemented using the repetitive controller plus PI controller. The implementation of a time delay in repetitive controller is a complicated point in continuous-time. Fortunately, in discrete time it is an easier task. If the reference signal period T_0 is a multiple of the sampling period T_{sw}, the digital implementation is reduced to a circular queue. Fig. 149 shows the block scheme of the repetitive controller and its control transfer function in the discrete domain is given in (209), where z^{-N} is the delay line, with $N=T_0/T_{sw}$, k_{RC} is the repetitive learning gain and $Q_R(z)$ is the robustness filter. Since the switching frequency is 24 kHz and fundamental frequency is 50 Hz, the number N is 480.

$$G_{Rep}(z) = k_{RC}\frac{z^{-N}}{1-Q_R(z)z^{-N}} \tag{209}$$

The use of the robustness filter $Q_R(z)$ is to modify the internal model, which effectively increases the system stability margin.

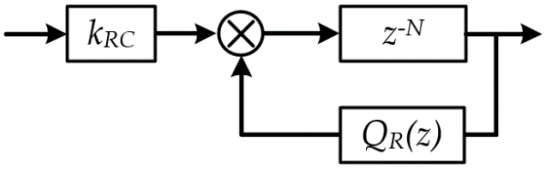


Fig. 149. Block scheme of the repetitive controller.

The transfer function of the PI controller is given in (210), where k_p, k_i denote the coefficients for the proportional and integral terms, respectively.

$$G_{PI}(s) = k_P + \frac{k_I}{s} \tag{210}$$

Additionally, both in the rectifier and inverter there is an additional loop in order to obtain an equal current distribution between the two ICT's windings.

11.2 Control algorithm implementation

The rectifier and inverter control algorithm have been implemented in LabVIEW. The resulting program is composed by three targets: FPGA, real-time (RT) and host. The most demanding tasks, like control loops, PWM signals, protections and connecting devices, runs on the FPGA. The less demanding tasks such as Graphical User Interface (GUI) are executed on the RT. Finally, the non-deterministic tasks such as handling the GUI runs on the host target. The block diagram of the implemented control algorithm is depicted in Fig. 150.

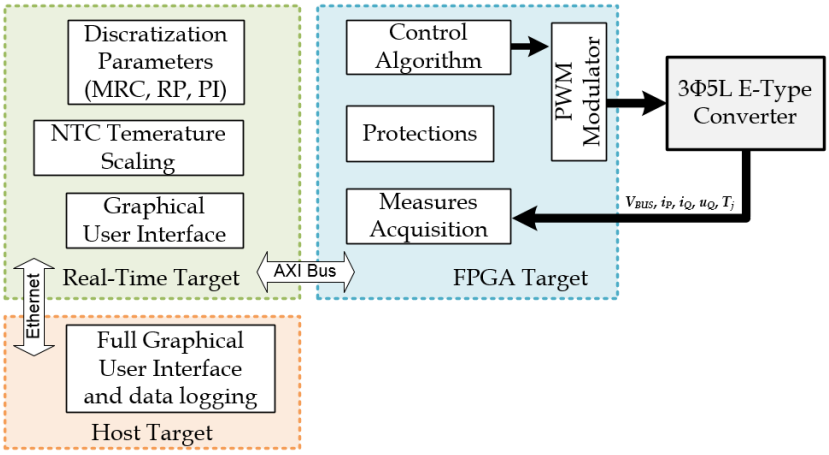


Fig. 150. Block scheme control algorithm on LabVIEW.

Communication between host and RT target is physically realized by the Ethernet link. If, for any reason the Host fails, RT and FPGA targets continue running without any issue, as well they can perform specifics user defined tasks. FPGA is not able to communicate directly to the host, for this reason the RT system is always the link between them.

11.2.1 FPGA Target

The FPGA code structure is illustrated in Fig. 151. Each block runs in different frequencies.

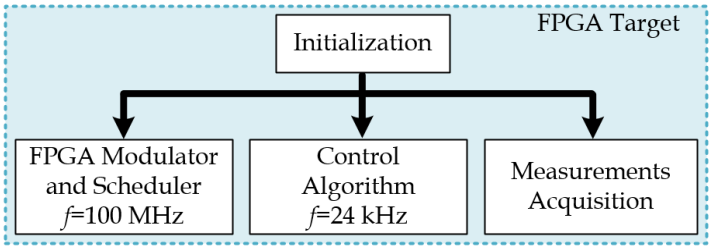


Fig. 151. FPGA code structure.

The Virtual Instruments (VI) starts performing once the initialization task. In this task are initialized the Digital Analogic Converter (DAC), Analogic Digital Converter and Digital I/O which are present on the Ped-board. The switching frequency and dead-time are set in ticks according to the equations (211) and (212).

$$f_{SW}[ticks] = \frac{Core\ Clock[kHz]}{2 \cdot f_{SW}[kHz]} \tag{211}$$

$$DT[ticks] = \frac{DT[\mu s] \cdot Core\ Clock[MHz]}{2} \tag{212}$$

Fig. 151 shows the FPGA modulator and scheduler with also the FIFO Item used to synch the control loop. The scheduler is the same for both the rectifier and inverter. PWM modulator is realized by an up/down counter and it is capable to insert the required dead-time between any pair of switches. At the beginning of the PWM period, the control task is called with the possibility to introduce a down sampling. Additionally, FPGA accomplishes measure acquisition directly controlling the PED-Board ADCs, overcurrent, over voltage, over temperature

scaling and protections, as shown in Fig. 153.

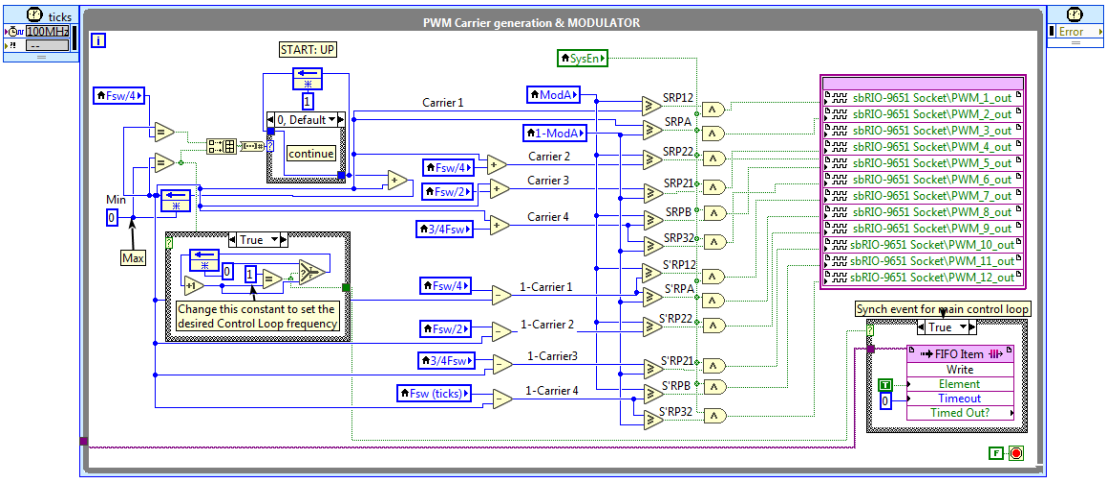


Fig. 152. PWM modulator and scheduler.

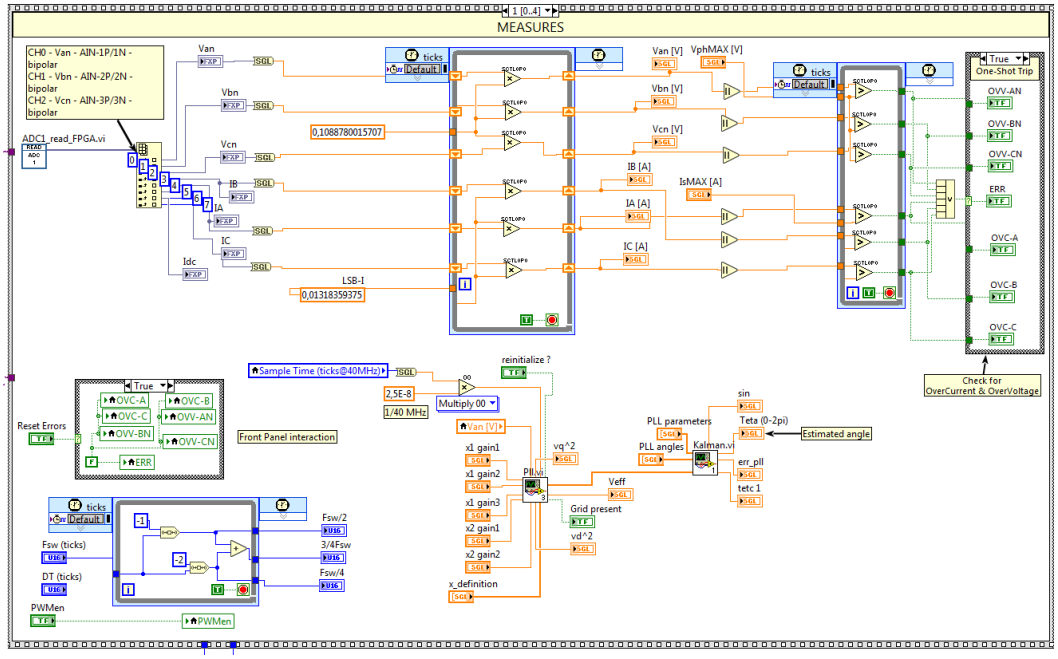
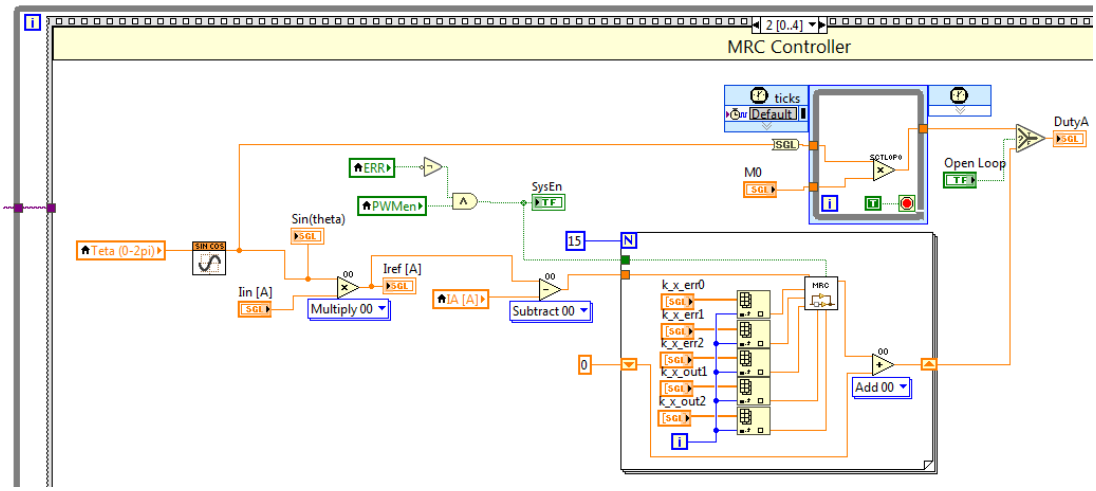
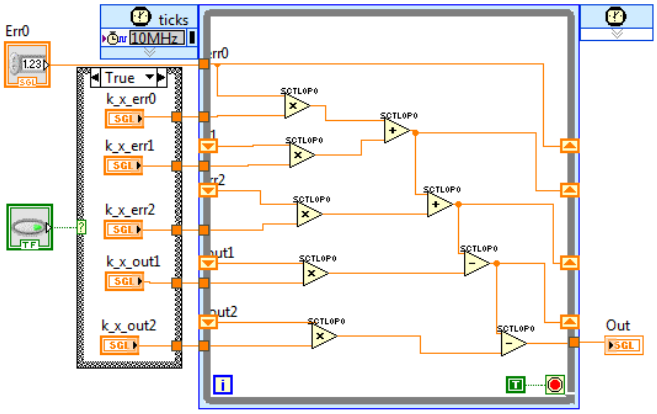


Fig. 153. Acquisition measures tasks.

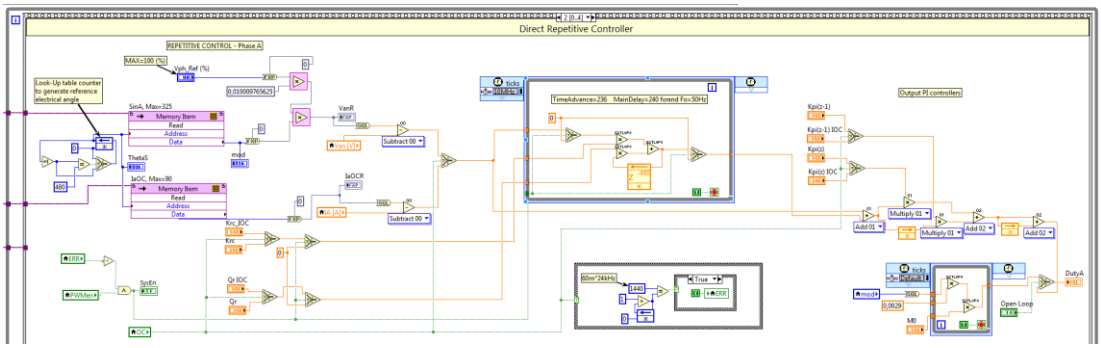
As it can be seen from Fig. 153, the estimated grid phase $\hat{\theta}_{grid}$ is obtained using the subVI named "Pll.vi" and "Kalman.vi" whose input parameters are provided by Real-Time Target. The multi-resonant controller and the repetitive control plus PI controller have been implemented on FPGA, Fig. 154.



(a)



(b)



(c)

Fig. 154. a) Multi-resonant controller code; b) MRC Sub-VI code
c) Repetitive Control plus PI code.

11.2.2 Real-Time Target

RT target receives data from the FPGA and mainly manages the Graphical User Interface (GUI). The GUI is illustrated in Fig. 155. It can be noticed how the high-level target is able to manage and illustrate to the user the rectifier or inverter

operating conditions: currents, voltage, faults, on-line discretization of controllers and FPGA and RT executions time.

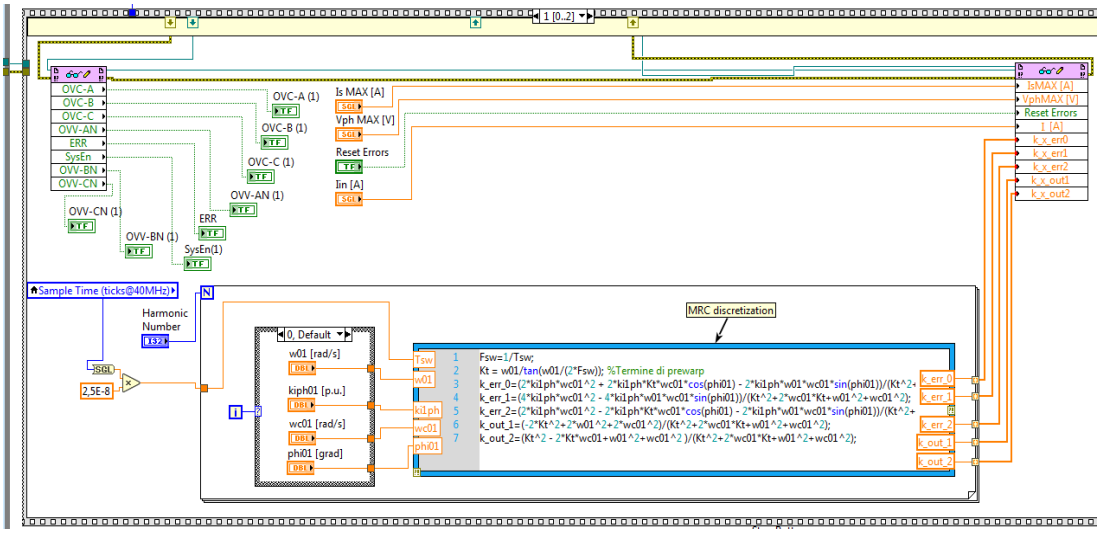


Fig. 155. Discretization parameters on Real-Time target.

Discretization of the multi-resonant controller amplitude $M_{RC(n)}$ and phase $\theta_{(n)}$, regulator proportional and integral gain and repetitive control coefficients, k_{R1}, k_{R2} are operated by the RT target. The resulting outputs are sent to the FPGA. Furthermore, the discretization of the repetitive control parameters occurs on the real-time target.

11.3 Open Loop Results

The open-loop tests of the 1ΦN5L BTB E-Type Rectifier and Inverter have been performed in order to verify the correct operation of the PWM modulator and PLL. To this purpose, the control board shown in Fig. 53 has been used. The estimated grid phase $\hat{\theta}_{grid}$ and the current reference $i_{ref,a}$ are shown in Fig. 156. The effectiveness of the proposed PWM modulator has also been tested, acquiring the modulating signal and the control signals of the related power devices.

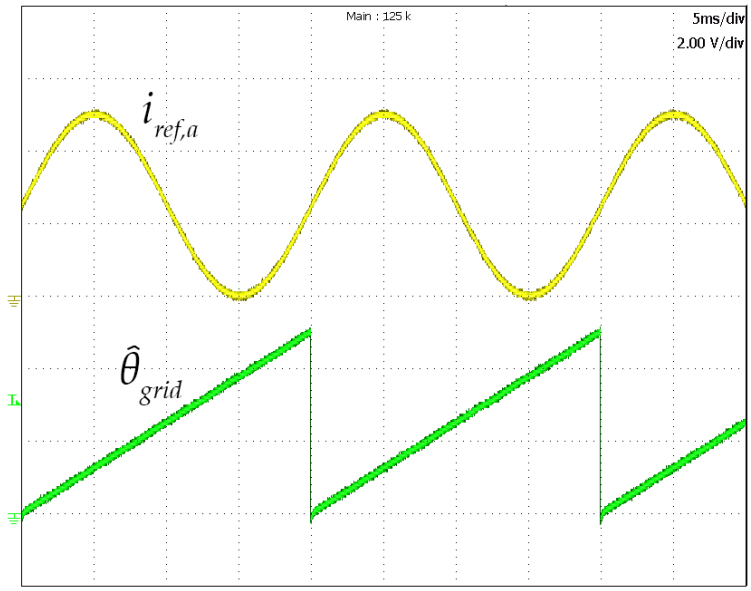


Fig. 156. Estimated grid phase $\hat{\theta}_{grid}$ (green line) and current reference $i_{ref,a}$ (yellow).

The comparison between the experimental and simulation control signals linked to each power semiconductor of the single-phase rectifier and inverter are shown in the following figures.

- **Rectifier Modulator**

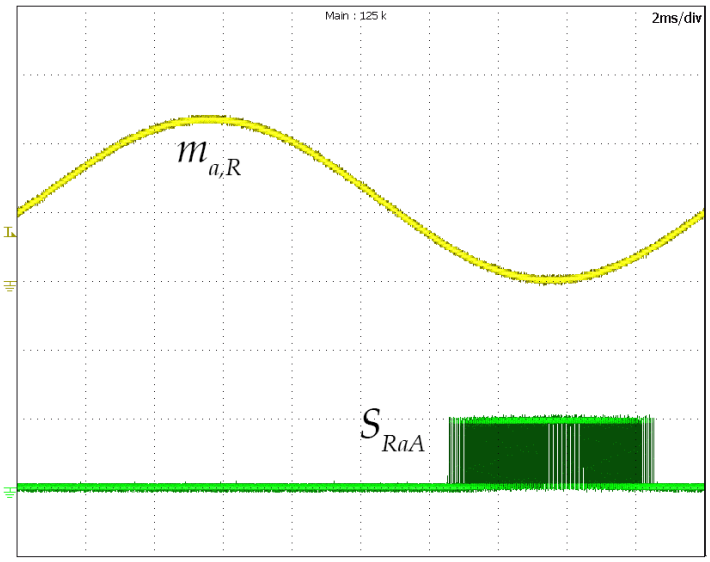


Fig. 157. PWM signal S_{RaA}: experimental results (2 V/div).

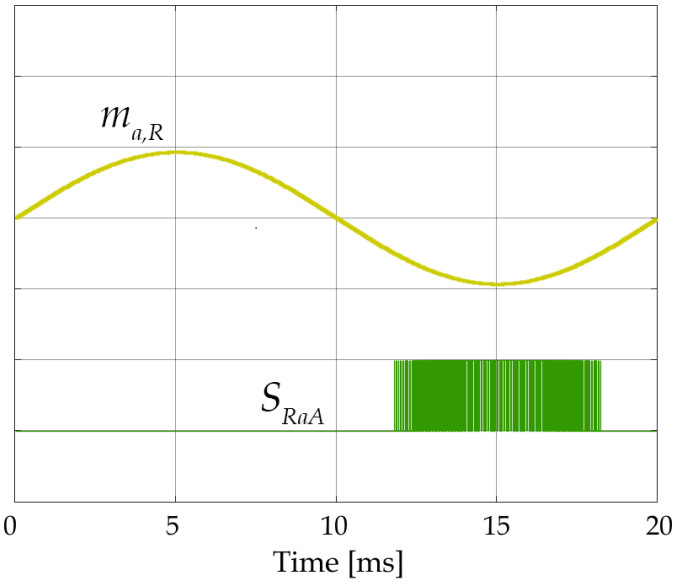
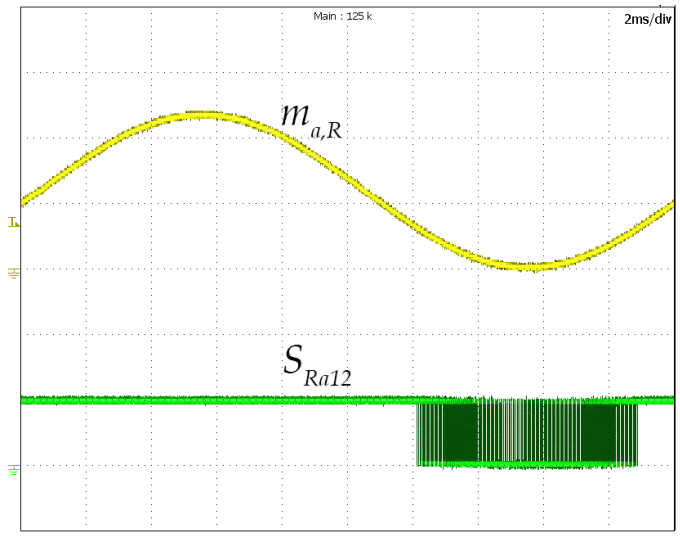
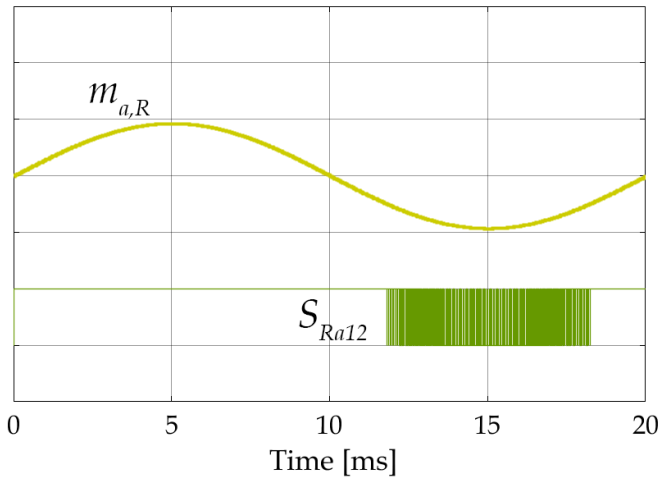


Fig. 158. PWM signal S_{RaA}: simulation results.

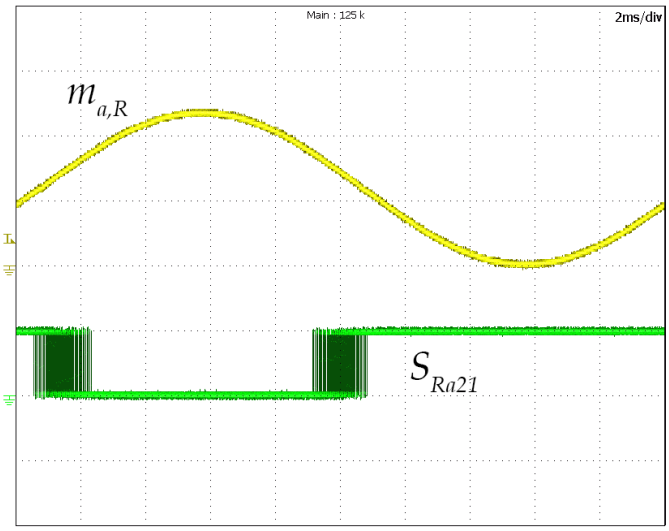


(a)

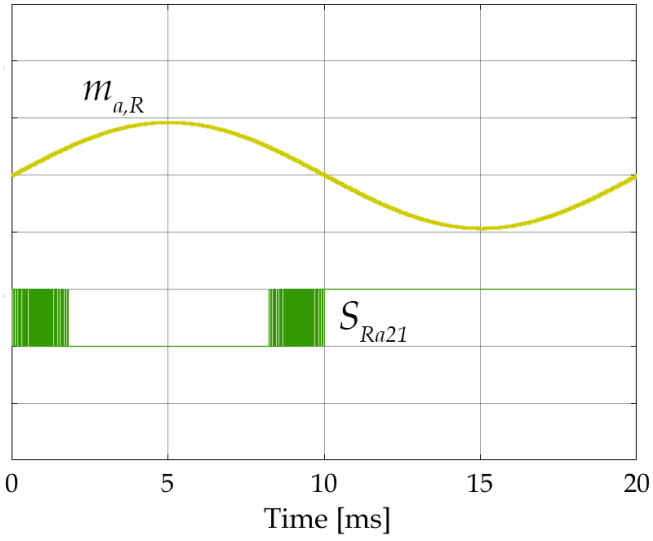


(b)

Fig. 159. PWM signal S_{Ra12}. a) experimental results (2 V/div), b) simulation results.



(a)



(b)

Fig. 160. PWM signal S_{Ra21}. a) experimental results (2 V/div), b) simulation results.

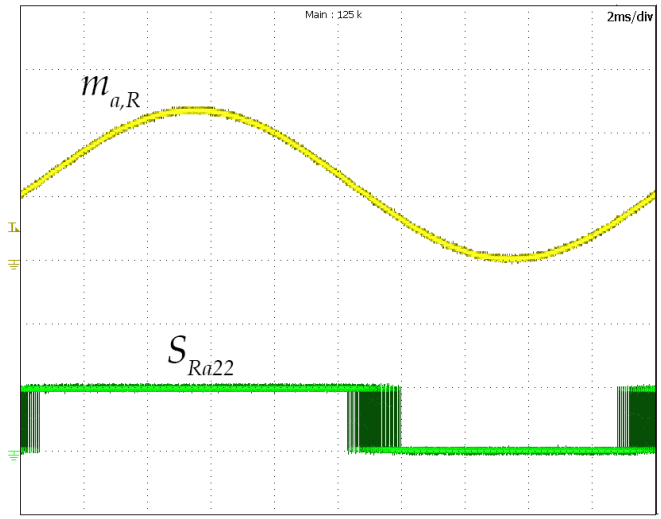


Fig. 161. PWM signal S_{Ra22}: experimental results (2 V/div).

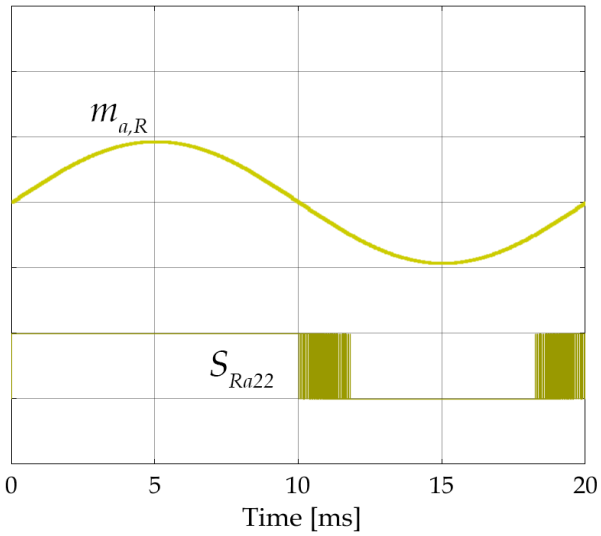
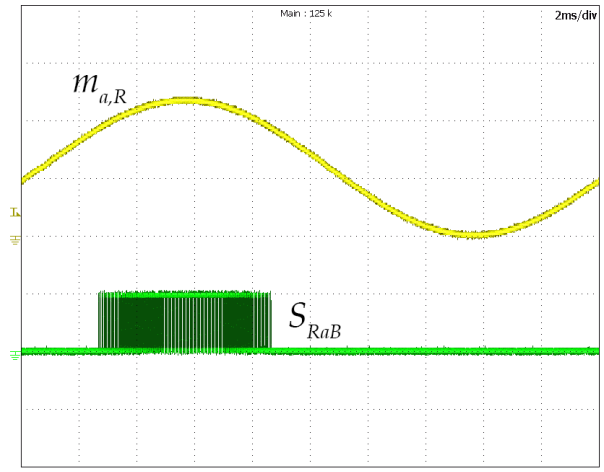
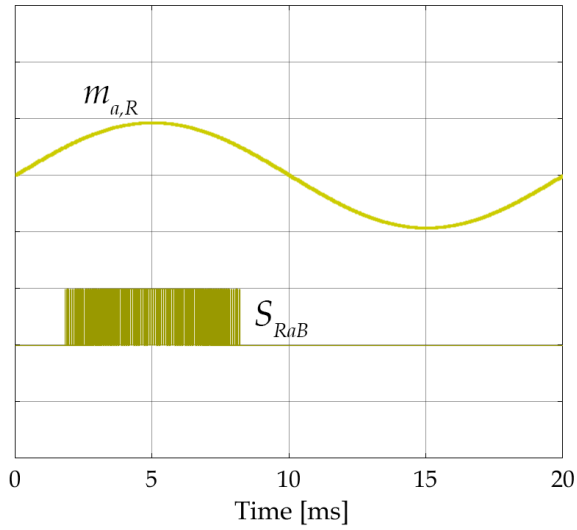


Fig. 162. PWM signal S_{Ra22}: simulation results.

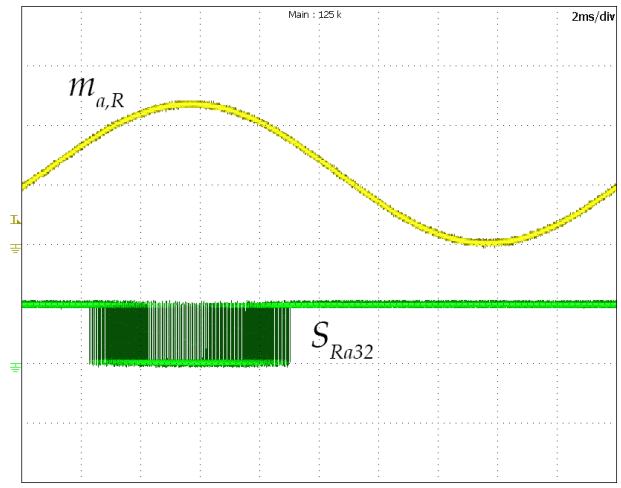


(a)

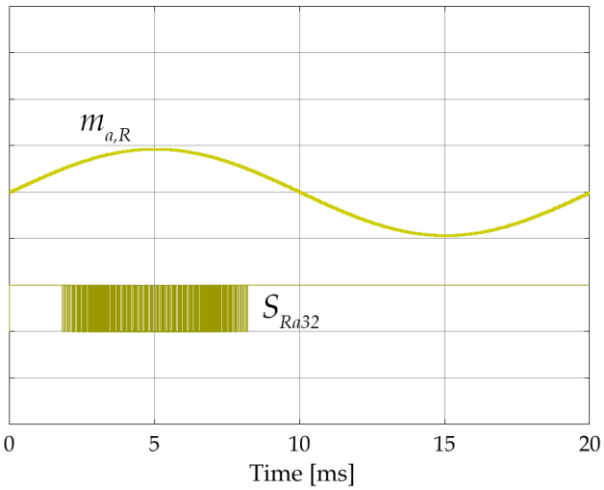


(b)

Fig. 163. PWM signal S_{RaB}. a) experimental results (2 V/div), b) simulation results.



(a)



(b)

Fig. 164. PWM signal S_{Ra32}. a) experimental results (2 V/div), b) simulation results.

- Inverter Modulator

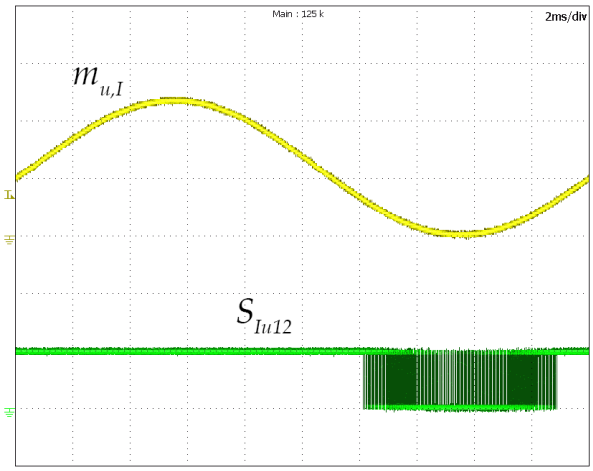


Fig. 165. PWM signal S_{Iu12}: experimental results (2 V/div).

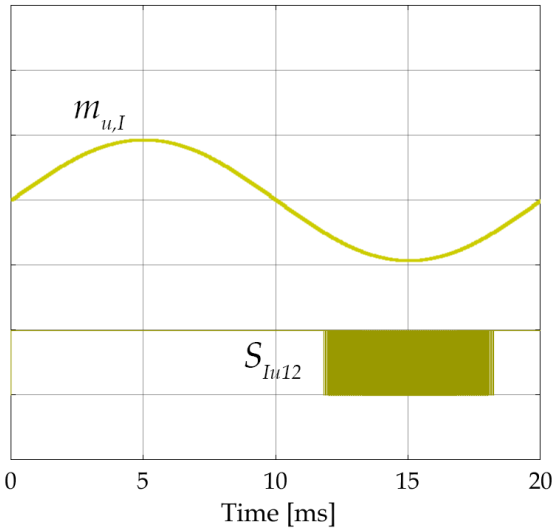
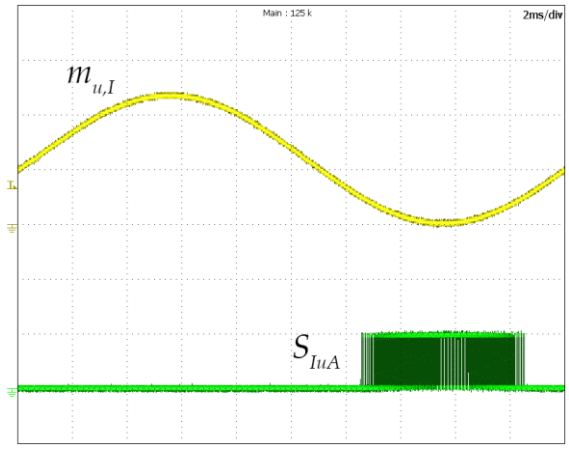
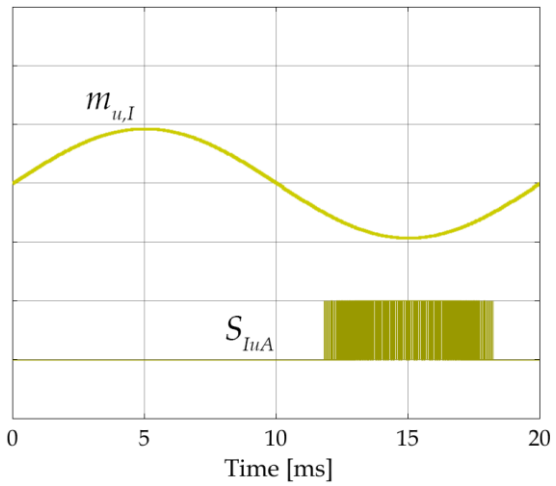


Fig. 166. PWM signal S_{Iu12}: simulation results.

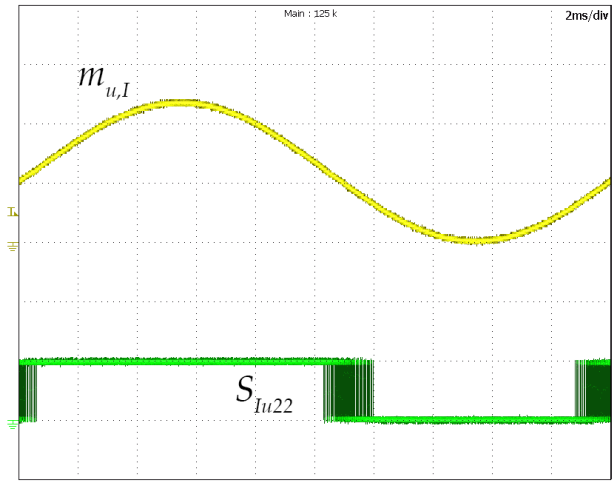


(a)

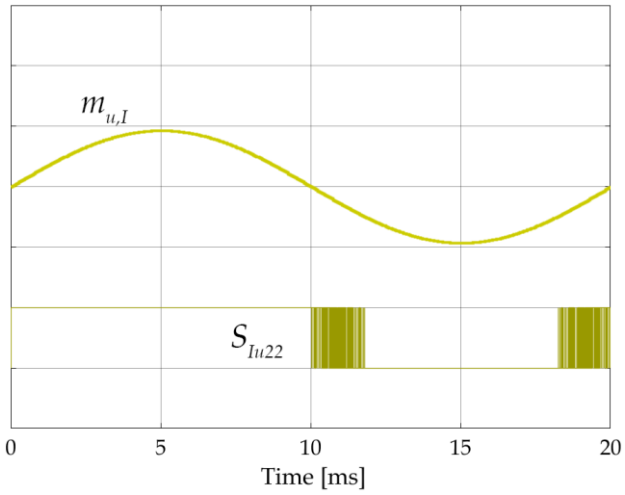


(b)

Fig. 167. PWM signal S_{IuA}. a) experimental results (2 V/div), b) simulation results.



(a)



(b)

Fig. 168. PWM signal S_{Iu22}. a) experimental results (2 V/div), b) simulation results.

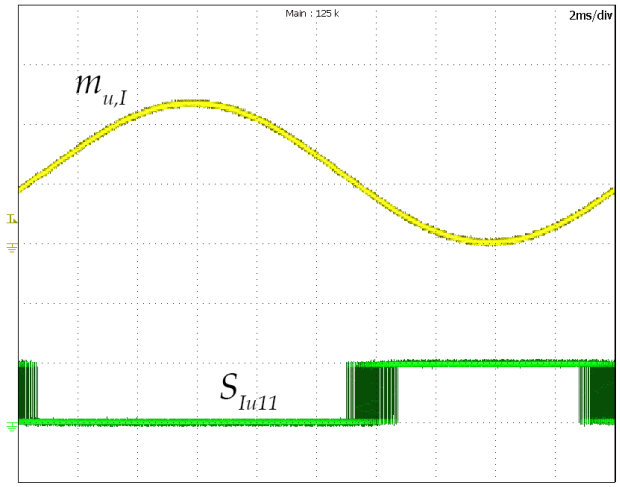


Fig. 169. PWM signal S_{Iu11}: experimental results (2 V/div).

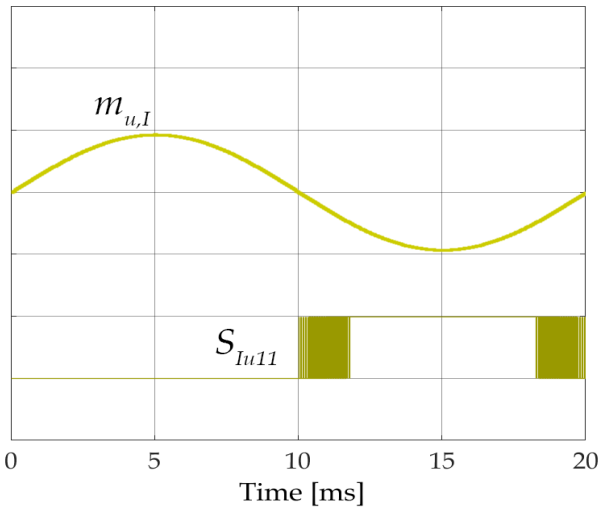
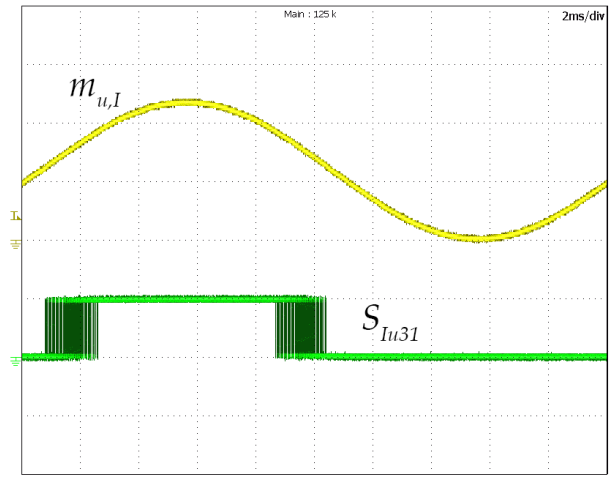
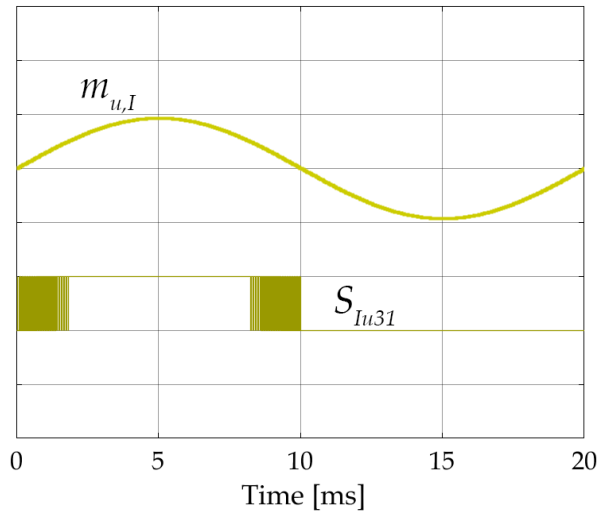


Fig. 170. PWM signal S_{Iu11}: simulation results.

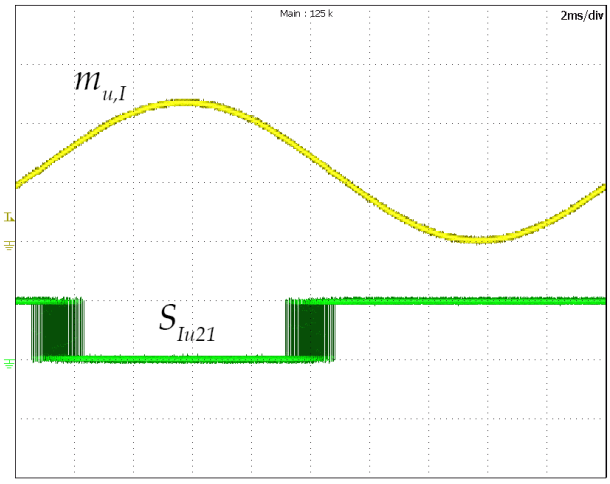


(a)

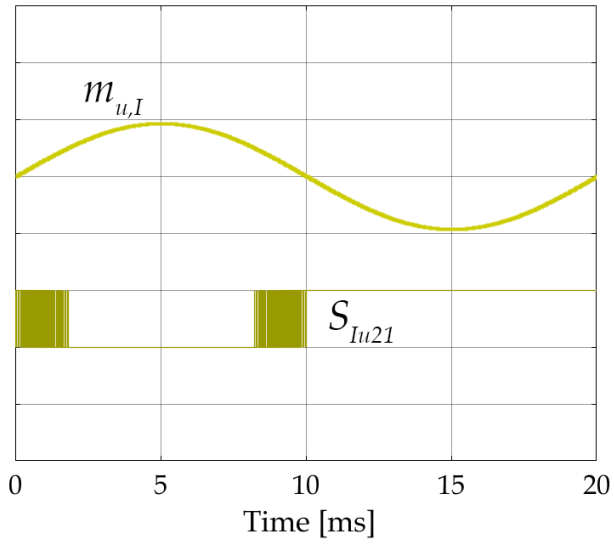


(b)

Fig. 171. PWM signal S_{Iu31}. a) experimental results (2 V/div), b) simulation results.



(a)



(b)

Fig. 172. PWM signal S_{Iu21}. a) experimental results (2 V/div), b) simulation results.

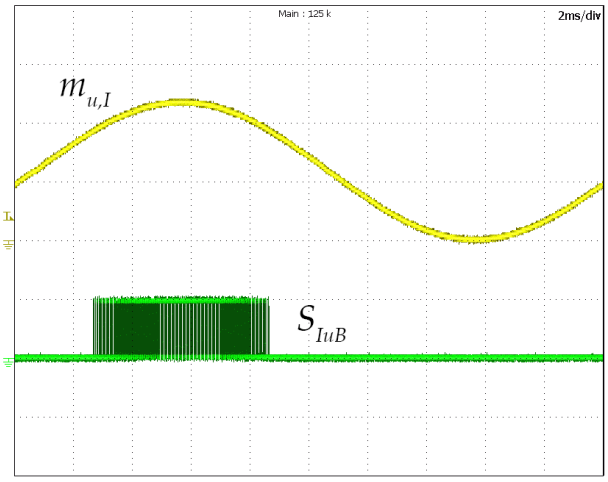


Fig. 173. PWM signal S_{IuB}: experimental results (2 V/div).

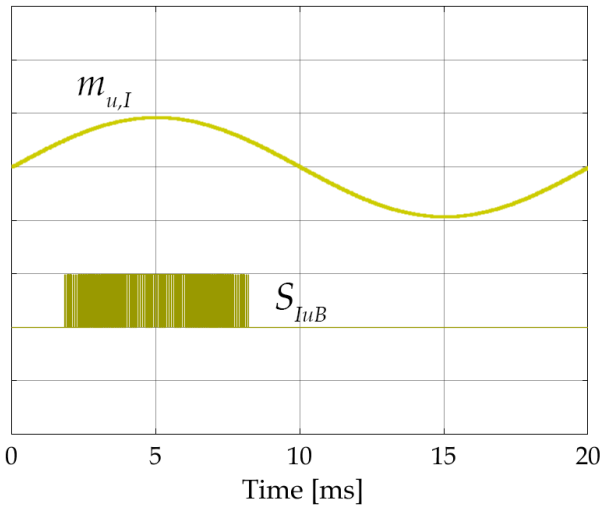
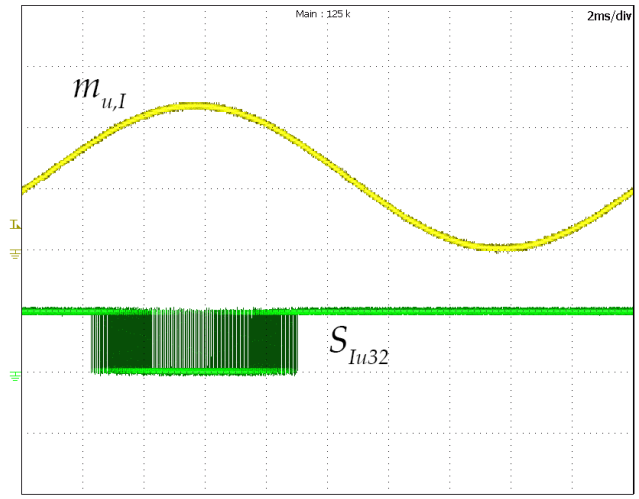
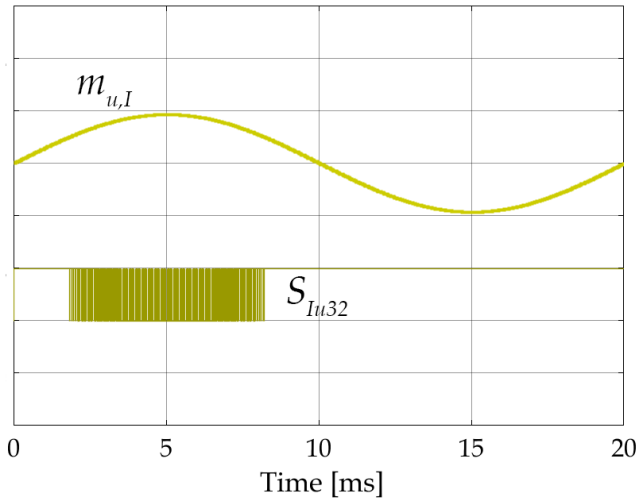


Fig. 174. PWM signal S_{IuB}: simulation results.



(a)



(b)

Fig. 175. PWM signal S_{Iu32}. a) experimental results (2 V/div), b) simulation results.

Furthermore, the dead-time of 1µs has been implemented into control algorithm. Fig. 176 shows the control signals in opposite phase between S_{IuB} and S_{Iu32}. Looking at Fig. 176, it can be noticed the effective dead-time of the devices.

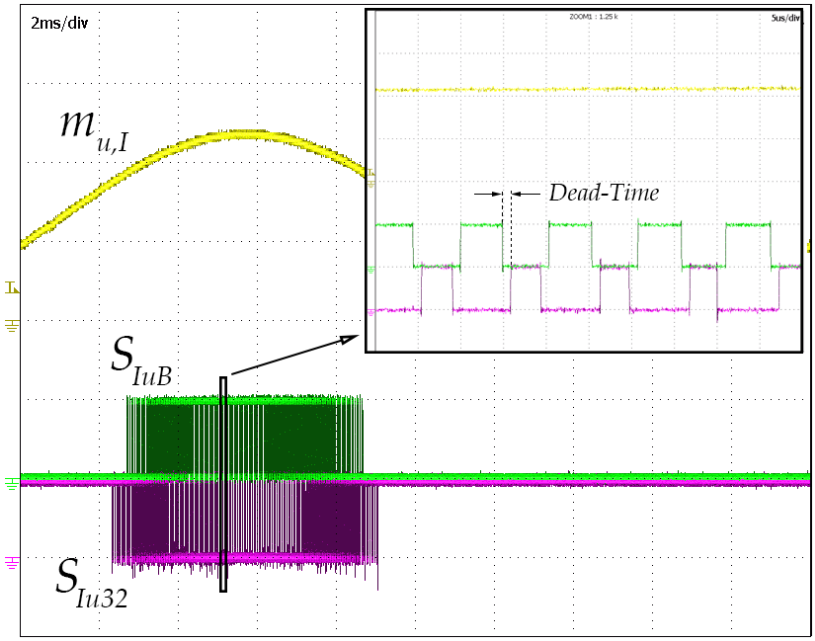


Fig. 176. Control signals with dead-time between S_{IuB} and S_{Iu32}.

11.4 Closed-Loop Results

The closed-loop control algorithm has been validated using the co-simulation capabilities between NI Multisim and LabVIEW. The co-simulation process of the system is represented in Fig. 177.

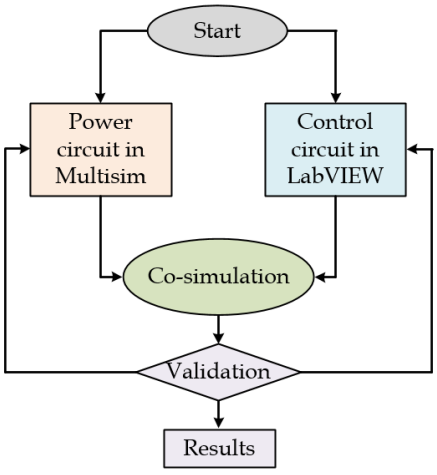
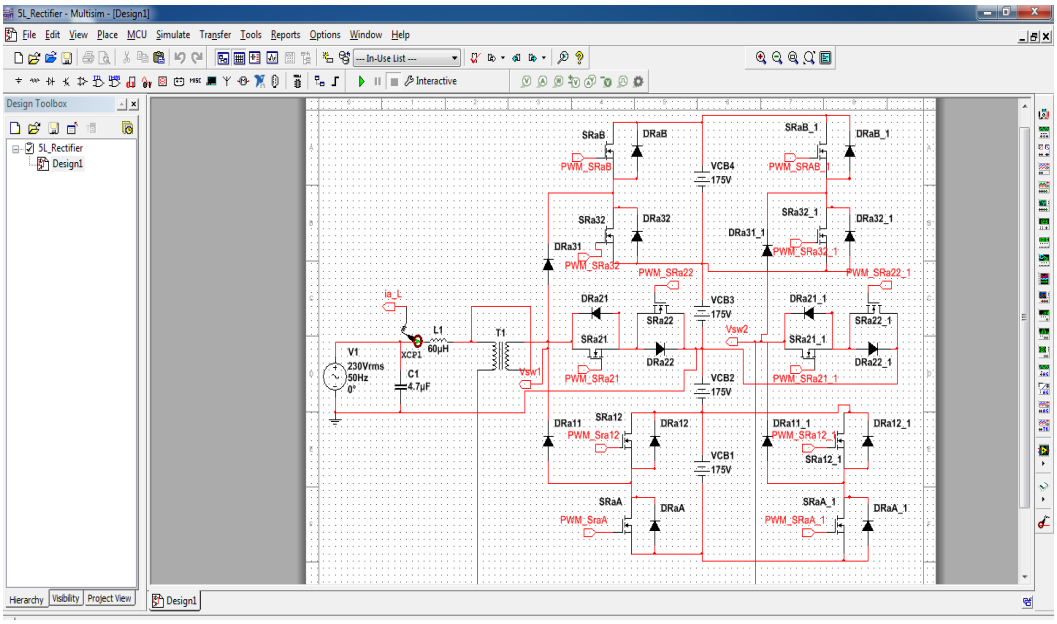


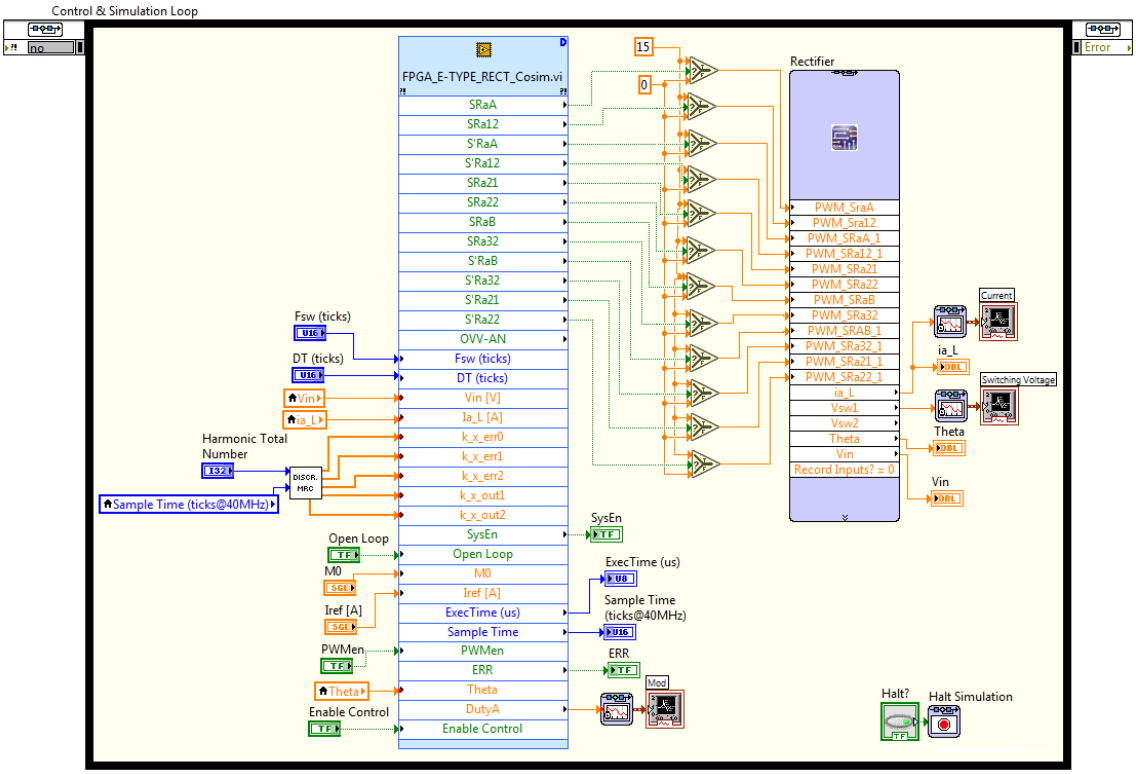
Fig. 177. Co-simulation Process.

The NI Multisim is a modeling tool of the electronic circuit which can be

interfaced with the LabVIEW. The power circuit of the 3ΦN5L BTB E-Type Converter has been built in NI Multisim environment. Fig. 178a shows the 3ΦN5L E-Type Rectifier built in NI Multisim.



(a)

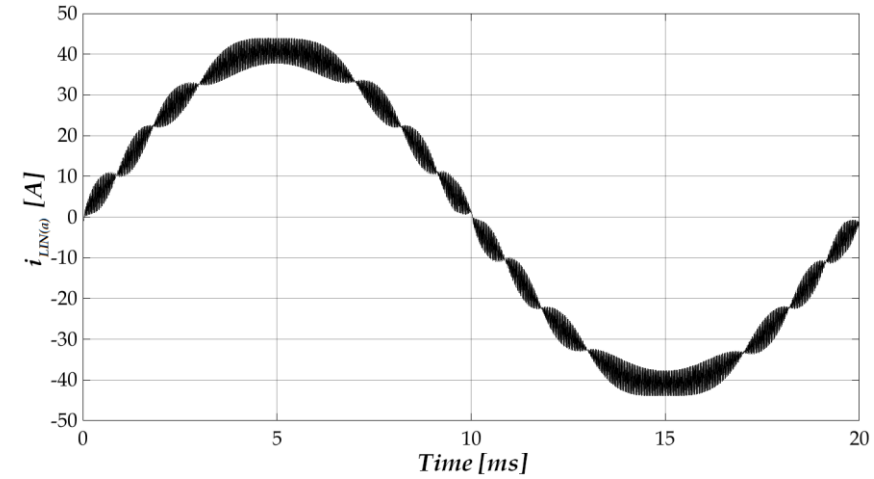


(b)

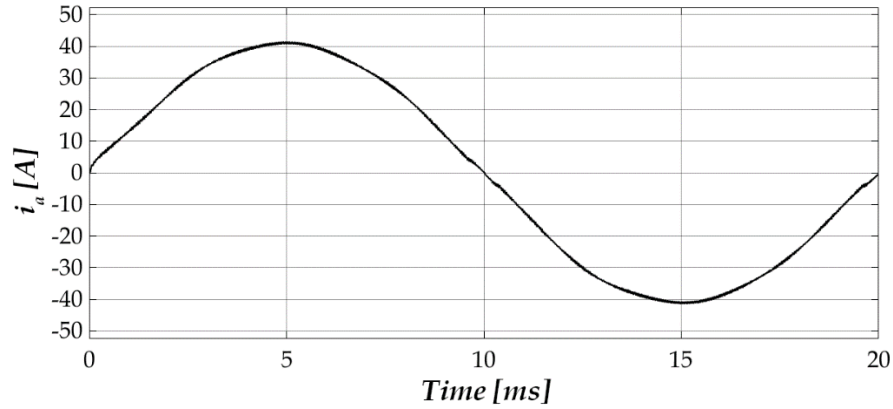
Fig. 178. a) Screenshot of the 3ΦN5L BTB E-Type Rectifier built in NI Multisim; b) screenshot of the simulation loop between the FPGA and Multisim.

Communication between implemented control algorithm in FPGA target and the

converter built in Multisim is realized inside the "Control and Simulation Loop" in Host target, as shown in Fig. 178b.



(a)



(b)

Fig. 179. a) Input Inductor Current; b) Input current.

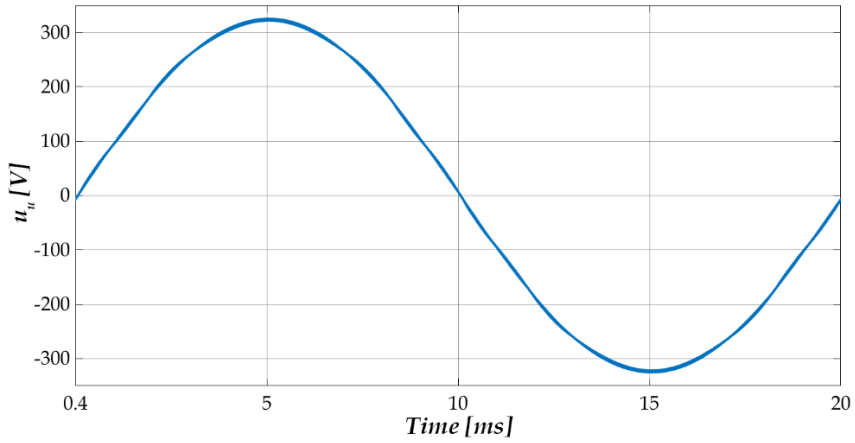
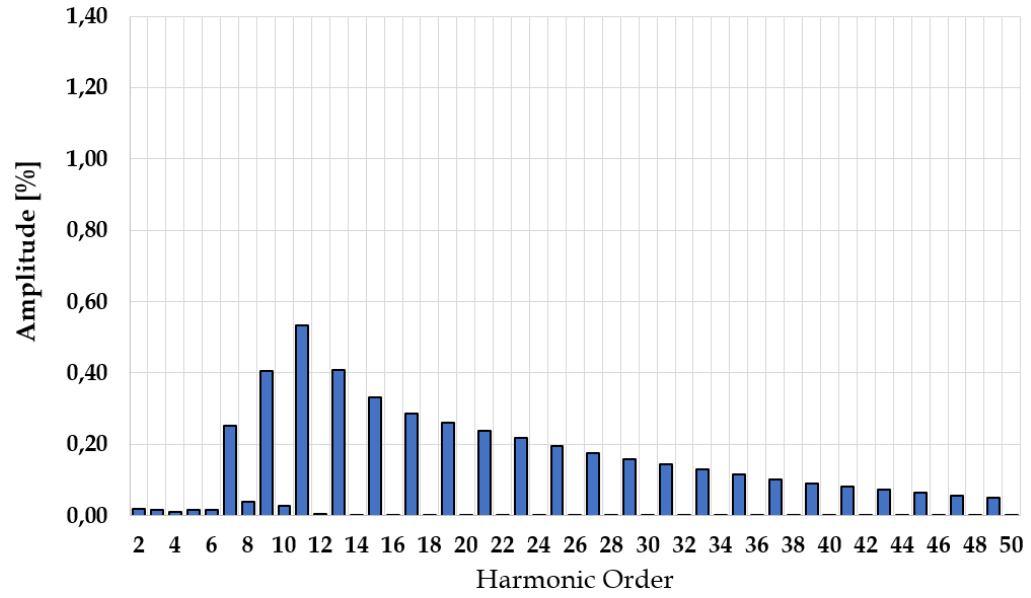


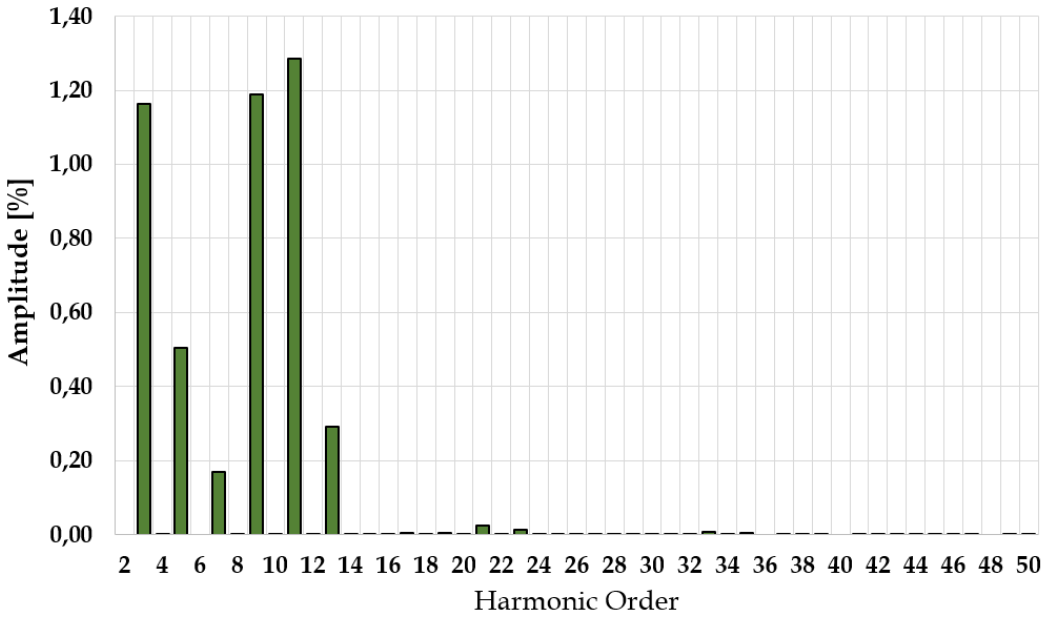
Fig. 180. Output Voltage.

Fig. 179 and Fig. 180 show the input inductor current $i_{LIN(a)}$, input current i_a and the output voltage u_u, respectively. The input current and output voltage

harmonics contents up to 50th order normalized with respect to the fundamental harmonic are depicted in Fig. 181. According to the IEEE STD 519-2014 and IEC 61000-2-4 international standards, the total harmonic distortion of the input current THD_i and output voltage THD_u, estimated considering the harmonic components up to the 50th order, are equal to 1.10 % and 0.66 %, respectively.



(a)



(b)

Fig. 181. Harmonic contents: a) input current i_a, b) output voltage u_u.

Finally, the output and reference currents under the short-circuit condition are shown in Fig. 182. The 1ΦN5L BTB E-Type Inverter is generally controlled

through the voltage control mode during the normal operation. When the short circuit fault occurs, the phase voltage decreases and the phase current increases (peak current). In this condition, the control changes in "current control mode" and the phase current i_u starts to track its reference $i_{ref,u}$.

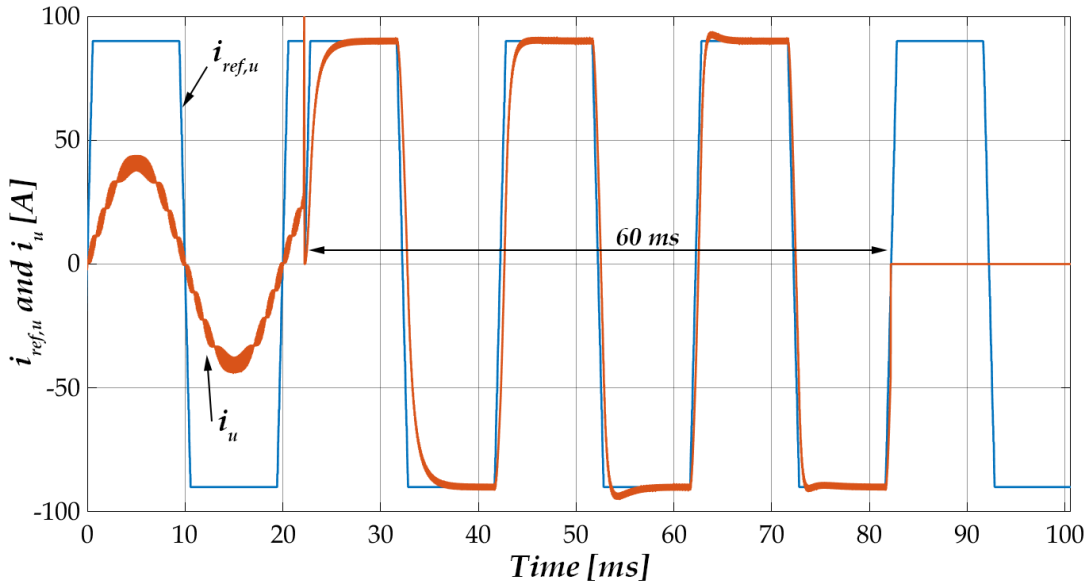


Fig. 182. Short circuit capability.

The reference signal $i_{ref,u}$ is a square wave with the fundamental frequency of 50 Hz and the amplitude equal to 3 times the RMS phase current. After 60 milliseconds, the converter is turned off by opening all the switches.

CONCLUSIONS

The first part of the dissertation has dealt with the background of the multi-level topologies and then a review of the 5 level BTB multi-level converters and patents in industrial applications has been carried-out. Particularly, motivations and requirements for multi-level conversion have been clearly explained. Each one of multi-level BTB topologies has its own pros and cons which give a great flexibility to select the right topology for each application. The main advantages of the three-phase multi-level converter topologies can be briefly summarized:

- lower common mode voltage,
- smoother waveform with lower THD,
- less distorted input current and lower switching frequency,
- lower switching loss.

Three-phase multi-level converters have also some drawbacks like a higher number of active components which results in lower reliability. Furthermore, additional circuits can be used to balance the capacitor voltages and long commutation path can cause high total commutation inductance, which means high over-voltages. All this leads to circuit higher cost and to circuit control higher complexity. However, the drawbacks resulting from the use of three-level or multi-level converters can be neglected in comparison to their numerous advantages. Finally, a description of the three-phase BTB systems and multi-level converters protected by patents has been performed in order to identify existing solutions in the industrial environment.

After examining the multi-level converter topologies, the T-Type multi-level converter has been identified as the most promising configuration, thanks to its specific features in terms of current path and commutation inductance. Thus, the 3Φ5L E-Type Rectifier for high-speed electrical drive has been analyzed in great details. The working principle of the rectifier has been explained. The 3Φ5L E-Type Rectifier has been carefully studied by considering the combination of high

speed IGBT, SiC Schottky diodes, and Si rapid switching diodes. The thermal model of power semiconductors has been created taking into account the parameters provided by the manufactures and employing multidimensional look-up tables in Plexim/PLECS environment. Consequently, the efficiency and losses distribution in relation to the function of the operating conditions have been estimated. Moreover, the voltage balancing issue of the rectifier has been addressed and a hardware solution which involves two SRBC has been analyzed. At the end of this study, the prototype of the rectifier and SRBC have been built. The single-phase rectifier is composed of Semitop4 power module and the SRBC is accomplished by Semitop3 60A-600V power module (manufacturer Semikron®). The rectifier control strategy for the regulation of both DC-bus voltage and the input sinusoidal current has been successfully implemented using a graphical programming environment called LabVIEW. The tuning procedure of the control loops is based on the achieved large and small signal mathematical modelling of the converter. The rectifier and PMSG have been controlled by the proper control platform, whose board is named PED-Board, realized thanks to a collaboration between E.D. Elettronica Dedicata S.r.l. and Roma Tre University.

The converter prototype coupled to the PMSG has been widely tested at variable rotation speed and constant torque. Achieved results have been compared with simulation results in order to prove the validity of the performed comparison. Results have really shown a good accordance between experimental and simulation results, thus validating the theoretical analysis of the rectifier.

Afterwards, the 3Φ5L E-Type Rectifier has been used in BTB configuration with a 3Φ5L E-Type Inverter. Then, the analysis of the 3Φ5L E-Type Back-to-Back Converter has been performed. The investigation has been extended to a new 3Φ5L E-Type BTB power converter as a new solution for extreme efficiency and power density. In order to obtain a great improvement from the switches voltage rating point of view, a small modification in the 5L E-Type BTB Converter has

been done. The advantages of the new 3Φ5L E-Type Back-to-Back topology over the previous 3Φ5L E-Type Back-to-Back configuration can be highlighted as follows:

- the voltage ratings of the power semiconductors are lower,
- the commutation loop and current path are smaller.

The selection process of power semiconductors of the proposed N3Φ5L E-Type BTB Converter has been also addressed. The analytical equations of the duty cycles, AVG and RMS current for each power device have been obtained. The origin of the losses mechanism of the power semiconductors has been described in details. The concept of the interleaving converter using an ICT has been then explained. The design and selection of passive components, such as the input filter, output filter and DC-bus capacitors, have been described by a proper step-by-step procedure. The use of the two-cell interleaved topology offers advantages as the reduction of size, losses and cost of the input and output filters, as well as reduction of current stress of the DC-bus capacitors, enabling a better utilization of the power semiconductors. Finally, using the AVG and RMS analytical equations previously obtained, the conduction and switching losses of the N3Φ5L E-Type BTB Converter have been fully addressed. An appropriate design of the N3Φ5L E-Type BTB Converter is of utmost importance and practical interest to evaluate the converter conduction and switching power losses. At the end, thermal management of the N3Φ5L E-Type BTB Converter has been discussed. According to the preliminary analysis and design, the targets on efficiency and power density are met. Taking into account suitable options in managing the heatsink temperature and the switching frequency, it seems possible to improve the theoretical peak efficiency above 98.30%.

Finally, the control strategy of the N3Φ5L E-Type BTB Converter has been implemented in LabVIEW environment. Then, in order to verify the control strategy effectiveness and performance, the N3Φ5L E-Type BTB Converter has been realized in NI Multisim environment and the co-simulation between NI

Multisim and LabVIEW has been performed. Co-simulation results show the correct functioning of the implemented strategy and the targets on the THD_v, THD_i and a short circuit capability equal to three times nominal current for 60 ms are met.

LIST OF FIGURES

LIST OF TABLES

REFERENCES

[1] D. C. Prince, "Mercury arc rectifier phenomena," in Journal of the A.I.E.E., vol. 46, no. 7, pp. 667-674, July 1927.

[2] R. S. Alishah, S. H. Hosseini, E. Babaei, and M. Sabahi, "Optimization Assessment of a New Extended Multilevel Converter Topology," *IEEE Trans. Ind. Electron.*, vol. PP, no. 99, pp. 1–1, 2017,

[3] S. Rivera, B. Wu, R. Lizana, S. Kouro, M. Perez, and J. Rodriguez, "Modular multilevel converter for large-scale multistring photovoltaic energy conversion system," in *Energy Conversion Congress and Exposition (ECCE), 2013 IEEE*, 2013, pp. 1941–1946.

[4] Y. Kashihara and J. i Itoh, "The performance of the multilevel converter topologies for PV inverter," in *2012 7th International Conference on Integrated Power Electronics Systems (CIPS)*, 2012, pp. 1–6.

[5] N.-Y. Dai, M.-C. Wong, and Y.-D. Han, "Application of a three-level NPC inverter as a three-phase four-wire power quality compensator by generalized 3DSVM," *IEEE Trans. Power Electron.*, vol. 21, no. 2, pp. 440–449, Mar. 2006.

[6] N. Bel Haj Youssef and K. Al-Haddad, "Experimental Implementation of a New Quasi-Linear Control Technique on a 1.5 kW Three-Phase Boost-Type Vienna Rectifier," in *Industrial Electronics, 2007. ISIE 2007. IEEE International Symposium on*, 2007, pp. 497–502.

[7] F. Blaabjerg, M. Liserre, and K. Ma, "Power Electronics Converters for Wind Turbine Systems," *IEEE Trans. Ind. Appl.*, vol. 48, no. 2, pp. 708–719, Mar. 2012.

[8] K. Ma and F. Blaabjerg, "Multilevel converters for 10 MW Wind Turbines," in *Proceedings of the 2011 14th European Conference on Power Electronics and Applications*, 2011, pp. 1–10.

[9] F. Merahi, S. Mekhilef, and E. M. Berkouk, "DC-voltage regulation of a five levels neutral point clamped cascaded converter for wind energy conversion system," in *2014 International Power Electronics Conference (IPEC-Hiroshima 2014 - ECCE ASIA)*, 2014, pp. 560–566.

[10] F. Crescimbini, A. Lidozzi, G. L. Calzo, and L. Solero, "High-Speed Electric Drive for Exhaust Gas Energy Recovery Applications," *IEEE Trans. Ind. Electron.*, vol. 61, no. 6, pp. 2998–3011, Jun. 2014.

[11] F. Crescimbini, A. Lidozzi, and L. Solero, "High-Speed Generator and Multilevel Converter for Energy Recovery in Automotive Systems," *IEEE Trans. Ind. Electron.*, vol. 59, no. 6, pp. 2678–2688, Jun. 2012.

[12] P. J. Grbović, F. Crescimbini, A. Lidozzi, and L. Solero, "Multi-level converters for low voltage high current applications: Issues, challenges and limitations," in *2014 16th International Power Electronics and Motion Control Conference and Exposition*, 2014, pp. 737–744.

[13] C. Bassi, A. Tessarolo, R. Menis, and G. Sulligoi, "Analysis of different system design solutions for a high-power ship propulsion synchronous motor drive with multiple PWM converters," in *Electrical Systems for Aircraft, Railway and Ship Propulsion*, 2010, pp. 1–6.

[14] M. D. Benedetto, A. Lidozzi, L. Solero, F. Crescimbini, and P. J. Grbovic, "Five-level back to back E-Type converter for high speed gen-set applications," in *IECON 2016 - 42nd Annual Conference of the IEEE Industrial Electronics Society*, 2016, pp. 3409–3414.

[15] M. Alsolami, K. A. Potty, and J. Wang, "A Gallium-Nitride-Device-Based Switched Capacitor Multiport Multilevel Converter for UPS Applications," *IEEE Trans. Power Electron.*, vol. 32, no. 9, pp. 6853–6862, Sep. 2017.

[16] L. G. Franquelo, J. Rodriguez, J. I. Leon, S. Kouro, R. Portillo, and M. A. M. Prats, "The age of multilevel converters arrives," *IEEE Ind. Electron. Mag.*, vol. 2, no. 2, pp. 28–39, Jun. 2008.

[17] B. Burger and D. Kranzer, "Extreme high efficiency PV-power converters," in *2009 13th European Conference on Power Electronics and Applications*, 2009, pp. 1–13.

[18] F. Merahi, S. Mekhilef, E. M. Berkouk, and A. Taallah, "DC-voltage regulation of a five levels neutral point clamped cascaded converter for wind energy conversion system," in *Power Electronics for Distributed Generation Systems (PEDG), 2013 4th IEEE International Symposium on*, 2013, pp. 1–7.

[19] R. G. A. Cacau, R. P. T. Bascopé, J. A. F. Neto, and G. V. T. Bascopé, "Five-level T-type inverter based on multi-state switching cell," in *Industry Applications (INDUSCON), 2012 10th IEEE/IAS International Conference on*, 2012, pp. 1–8.

[20] C. A. Rojas, S. Kouro, D. Edwards, B. Wu, and S. Rivera, "Five-level H-bridge NPC central photovoltaic inverter with open-end winding grid connection," in *IECON 2014 - 40th Annual Conference of the IEEE Industrial Electronics Society*, 2014, pp. 4622–4627.

[21] J. R. Rodriguez, J. W. Dixon, J. R. Espinoza, J. Pontt, and P. Lezana, "PWM regenerative rectifiers: state of the art," *IEEE Trans. Ind. Electron.*, vol. 52, no. 1, pp. 5–22, Feb. 2005.

[22] J. Rodriguez, J.-S. Lai, and F. Z. Peng, "Multilevel inverters: a survey of topologies, controls, and applications," *IEEE Trans. Ind. Electron.*, vol. 49, no. 4, pp. 724–738, Aug. 2002.

[23] M. Salehifar, V. Dargahi, and A. Shoulaie, "A series active power filter using a flying capacitor multicell inverter," in *Power Electronic Drive Systems Technologies Conference (PEDSTC), 2010 1st*, 2010, pp. 191–195.

[24] P. Lezana and J. Rodriguez, "Mixed Multicell Cascaded Multilevel Inverter," in *2007 IEEE International Symposium on Industrial Electronics*, 2007, pp. 509–514.

[25] C. Anandababu and B. G. Fernandes, "A novel neutral point clamped transformerless inverter for grid-connected photovoltaic system," in *Industrial Electronics Society, IECON 2013 - 39th Annual Conference of the IEEE*, 2013, pp. 6962–6967.

[26] N. Maheshkumar, V. Maheskumar, and M. Divya, "The new topology in Flying Capacitor Multilevel Inverter," in *Computer Communication and Informatics (ICCCI), 2013 International Conference on*, 2013, pp. 1–6.

[27] R. Naderi and K. Smedley, "A new hybrid active neutral point clamped flying capacitor multilevel inverter," in *2015 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2015, pp. 794–798.

[28] D. Sun, B. Ge, F. Z. Peng, A. R. Haitham, D. Bi, and Y. Liu, "A new grid-connected PV system based on cascaded H-bridge quasi-Z source inverter," in *Industrial Electronics (ISIE), 2012 IEEE International Symposium on*, 2012, pp. 951–956.

[29] V. F. Pires, D. Foito, and J. F. Martins, "Multilevel power converter with a dual T-type three level inverter for energy storage," in *2014 International Conference on Optimization of Electrical and Electronic Equipment (OPTIM)*, 2014, pp. 1091–1096.

[30] J. M. Carrasco *et al.*, "Power-Electronic Systems for the Grid Integration of Renewable Energy Sources: A Survey," *IEEE Trans. Ind. Electron.*, vol. 53, no. 4, pp. 1002–1016, Jun. 2006.

[31] B. Xiao, L. Hang, J. Mei, C. Riley, L. M. Tolbert, and B. Ozpineci, "Modular Cascaded H-Bridge Multilevel PV Inverter With Distributed MPPT for Grid-Connected Applications," *IEEE Trans. Ind. Appl.*, vol. 51, no. 2, pp. 1722–1731, Mar. 2015.

[32] B. Singh, B. N. Singh, A. Chandra, K. Al-Haddad, A. Pandey, and D. P. Kothari, "A review of three-phase improved power quality AC-DC converters," *IEEE Trans. Ind. Electron.*, vol. 51, no. 3, pp. 641–660, Jun. 2004.

[33] J. W. Kolar and T. Friedli, "The essence of three-phase PFC rectifier systems," in *Telecommunications Energy Conference (INTELEC), 2011 IEEE 33rd International*, 2011, pp. 1–27.

[34] T. Friedli, M. Hartmann, and J. W. Kolar, "The Essence of Three-Phase PFC Rectifier Systems #x2014;Part II," *Power Electron. IEEE Trans. On*, vol. 29, no. 2, pp. 543–560, Feb. 2014.

[35] H. Kanaan and K. Al-Haddad, "Small-signal averaged model and simple control of a high-power-factor three-phase/switch/level fixed-frequency PWM rectifier for high-power telecommunications," in *Telecommunications Energy Conference, 2004. INTELEC 2004. 26th Annual International*, 2004, pp. 449–456.

[36] N. Bel Haj Youssef, K. Al-Haddad, and H. Y. Kanaan, "Implementation of a New Linear Control Technique Based on Experimentally Validated Small-Signal Model of Three-Phase Three-Level Boost-Type Vienna Rectifier," *Ind. Electron. IEEE Trans. On*, vol. 55, no. 4, pp. 1666–1676, Apr. 2008.

[37] A. H. Bhat and P. Agarwal, "An Improved Performance Three-Phase Neutral-Point Clamped Rectifier with Simplified Control Scheme," in *2006 IEEE International Symposium on Industrial Electronics*, 2006, vol. 2, pp. 1019–1024.

[38] T. Thangavelu, P. Shanmugam, and K. Raj, "Modelling and control of VIENNA rectifier a single phase approach," *IET Power Electron.*, vol. 8, no. 12, pp. 2471–2482, 2015.

[39] P. Grbovic, A. Lidozzi, L. Solero, and F. Crescimbini, "Five-Level Unidirectional T-Rectifier for High-Speed Gen-Set Applications," *IEEE Trans. Ind. Appl.*, vol. 52, no. 2, pp. 1642–1651, Mar. 2016.

[40] P. Grbovic, A. Lidozzi, L. Solero, and F. Crescimbini, "Performance evaluation for the five-level unidirectional T-rectifier in high-speed electric generating units," in *Energy Conversion Congress and Exposition (ECCE), 2015 IEEE*, 2015, pp. 5110–5116.

[41] A. Binder and T. Schneider, "High-speed inverter-fed AC drives," in Electrical Machines and Power Electronics, 2007. ACEMP '07. International Aegean Conference on, 2007, pp. 9–16.

[42] P. J. Grbovic, P. Delarue, and P. Le Moigne, "A Novel Three-Phase Diode Boost Rectifier Using Hybrid Half-DC-Bus-Voltage Rated Boost Converter," *IEEE Trans. Ind. Electron.*, vol. 58, no. 4, pp. 1316–1329, Apr. 2011.

[43] T. B. Soeiro and J. W. Kolar, "Analysis of High-Efficiency Three-Phase Two- and Three-Level Unidirectional Hybrid Rectifiers," *IEEE Trans. Ind. Electron.*, vol. 60, no. 9, pp. 3589–3601, Sep. 2013.

[44] R. H. Osman, "A medium-voltage drive utilizing series-cell multilevel topology for outstanding power quality," in *Industry Applications Conference, 1999. Thirty-Fourth IAS Annual Meeting. Conference Record of the 1999 IEEE*, 1999, vol. 4, pp. 2662–2669 vol.4.

[45] P. Kollensperger, C. Meyer, U. Schwarzer, S. Schroder, and R. W. D. Doncker, "High-power converter systems for high-speed generators," in *Power Electronics and Applications, 2005 European Conference on*, 2005, p. 9 pp.-P.9.

[46] L. M. Tolbert, F. Z. Peng, and T. G. Habetler, "Multilevel converters for large electric drives," *IEEE Trans. Ind. Appl.*, vol. 35, no. 1, pp. 36–44, Jan. 1999.

[47] M. Malinowski, K. Gopakumar, J. Rodriguez, and M. A. Perez, "A Survey on Cascaded Multilevel Inverters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 7, pp. 2197–2206, Jul. 2010.

[48] J. Li, A. Huang, S. Bhattacharya, and S. Lukic, "ETO light multilevel converters for large electric vehicle and hybrid electric vehicle drives," in *Vehicle Power and Propulsion Conference, 2009. VPPC '09. IEEE*, 2009, pp. 1455–1460.

[49] X. Kou, K. A. Corzine, and Y. L. Familiant, "A unique fault-tolerant design for flying capacitor multilevel inverter," *IEEE Trans. Power Electron.*, vol. 19, no. 4, pp. 979–987, Jul. 2004.

[50] A. Chen, C. Zhang, X. He, and N. Cui, "Fault-tolerant design for flying capacitor multilevel inverters," in *Power Electronics and Motion Control Conference, 2009. IPEMC '09. IEEE 6th International*, 2009, pp. 1460–1464.

[51] M. Biberoglu, K. Ince, and F. Karaosmanoglu, "Design of fault-tolerant cascaded H-Bridge multilevel inverter with output-side transformers using bidirectional switches," in *2015 International Conference on Renewable Energy Research and Applications (ICRERA)*, 2015, pp. 98–103.

[52] M. Díaz, R. Cardenas, B. M. Espinoza, A. Mora, and F. Rojas, "A novel LVRT control strategy for Modular Multilevel Matrix Converter based high-power Wind Energy Conversion Systems," in *Ecological Vehicles and Renewable Energies (EVER), 2015 Tenth International Conference on*, 2015, pp. 1–11.

[53] F. H. Khan, L. M. Tolbert, and W. E. Webb, "Hybrid Electric Vehicle Power Management Solutions Based on Isolated and Nonisolated Configurations of Multilevel Modular Capacitor-Clamped Converter," *IEEE Trans. Ind. Electron.*, vol. 56, no. 8, pp. 3079–3095, Aug. 2009.

[54] M. D. Benedetto, A. Lidozzi, L. Solero, P. J. Grbovic, and S. Bifaretti, "ISOP DC-DC converters equipped 5-level unidirectional T-Rectifier for aerospace applications," in *Energy Conversion Congress and Exposition (ECCE), 2015 IEEE*, 2015, pp. 1694–1700.

[55] M. Sadikin, T. Senjyu, and A. Yona, "DC-DC type high-frequency link DC for improved power quality of cascaded multilevel inverter," in *Renewable Energy Research and Applications (ICRERA), 2012 International Conference on*, 2012, pp. 1–5.

[56] R. Li, G. P. Adam, D. Holliday, J. E. Fletcher, and B. W. Williams, "Hybrid Cascaded Modular Multilevel Converter With DC Fault Ride-Through Capability for the HVDC Transmission System," *IEEE Trans. Power Deliv.*, vol. 30, no. 4, pp. 1853–1862, Aug. 2015.

[57] D. Montesinos-Miracle, M. Massot-Campos, J. Bergas-Jane, S. Galceran-Arellano, and A. Rufer, "Design and Control of a Modular Multilevel DC/DC Converter for Regenerative Applications," *IEEE Trans. Power Electron.*, vol. 28, no. 8, pp. 3970–3979, Aug. 2013.

[58] Y. K. Wu; J. H. Lin; H. J. Lin, "Standards and Guidelines for Grid-connected Photovoltaic Generation Systems: a Review and Comparison," in IEEE Transactions on Industry Applications, vol.PP, no.99, pp.1-1

[59] J. W. Kolar, T. Friedli, J. Rodriguez, and P. W. Wheeler, "Review of Three-Phase PWM AC-AC Converter Topologies," *IEEE Trans. Ind. Electron.*, vol. 58, no. 11, pp. 4988–5006, Nov. 2011.

[60] T. Friedli, J. W. Kolar, J. Rodriguez, and P. W. Wheeler, "Comparative Evaluation of Three-Phase AC-AC Matrix Converter and Voltage DC-Link Back-to-Back Converter Systems," *IEEE Trans. Ind. Electron.*, vol. 59, no. 12, pp. 4487–4510, Dec. 2012.

[61] J. Rodriguez *et al.*, "Multilevel Converters: An Enabling Technology for High-Power Applications," *Proc. IEEE*, vol. 97, no. 11, pp. 1786–1817, Nov. 2009.

[62] K. Niyomsatian, S. Samermurn, S. Suwankawin, and S. Sangwongwanich, "Novel topologies for three-level back-to-back converters based on matrix converter theory," in *IECON 2012 - 38th Annual Conference on IEEE Industrial Electronics Society*, 2012, pp. 6099–6104.

[63] L. M. Grzesiak and J. Tomasik, "DC Link Balancing Method in Back-to-Back UPS System with Multi-Level Converters," in *2006 IEEE International Symposium on Industrial Electronics*, 2006, vol. 2, pp. 908–913.

[64] Z. Zhao, J. Zhao, and C. Huang, "An Improved Capacitor Voltage-Balancing Method for Five-Level Diode-Clamped Converters With High Modulation Index and High Power Factor," *IEEE Trans. Power Electron.*, vol. 31, no. 4, pp. 3189–3202, Apr. 2016.

[65] L. M. Grzesiak and J. G. Tomasik, "Autonomous power generating system with generic n-level back-to-back converters," in *2007 International Power Engineering Conference (IPEC 2007)*, 2007, pp. 245–250.

[66] Z. Pan, F. Z. Peng, V. Stefanovic, and M. Leuthen, "A diode-clamped multilevel converter with reduced number of clamping diodes," in *Applied Power Electronics Conference and Exposition, 2004. APEC '04. Nineteenth Annual IEEE*, 2004, vol. 2, pp. 820–824 vol.2.

[67] M. Schweizer and J. W. Kolar, "Design and Implementation of a Highly Efficient Three-Level T-Type Converter for Low-Voltage Applications," *IEEE Trans. Power Electron.*, vol. 28, no. 2, pp. 899–907, Feb. 2013.

[68] M. Schweizer and J. W. Kolar, "High efficiency drive system with 3-level T-type inverter," in *Power Electronics and Applications (EPE 2011), Proceedings of the 2011-14th European Conference on*, 2011, pp. 1–10.

[69] M. Schweizer, T. Friedli, and J. W. Kolar, "Comparative Evaluation of Advanced Three-Phase Three-Level Inverter/Converter Topologies Against Two-Level Systems," *IEEE Trans. Ind. Electron.*, vol. 60, no. 12, pp. 5515–5527, Dec. 2013.

[70] R. P. T. Bascopé, J. A. F. Neto, and G. V. T. Bascopé, "Multi-state commutation cells to increase current capacity of multi-level inverters," in *2011 IEEE 33rd International Telecommunications Energy Conference (INTELEC)*, 2011, pp. 1–9.

[71] W. Wu, F. Wang, and Y. Wang, "A novel efficient T type Three level Neutral-Point-Clamped inverter for renewable energy system," in *2014 International Power Electronics Conference (IPEC-Hiroshima 2014 - ECCE ASIA)*, 2014, pp. 470–474.

[72] K. Fujii, T. Kikuchi, H. Koubayashi, and K. Yoda, "1-MW advanced T-type NPC converters for solar power generation system," in *Power Electronics and Applications (EPE), 2013 15th European Conference on*, 2013, pp. 1–10.

[73] G. Karthick and E. Prasanna Kumar, "Design of Five Level T-Type Neutral-Point Clamped Inverter Using Cool-MOSFET for Solar Energy System," *Int. J. Electr. Electron. Res. IS*, vol. 3, no. 2, pp. 586–593, Jun. 2015.

[74] R. Guedouani, B. Fiala, E. M. Berkouk, and M. S. Boucherit, "Modelling and control of three-phase PWM voltage source rectifiers- five-level NPC voltage source inverter-induction machine system," in *Control Automation (MED), 2010 18th Mediterranean Conference on*, 2010, pp. 533–538.

[75] O. Bouhali, N. Rizoug, T. Mesbahi, and B. Francois, "Modeling and control of the three-phase NPC multilevel converter using an equivalent matrix structure," in *Power Electronics, Machines and Drives (PEMD 2014), 7th IET International Conference on*, 2014, pp. 1–6.

[76] F. Z. Peng, "A generalized multilevel inverter topology with self voltage balancing," *IEEE Trans. Ind. Appl.*, vol. 37, no. 2, pp. 611–618, Mar. 2001.

[77] F. Kieferndorf, M. Basler, L. A. Serpa, J. H. Fabian, A. Coccia, and G. A. Scheuer, "A new medium voltage drive system based on ANPC-5L technology," in *Industrial Technology (ICIT), 2010 IEEE International Conference on*, 2010, pp. 643–649.

[78] J. Meili, S. Ponnaluri, L. Serpa, P. K. Steimer, and J. W. Kolar, "Optimized Pulse Patterns for the 5-Level ANPC Converter for High Speed High Power Applications," in *IECON 2006 - 32nd Annual Conference on IEEE Industrial Electronics*, 2006, pp. 2587–2592.

[79] S. R. Pulikanti and V. G. Agelidis, "Hybrid Flying-Capacitor-Based Active-Neutral-Point-Clamped Five-Level Converter Operated With SHE-PWM," *IEEE Trans. Ind. Electron.*, vol. 58, no. 10, pp. 4643–4653, Oct. 2011.

[80] C. M. Wu, W. H. Lau, and H. Chung, "A five-level neutral-point-clamped H-bridge PWM inverter with superior harmonics suppression: a theoretical analysis," in *Circuits and Systems, 1999. ISCAS '99. Proceedings of the 1999 IEEE International Symposium on*, 1999, vol. 5, pp. 198–201 vol.5.

[81] Z. Cheng and B. Wu, "A Novel Switching Sequence Design for Five-Level NPC/H-Bridge Inverters With Improved Output Voltage Spectrum and Minimized Device Switching Frequency," *IEEE Trans. Power Electron.*, vol. 22, no. 6, pp. 2138–2145, Nov. 2007.

[82] A. M. Y. M. Ghias, J. Pou, M. Ciobotaru, and V. G. Agelidis, "Voltage balancing of a five-level flying capacitor converter using optimum switching transitions," in *IECON 2012 - 38th Annual Conference on IEEE Industrial Electronics Society*, 2012, pp. 5006–5012.

[83] S. Thielemans, A. Ruderman, B. Reznikov, and J. Melkebeek, "Improved Natural Balancing With Modified Phase-Shifted PWM for Single-Leg Five-Level Flying-Capacitor Converters," *IEEE Trans. Power Electron.*, vol. 27, no. 4, pp. 1658–1667, Apr. 2012.

[84] M. Narimani, B. Wu, Z. Cheng, and N. R. Zargari, "A New Nested Neutral Point-Clamped (NNPC) Converter for Medium-Voltage (MV) Power Conversion," *IEEE Trans. Power Electron.*, vol. 29, no. 12, pp. 6375–6382, Dec. 2014.

[85] K. Tian, B. Wu, M. Narimani, D. (Xu, Z. Cheng, and N. R. Zargari, "A Capacitor Voltage-Balancing Method for Nested Neutral Point Clamped (NNPC) Inverter," *IEEE Trans. Power Electron.*, vol. 31, no. 3, pp. 2575–2583, Mar. 2016.

[86] M. Narimani, B. Wu, and N. R. Zargari, "A Novel Five-Level Voltage Source Inverter With Sinusoidal Pulse Width Modulator for Medium-Voltage Applications," *IEEE Trans. Power Electron.*, vol. 31, no. 3, pp. 1959–1967, Mar. 2016.

[87] S. K. Giri, S. Chakrabarti, S. Banerjee, and C. Chakraborty, "A Carrier-Based PWM Scheme for Neutral Point Voltage Balancing in Three-Level Inverter Extending to Full Power Factor Range," *IEEE Trans. Ind. Electron.*, vol. 64, no. 3, pp. 1873–1883, Mar. 2017.

[88] P. Fazio, G. Maragliano, M. Marchesoni, and L. Vaccaro, "A new capacitor balancing technique in Diode-Clamped Multilevel Converters with Active Front End for extended operation range," in *Power Electronics and Applications (EPE 2011), Proceedings of the 2011-14th European Conference on*, 2011, pp. 1–10.

[89] M. Zygmanowski, J. Michalak, and B. Grzesik, "DC-link voltage balancing method for a hybrid asymmetric multilevel converter," in *Power Electronics and Applications (EPE), 2013 15th European Conference on*, 2013, pp. 1–10.

[90] S. Mekhilef and M. N. A. Kadir, "Voltage Control of Three-Stage Hybrid Multilevel Inverter Using Vector Transformation," *IEEE Trans. Power Electron.*, vol. 25, no. 10, pp. 2599–2606, Oct. 2010.

[91] Y. Jiao, F. C. Lee, and S. Lu, "Space vector modulation for 3-level NPC converter with neutral voltage balancing and switching loss/noise reduction," in *2014 IEEE Applied Power Electronics Conference and Exposition - APEC 2014*, 2014, pp. 1780–1787.

[92] R. Stala, "Application of Balancing Circuit for DC-Link Voltages Balance in a Single-Phase Diode-Clamped Inverter With Two Three-Level Legs," *IEEE Trans. Ind. Electron.*, vol. 58, no. 9, pp. 4185–4195, Sep. 2011.

[93] L. M. Grzesiak and J. G. Tomasik, "Novel DC link balancing scheme in generic n-level back-to-back converter system," in *2007 7th Internatonal Conference on Power Electronics*, 2007, pp. 1044–1049.

[94] J. C. Rosas-Caro, J. M. Ramirez, and A. Valderrabano, "Voltage balancing in DC/DC multilevel boost converters," in *2008 40th North American Power Symposium*, 2008, pp. 1–7.

[95] K. Sano and H. Fujita, "Voltage-Balancing Circuit Based on a Resonant Switched-Capacitor Converter for Multilevel Inverters," *IEEE Trans. Ind. Appl.*, vol. 44, no. 6, pp. 1768–1776, Nov. 2008.

[96] T. V. Dinh *et al.*, "Modeling and characterization of bond-wire arrays for distributed Chip-Package-PCB Co-design," in *2015 European Microwave Conference (EuMC)*, 2015, pp. 1022–1025.

[97] B. Gutsmann, P. Mourick, and D. Silber, "Exact inductive parasitic extraction for analysis of IGBT parallel switching including DCB-backside eddy currents," in *2000 IEEE 31st Annual Power Electronics Specialists Conference. Conference Proceedings (Cat. No.00CH37018)*, 2000, vol. 3, pp. 1291–1295 vol.3.

[98] U. Divan Deepakraj M.(San Jose, CA, US), Kandula, Rajendra Prasad (Atlanta, GA, US), Prasai, Anish (San Jose, CA, "Power flow controller with a fractionally rated back-to-back converter," 9281756, Mar-2016.

[99] M. Berglund and B. \AAKESSON, *Transformer configuration for a back-to-back converter*. Google Patents, 2013.

[100] U. Lai Jih-sheng (Blacksburg, VA, US), Mansoor, Arshad (Oak Ridge, TN, US), Maitra, Arindam (Knoxville, TN, US), Goodman, Frank (Palo Alto, CA, "Multilevel converter based intelligent universal transformer," 7050311, May-2006.

[101] K. Hong Myoung-shin (Kyunggi, KR), Jang, Donghwan (Kyunggi, KR), Roh, Whanjin (Seoul, KR), Park, Jongho (Seoul, KR), Cho, Soonnam (Kyunggi, "Uninterruptible power supply for the backup of AC-power supply," 7259475, Aug-2007.
[102] U. Liu Jingbo (Grafton, WI, US), Nondahl, Thomas (Greenfield, WI, "Power stage precharging and dynamic braking apparatus for multilevel inverter," 9083274, Jul-2015.
[103] D. Hjort Thomas Enné (Vejle, DK), Pedersen, Michael (Roedding, "Method and apparatus for providing uninterruptible power," 7939968, May-2011.
[104] J. Yamamoto Yuushin (Tokyo, "Parallel operation method for an uninterruptible power supply apparatus," 7061141, Jun-2006.
[105] B. Torrico, and V. Grover, "Five-level pv inverter based on a multi-state switching cell," 20160118910, Apr-2016.
[106] M. Narimani, B. Wu, Z. Cheng, and N. R. Zargari, "Multilevel voltage source converters and systems," 9083230, Jul-2015.
[107] C. He Bo (Shenzhen, CN), Fu, Dianbo (Plano, TX, US), Lv, Yihang (Shenzhen, "Five-Level Power Converter, and Control Method and Control Apparatus for the Same," 20110299312, Nov-2014.
[108] U. Fu Dianbo (Plano, TX, "Multilevel hybrid inverter and operating method," 9190934, Nov-2015.
[109] M. Hochgraf Clark Glenn (Levonia, "High voltage modular inverter," 6072707, Jun-2000.
[110] H. Wang and Y. Liu, "Five-level topology units and inverter thereof," 20150333522, Nov-2015.
[111] I. Yoscovich, T. Glovinsky, G. Sella, and Y. Galin, "Multi-level inverter with flying capacitor topology," 9318974, Apr-2016.
[112] P. Rodriquez, B. M. Dias, A. R. S. Muñoz, and M. S. Busquets, *Multilevel-clamped multilevel converters (MLC2)*. Google Patents, 2013.
[113] J. Liu, T. Nondahl, Z. Cheng, and N. Zargari, *Cascaded H-bridge (CHB) inverter level shift PWM with rotation*. Google Patents, 2013.
[114] J. P. Lyons, V. Vlatkovic, P. M. Espelage, A. A. M. Esser, Y. Zhao, and F. F. Wang, *Five level high power motor drive converter and control system*. Google Patents, 2000.
[115] M. F. Aiello, P. W. Hammond, and M. Rastogi, *Modular multi-level adjustable supply with series connected active inputs*. Google Patents, 2001.
[116] K. A. Corzine, *Cascaded multi-level H-bridge drive*. Google Patents, 2004.
[117] T. Tanaka and R. Nakagawa, *Three-level power converting apparatus*. Google Patents, 2011.
[118] F. Flury Guy (Balschwiller, "3N-4-level voltage inverter," 8288896, Oct-2012.
[119] D. Grbovic Petar Jovan (Ismaning, DE), Giroux, Mathieu (Munich, "Neutral point clamped (NPC) power converter fault protection system," 8625316, Jan-2014.
[120] F. Capitaneanu Stefan (Mousseaux Neuville, FR), Malrait, Francois (Jouy sur Eure, FR), Rouchon, Pierre (Meudon, "Method of controlling an NPC inverter operating in overmodulation," 8564994, Oct-2013.
[121] A. Yoo, "Multi-level medium-voltage inverter," 9270222, Feb-2016.
[122] F. Karraker Douglas W.(Muskego, WI, US), Gokhale, Kalyan P.(New Berlin, WI, US), Jussila, Matti T.(Vantaa, "Soft switching three-level inverter," 20110299312, Dec-2011.
[123] H. M. Yun, *Multilevel inverter*. Google Patents, 2012.
[124] I. Yoscovitch, *Multi-level inverter*. Google Patents, 2016.

[125] U. Teo Koon Hoo (Lexington, MA, US), Deng, Yi (Atlanta, GA, "DC-link voltage balancing control for multilevel inverters," 8934276, Jan-2015.

[126] J. T. Tan, Q. H. Zhu, C. Z. MA, D. G. YI, W. Y. Tsai, and J. P. Ying, *Three-level AC generating circuit and control method thereof*. Google Patents, 2010.

[127] S. POTHARAJU, Solar module having a back plane integrated inverter. Google Patents, 2014.

[128] D. Martini, M. Valiani, and S. Soldani, *Multi-Level DC/AC Converter*. Google Patents, 2013.

[129] D. Shen Jie (Ingolstadt, DE), Schroeder, Stefan (Munich, DE), Roesner, Robert (Unterfoehring, "DC-link voltage balancing system and method for multilevel converters," 8441820, May-2013.

[130] U. Mihalache Liviu (Evans City, PA, "Pulse width modulation control for a multilevel converter," 9184673, Nov-2015.

[131] R. Lai, F. Wang, R. Burgos, D. Boroyevich, D. Jiang, and D. Zhang, "Average Modeling and Control Design for VIENNA-Type Rectifiers Considering the DC-Link Voltage Balance," *IEEE Trans. Power Electron.*, vol. 24, no. 11, pp. 2509–2522, Nov. 2009.

[132] S. Gataric and N. R. Garrigan, "Modeling and design of three-phase systems using complex transfer functions," in *Power Electronics Specialists Conference, 1999. PESC 99. 30th Annual IEEE*, 1999, vol. 2, pp. 691–697 vol.2.

[133] P. Van den Hof, "Identification of experimental models for control design," in *Instrumentation and Measurement Technology Conference, 2001. IMTC 2001. Proceedings of the 18th IEEE*, 2001, vol. 2, pp. 1155–1162 vol.2.

[134] R. Middlebrook and S. Cuk, "A general unified approach to modelling switching-converter power stages," in *Power Electronics Specialists Conference, 1976 IEEE*, 1976, pp. 18–34.

[135] S.-Y. Ou, C.-Y. Tang, and Z.-J. Chen, "Design and Implementation of a ZCS-PWM Half-Bridge Boost Rectifier With Output Voltage Balance Control," *Ind. Electron. IEEE Trans. On*, vol. 59, no. 12, pp. 4646–4656, Dec. 2012.

[136] B. Choi, S.-S. Hong, and H. Park, "Modeling and small-signal analysis of controlled on-time boost power-factor-correction circuit," *Ind. Electron. IEEE Trans. On*, vol. 48, no. 1, pp. 136–142, Feb. 2001.

[137] A. Lidozzi, L. Solero, and F. Crescimbini, "Adaptive Direct-Tuning Control for Variable-Speed Diesel-Electric Generating Units," *IEEE Trans. Ind. Electron.*, vol. 59, no. 5, pp. 2126–2134, May 2012.

[138] N. B. H. Youssef, F. Fnaiech, and K. Al-Haddad, "Small signal modeling and control design of a three-phase AC/DC Vienna converter," in *Industrial Electronics Society, 2003. IECON '03. The 29th Annual Conference of the IEEE*, 2003, vol. 1, pp. 656–661 vol.1.

[139] T. Thangavelu, P. Shanmugam, and K. Raj, "Modelling and control of VIENNA rectifier a single phase approach," IET Power Electron., vol. 8, no. 12, pp. 2471–2482, 2015.

[140] M. D. Benedetto, A. Lidozzi, L. Solero, F. Crescimbini and P. J. Grbovic, "Small-Signal Model of the Five-Level Unidirectional T-Rectifier," in IEEE Transactions on Power Electronics, vol. 32, no. 7, pp. 5741-5751, July 2017.

[141] N. B. Hadj-Youssef, K. Al-Haddad, H. Y. Kanaan, and F. Fnaiech, "Small-signal perturbation technique used for DSP-based identification of a three-phase three-level boost-type Vienna rectifier," *IET Electr. Power Appl.*, vol. 1, no. 2, pp. 199–208, 2007.

[142] N. Bel Haj Youssef, K. Al-Haddad, and H. Y. Kanaan, "Large-Signal Modeling and Steady-State Analysis of a 1.5-kW Three-Phase/Switch/Level (Vienna) Rectifier with Experimental Validation," *IEEE Trans. Ind. Electron.*, vol. 55, no. 3, pp. 1213–1224, 2008.

[143] R. S. Colby, T. A. Lipo, and D. W. Novotny, "A State Space Analysis of LCI Fed Synchronous Motor Drives in the Steady State," *IEEE Trans. Ind. Appl.*, vol. IA-21, no. 4, pp. 1016–1022, Jul. 1985.

[144] J. Mahdavi, A. Emaadi, M. D. Bellar, and M. Ehsani, "Analysis of power electronic converters using the generalized state-space averaging approach," *IEEE Trans. Circuits Syst. Fundam. Theory Appl.*, vol. 44, no. 8, pp. 767–770, Aug. 1997.

[145] C. Deml and P. Turkes, "Fast simulation technique for power electronic circuits with widely different time constants," *IEEE Trans. Ind. Appl.*, vol. 35, no. 3, pp. 657–662, May 1999.

[146] A. Yazdani and R. Iravani, "A Generalized State-Space Averaged Model of the Three-Level NPC Converter for Systematic DC-Voltage-Balancer and Current-Controller Design," *IEEE Trans. Power Deliv.*, vol. 20, no. 2, pp. 1105–1114, Apr. 2005.

[147] A. F. Witulski and R. W. Erickson, "Extension of state-space averaging to resonant switches and beyond," *IEEE Trans. Power Electron.*, vol. 5, no. 1, pp. 98–109, Jan. 1990.

[148] A. Davoudi, J. Jatskevich, and T. D. Rybel, "Numerical State-Space Average-Value Modeling of PWM DC-DC Converters Operating in DCM and CCM," *IEEE Trans. Power Electron.*, vol. 21, no. 4, pp. 1003–1012, Jul. 2006.

[149] A. Yazdani and R. Iravani, "Dynamic Model and Control of the NPC-Based Back-to-Back HVDC System," *IEEE Trans. Power Deliv.*, vol. 21, no. 1, pp. 414–424, Jan. 2006.

[150] A. Emadi, "Modeling and Analysis of Multiconverter DC Power Electronic Systems Using the Generalized State-Space Averaging Method," *IEEE Trans. Ind. Electron.*, vol. 51, no. 3, pp. 661–668, Jun. 2004.

[151] A. Emadi, "Modeling of Power Electronic Loads in AC Distribution Systems Using the Generalized State-Space Averaging Method," *IEEE Trans. Ind. Electron.*, vol. 51, no. 5, pp. 992–1000, Oct. 2004.

[152] M. D. Benedetto, A. Lidozzi, L. Solero, F. Crescimbini, and P. J. Grbovic, "Low-Frequency State-Space Model for the Five-Level Unidirectional T-Rectifier," *IEEE Trans. Ind. Appl.*, vol. 53, no. 2, pp. 1127–1137, Mar. 2017.

[153] M. M. Bakran and H. G. Eckel, "Evolution of IGBT converters for mass transit applications," Conference Record of the 2000 IEEE Industry Applications Conference. Thirty-Fifth IAS Annual Meeting and World Conference on Industrial Applications of Electrical Energy (Cat. No.00CH37129), Rome, 2000, pp. 1930-1935 vol.3.

[154] A. Lidozzi, M. Di Benedetto, V. Sabatini, L. Solero and F. Crescimbini, "Towards LabVIEW and system on module for power electronics and drives control applications," IECON 2016 - 42nd Annual Conference of the IEEE Industrial Electronics Society, Florence, 2016, pp. 4995-5000.

[155] S. Vadhiraj, K. N. Swamy, and B. P. Divakar, "Generic SPWM technique for multilevel inverter," in *2013 IEEE PES Asia-Pacific Power and Energy Engineering Conference (APPEEC)*, 2013, pp. 1–5.

[156] A. K. Sadigh, V. Dargahi, and K. A. Corzine, "Analytical Determination of Conduction and Switching Power Losses in Flying-Capacitor-Based Active Neutral-Point-Clamped Multilevel Converter," *IEEE Trans. Power Electron.*, vol. 31, no. 8, pp. 5473–5494, Aug. 2016.

[157] P. J. Grbovic, *Ultra-capacitors in power conversion systems*. John Wiley & Sons Inc, 2013.

[158] M. Gerber, J. A. Ferreira, I. W. Hofsajer, and N. Seliger, "High density packaging of the passive components in an automotive DC/DC converter," *IEEE Trans. Power Electron.*, vol. 20, no. 2, pp. 268–275, Mar. 2005.

[159] T. Nussbaumer, K. Raggl, and J. W. Kolar, "Design Guidelines for Interleaved Single-Phase Boost PFC Circuits," *IEEE Trans. Ind. Electron.*, vol. 56, no. 7, pp. 2559–2573, Jul. 2009.

[160] M. G. Simões, C. L. Lute, A. N. Alsaleem, D. I. Brandao, and J. A. Pomilio, "Bidirectional floating interleaved buck-boost DC-DC converter applied to residential PV power systems," in *Power Systems Conference (PSC), 2015 Clemson University*, 2015, pp. 1–8.

[161] I. S. Mohamed, S. A. Zaid, M. F. Abu-Elyazeed and H. M. Elsayed, "Model predictive control-a simple and powerful method to control UPS inverter applications with output LC filter," 2013 Saudi International Electronics, Communications and Photonics Conference, Fira, 2013, pp. 1-6.

[162] N. Mukherjee and D. De, "Analysis and improvement of performance in LCL filter-based PWM rectifier/inverter application using hybrid damping approach," in IET Power Electronics, vol. 6, no. 2, pp. 309-325, Feb. 2013.

[163] F. Forest, T. A. Meynard, E. Labouré, B. Gelis, J. J. Huselstein, and J. C. Brandelero, "An Isolated Multicell Intercell Transformer Converter for Applications With a High Step-Up Ratio," IEEE Trans. Power Electron., vol. 28, no. 3, pp. 1107–1119, Mar. 2013.

[164] S. M. Sharkh, M. A. Abu-Sara, G. I. Orfanoudakis, and B. Hussain, "Design and Control of a Grid-Connected Interleaved Inverter," in Power Electronic Converters for Microgrids, Wiley-IEEE Press, 2014, p. 352.

[165] P. J. Grbovic, "Ultra-Capacitor Module Selection and Design," in Ultra-Capacitors in Power Conversion Systems:Analysis, Modeling and Design in Theory and Practice, Wiley-IEEE Press, 2014, p. 336-.

[166] P. J. Grbovic and M. Arpilliere, "IGBT cross conduction phenomenon #x2014; Origin and simple protection gate driving technique," in *2009 13th European Conference on Power Electronics and Applications*, 2009, pp. 1–10.

[167] P. T. Krein, R. S. Balog and M. Mirjafari, "Minimum Energy and Capacitance Requirements for Single-Phase Inverters and Rectifiers Using a Ripple Port" *IEEE Trans. Power Electronics* Vol. 27, No. 11, pp. 4690-4698, November 2012.

[168] A. Lidozzi, M. Di Benedetto, S. Bifaretti, L. Solero and F. Crescimbini, "Resonant Controllers With Three Degrees of Freedom for AC Power Electronic Converters," in IEEE Transactions on Industry Applications, vol. 51, no. 6, pp. 4595-4604, Nov.-Dec. 2015.

[169] S. Bifaretti, A. Lidozzi, L. Solero and F. Crescimbini, "Anti-Islanding Detector Based on a Robust PLL," in IEEE Transactions on Industry Applications, vol. 51, no. 1, pp. 398-405, Jan.-Feb. 2015.

[170] Vishay AN608A, "Power MOSFET Basics: Understanding Gate Charge and Using it to Assess Switching Performance" https://www.vishay.com/docs/73217/an608a.pdf.

APPENDIX

12 ANALYTICAL LOSSES CALCULATION

The conduction and switching losses have been calculated using a first-order approximation from the data-sheet characteristic curve provided by manufacturer. In the following, the conduction and switching losses values are related to the single power devices

12.1 MOSFET - IPT210N25NFD

12.1.1 Conduction Losses

MOSFET conduction losses can be calculated using an approximation with the drain source on-state resistance as in (213), where V_{DS} and I_D are drain-source voltage and the drain current, respectively.

$$V_{DS}(I_D) = R_{DS(on)}(I_D) \cdot I_D \tag{213}$$

The $R_{DS(on)}$ can be read from the data-sheet as in Fig. 183.

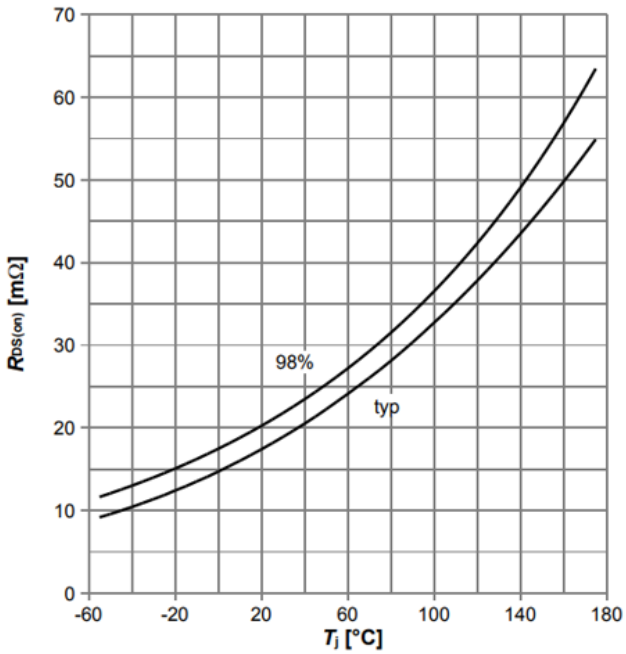


Fig. 183. $R_{DS(on)}$ versus T_j from data-sheet with I_D=69 A, V_{GS}=10 V.

The on-state resistance at T_j=100° is given in (214).

$$R_{DS(on)}(@100°C) \cong 0.035\ \Omega \tag{214}$$

Applying the equation (97), the conduction losses of the power devices S_{RaA} (or S_{RaB}, S_{IuA}, S_{IuB}) and S_{Ra12} (or S_{Ra32}, S_{Iu12}, S_{Iu32}) as listed in Table 45 and Table 46, respectively.

Table 45. Conduction losses S_{RaA} (or S_{RaB}, S_{IuA}, S_{IuB}) versus output power.				
P_{out} [kW]	$I_{OUT\text{-}leg}$ [A]	I_{AVG} [A]	I_{RMS} [A]	Conduction losses [W]
20	20,50	3,33	7,91	2,19
15	15,37	2,50	5,93	1,23
10	10,25	1,66	3,95	0,55
5	5,12	0,83	1,98	0,14
3	3,07	0,50	1,19	0,05

Table 46. Conduction losses S_{Ra12} (or S_{Ra32}, S_{Iu12}, S_{Iu32}) versus output power.				
P_{out} [kW]	$I_{OUT\text{-}leg}$ [A]	I_{AVG} [A]	I_{RMS} [A]	Conduction losses [W]
20	20,50	2,86	6,38	1,42
15	15,37	2,15	4,78	0,80
10	10,25	1,43	3,19	0,36
5	5,12	0,72	1,59	0,09
3	3,07	0,43	0,96	0,03

12.1.2 Switching Losses

The switching losses of the MOSFETs have been estimated starting from the turn-on t_{on} and turn-off t_{off} switching time [170]. The turn-on t_{on} and turn-off t_{off} switching time are given in (215), where t_{ir} is the rise-time of the current, t_{vf} is the fall-time of the voltage, t_{vr} is the rise-time of the voltage and t_{if} is the fall-time of the current.

$$t_{on} = \frac{t_{ir} + t_{vf}}{2}, \quad t_{off} = \frac{t_{vr} + t_{if}}{2} \tag{215}$$

According to the application note [170], the t_{on} and t_{off} are equal to 6,01 *ns* and 8,64 *ns*, respectively. Using the equations (100) and (102), the switching losses of the power devices S_{RaA} (or S_{RaB}, S_{IuA}, S_{IuB}) and S_{Ra12} (or S_{Ra32}, S_{Iu12}, S_{Iu32}) are listed in Table 47.

Table 47. Switching losses S_{RaA} (or S_{RaB}, S_{Iu12}, S_{Iu32}) and S_{Ra12} (or S_{Ra32}, S_{IuA}, S_{IuB}) versus output power.			
P_{out} [kW]	$I_{OUT\text{-}leg}$ [A]	Switching losses S_{RaA} (or S_{RaB}, S_{Iu12}, S_{Iu32}) [W]	Switching losses S_{Ra12} (or S_{Ra32}, S_{IuA}, S_{IuB}) [W]
20	20,50	0	0,34
15	15,37	0	0,25
10	10,25	0	0,17
5	5,12	0	0,08
3	3,07	0	0,05

12.1.3 Body Diode Losses

The on-state voltage V_{d0} and the resistance r_d parameters have been read in the MOSFET datasheet as shown in Fig. 184. The V_{d0} and r_d value are given in (216).

$$V_{d0}(@100°C) = 0.5\ \text{V},\quad r_d(@100°C) = \frac{0.62 - 0.5}{10 - 1} = 0.013\ \Omega \tag{216}$$

In this case, the dead time has not been considered; consequently, the conduction losses related to the body diode are neglected.

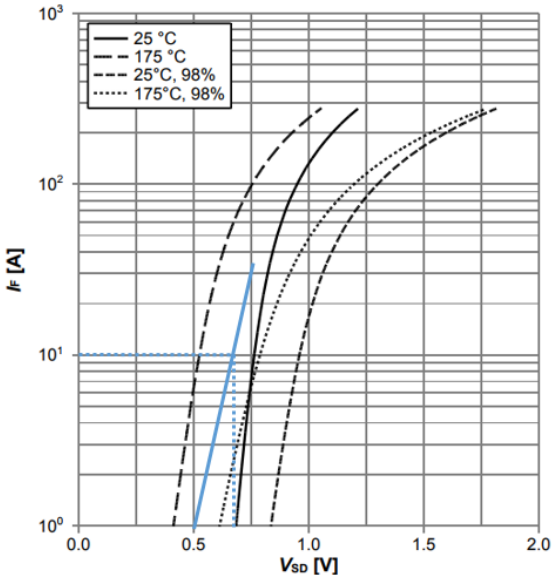


Fig. 184. Diode output characteristic.

Reverse recovery charge Q_{rr} and reverse recovery energy E_{rr} at V_{sw}=¼V_{BUS}=175 V have been read in the MOSFET datasheet and reported in (217) and (218), respectively.

$$Q_{rr}(@175V) = \left(\frac{175}{125}\right) Q_{rr}(@125V) = \left(\frac{175}{125}\right) \cdot 0.406 \cdot 10^{-6} = 0.568 \mu C \tag{217}$$

$$E_{rr}(V_{sw}) = \left(\frac{V_{BUS}}{4}\right) Q_{rr}(V_{sw}) = 99.4\mu J \quad (218)$$

Using the equation (103), the switching losses related to the D_{RaA} (or D_{RaB}, D_{IuA}, D_{IuB}) and D_{Ra12} (or D_{Ra32}, D_{Iu12}, D_{Iu32}) devices have been reported in Table 48.

Table 48. Switching losses D_{RaA} (or D_{RaB}, D_{IuA}, D_{IuB}) and D_{Ra12} (or D_{Ra32}, D_{Iu12}, D_{Iu32}) versus output power.			
P_{out} [kW]	$I_{OUT\text{-}leg}$ [A]	Switching losses D_{RaA} (or D_{RaB}, D_{Iu12}, D_{Iu32}) [W]	Switching losses D_{Ra12} (or D_{Ra32}, D_{IuA}, D_{IuB}) [W]
20	20,50	0,19	0
15	15,37	0,14	0
10	10,25	0,10	0
5	5,12	0,05	0
3	3,07	0,03	0

12.2 MOSFET - IPL60R104C7

12.2.1 Conduction Losses

The $R_{DS(on)}$ as a function of temperature can be read from the data-sheet as in Fig. 183.

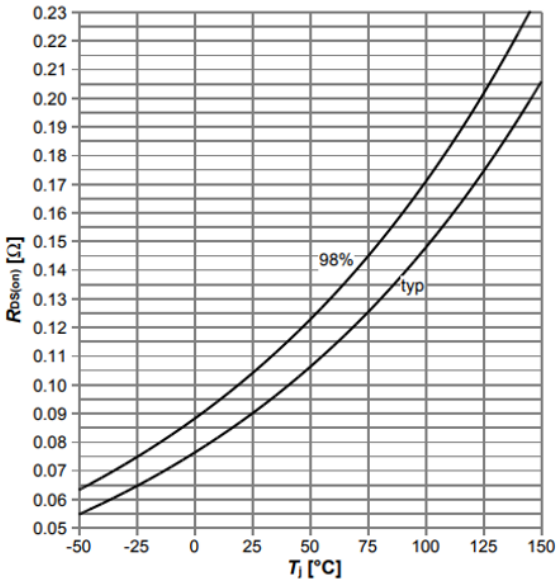


Fig. 185. $R_{DS(on)}$ versus T_j from data-sheet with I_D=9.7 A, V_{GS}=10 V.

The on-state resistance value at T_j=100° is given in (219).

$$R_{DS(on)}(@100°C) \cong 0.17\ \Omega \quad (219)$$

Applying the equation (97), the conduction losses of the power devices S_{Ra21} (or

S_{Ra22}) are listed in Table 49.

Table 49. Conduction losses S_{Ra21} (or S_{Ra22}) versus output power.				
P_{out} [kW]	$I_{OUT\text{-}leg}$ [A]	I_{AVG} [A]	I_{RMS} [A]	Conduction losses [W]
20	20,50	0,33	1,36	0,31
15	15,37	0,25	1,02	0,18
10	10,25	0,17	0,68	0,08
5	5,12	0,08	0,34	0,02
3	3,07	0,05	0,20	0,01

12.2.2 Switching Losses

According to the application note [170], the turn-on t_{on} and turn-off t_{off} switching time are equal to 10 *ns* and 10.6 *ns*, respectively. Using the equations (100) and (102), the switching losses of the power devices S_{Ra21} (or S_{Ra22}) are reported in Table 50.

Table 50. Switching losses S_{Ra21} (or S_{Ra22}) versus output power.		
P_{out} [kW]	$I_{OUT\text{-}leg}$ [A]	Switching losses [W]
20	20,50	0,09
15	15,37	0,07
10	10,25	0,04
5	5,12	0,02
3	3,07	0,01

12.2.3 Body Diode Losses

The on-state voltage V_{d0} and the resistance r_d parameters have been read in the MOSFET data-sheet as shown in Fig. 184. The V_{d0} and r_d value are given in (220).

$$V_{d0}(@100°C) = 0.55\ \text{V}\,,\quad r_d(@100°C) = \frac{0.83 - 0.58}{10 - 1} = 0.028\ \Omega \tag{220}$$

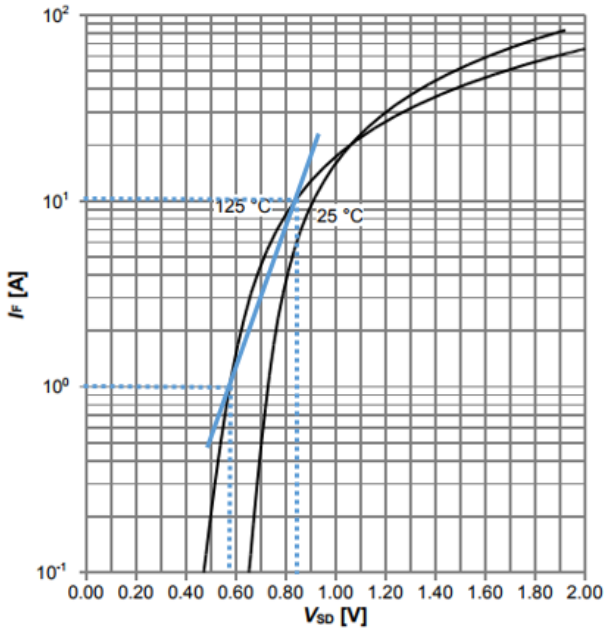


Fig. 186. Diode output characteristic from data-sheet.

Using the equation (97), the conduction losses related to the D_{Ra21} (or D_{Ra22}) have been reported in Table 51.

Table 51. Conduction losses D_{Ra21} (or D_{Ra22}) versus output power.				
P_{out} [kW]	$I_{OUT\text{-}leg}$ [A]	I_{AVG} [A]	I_{RMS} [A]	Conduction losses [W]
20	20,50	0,33	1,36	0,23
15	15,37	0,25	1,02	0,17
10	10,25	0,17	0,68	0,10
5	5,12	0,08	0,34	0,05
3	3,07	0,05	0,20	0,03

Since the D_{Ra21} (or D_{Ra22}) is always on, its switching losses are zero.

12.3 Diode - STPSC40065C

With reference to Fig. 194, the on-state voltage V_{d0} and the resistance r_d values are given in (221).

$$V_{d0}(@100°C) = 0.85\ \text{V}, \quad r_d(@100°C) = \frac{1.25 - 0.98}{2(15-5)} = 0.0135\ \Omega \tag{221}$$

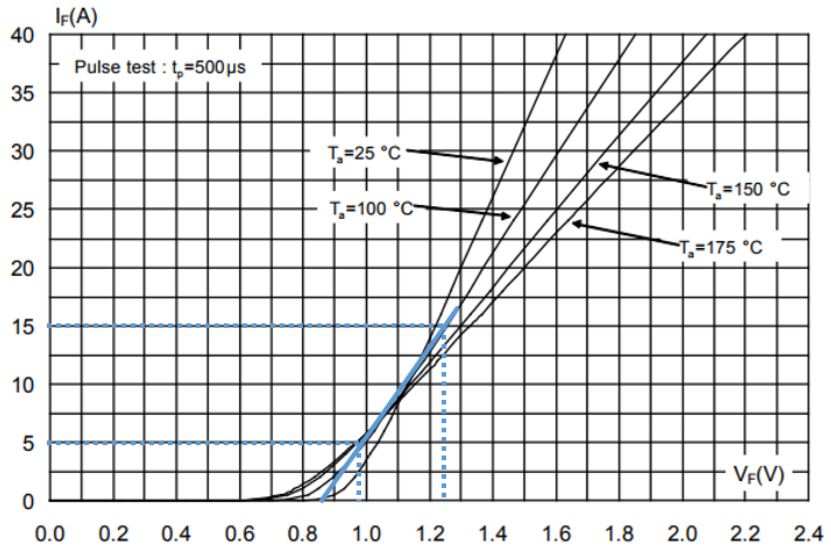


Fig. 187. Diode output characteristic from data-sheet per device.

Applying the equation (97), the conduction losses related to the D_{Ra11} (or D_{Ra31}) have been reported in Table 51.

Table 52. Conduction losses D_{Ra11} (or D_{Ra31}) versus output power.

P_{out} [kW]	$I_{OUT\text{-}leg}$ [A]	I_{AVG} [A]	I_{RMS} [A]	Conduction losses [W]
20	20,50	6,19	10,16	6,66
15	15,37	4,65	7,62	4,73
10	10,25	3,10	5,08	2,98
5	5,12	1,55	2,54	1,40
3	3,07	0,93	1,52	0,82

Due to the silicon carbide technology, the recovery losses are negligible.

12.4 IGBT- IKW75N65EL5

12.4.1 Conduction Losses

The linear approximation of the output characteristics I_C-V_{CE} from the device datasheet is depicted in Fig. 188. With reference to Fig. 188, the V_{CE0} and R_{CE0} values can easily be calculated by the equation (222).

$$V_{CE0}(@100°C) = 0.6\ \text{V},\quad r_{CE}(@100°C) = \frac{0.85-0.72}{25-12.5} = 0.01\ \Omega \tag{222}$$

Considering the AVG and RMS current reported in Table 18 and equation (97), the conduction losses versus output power related to the single-leg device S_{Ia11}

(or S_{Ia31}) are shown in Table 53.

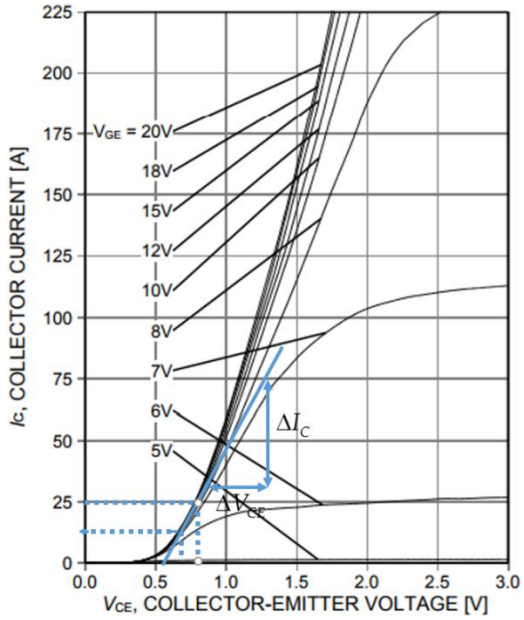


Fig. 188. IGBT output characteristic, T_{vj}=175°C.

Table 53. Conduction losses S_{Ia11} (or S_{Ia31}) versus output power.				
P_{out} [kW]	$I_{OUT\text{-}leg}$ [A]	I_{AVG} [A]	I_{RMS} [A]	Conduction losses [W]
20	20,50	6,19	10,16	4,75
15	15,37	4,65	7,62	3,37
10	10,25	3,10	5,08	2,12
5	5,12	1,55	2,54	0,99
3	3,07	0,93	1,52	0,58

12.4.2 Switching Losses

The switching losses have been obtained starting from the turn-on E_{on} and turn-off E_{off} energy curve characteristics shown in Fig. 189. The turn-on E_{on} and turn-off E_{off} energy are functions of the current flowing through the IGBT, junction temperature and blocking voltage. To this purpose, the junction temperature coefficient of turn-on and turn-off energy have been obtained from Fig. 189a, (223).

$$k_{on}(T_j)=\frac{E_{on}(@100°C)}{E_{on}(@150°C)}=\frac{1.9}{2.1}=0.9\,,\quad k_{off}(T_j)=\frac{E_{off}(@100°C)}{E_{off}(@150°C)}=\frac{4.1}{5}=0.82 \qquad (223)$$

From the Fig. 189b, the blocking voltage coefficient of turn-on and turn-off energy have been obtained in (224).

$$k_{on}(V_{CE}) = \frac{E_{on}(@175V)}{E_{on}(@400V)} = \frac{0.5}{2.1} = 0.24\,,\quad k_{off}(V_{CE}) = \frac{E_{off}(@175V)}{E_{off}(@400V)} = \frac{2.1}{5.1} = 0.41 \tag{224}$$

Finally, from the Fig. 189c, the turn-on and turn-off energy can be written in

$$\begin{aligned} E_{on}\left(T_j, V_{CE}, I_C\right) &= k_{on}(T_j)\cdot k_{on}(V_{CE})\cdot\left(\frac{2.1-0.62}{75-25}\right)10^{-3} = 0.0063mJ\,, \\ E_{off}\left(T_j, V_{CE}, I_C\right) &= k_{off}(T_j)\cdot k_{off}(V_{CE})\cdot\left(\frac{5.1-2.5}{75-25}\right)10^{-3} = 0.018mJ \end{aligned} \tag{225}$$

Having the turn-on and turn-off energy and using the equation (100) and (101), the switching losses linked to the single-leg device S_{Ia11} (or S_{Ia31}) are listed in Table 54.

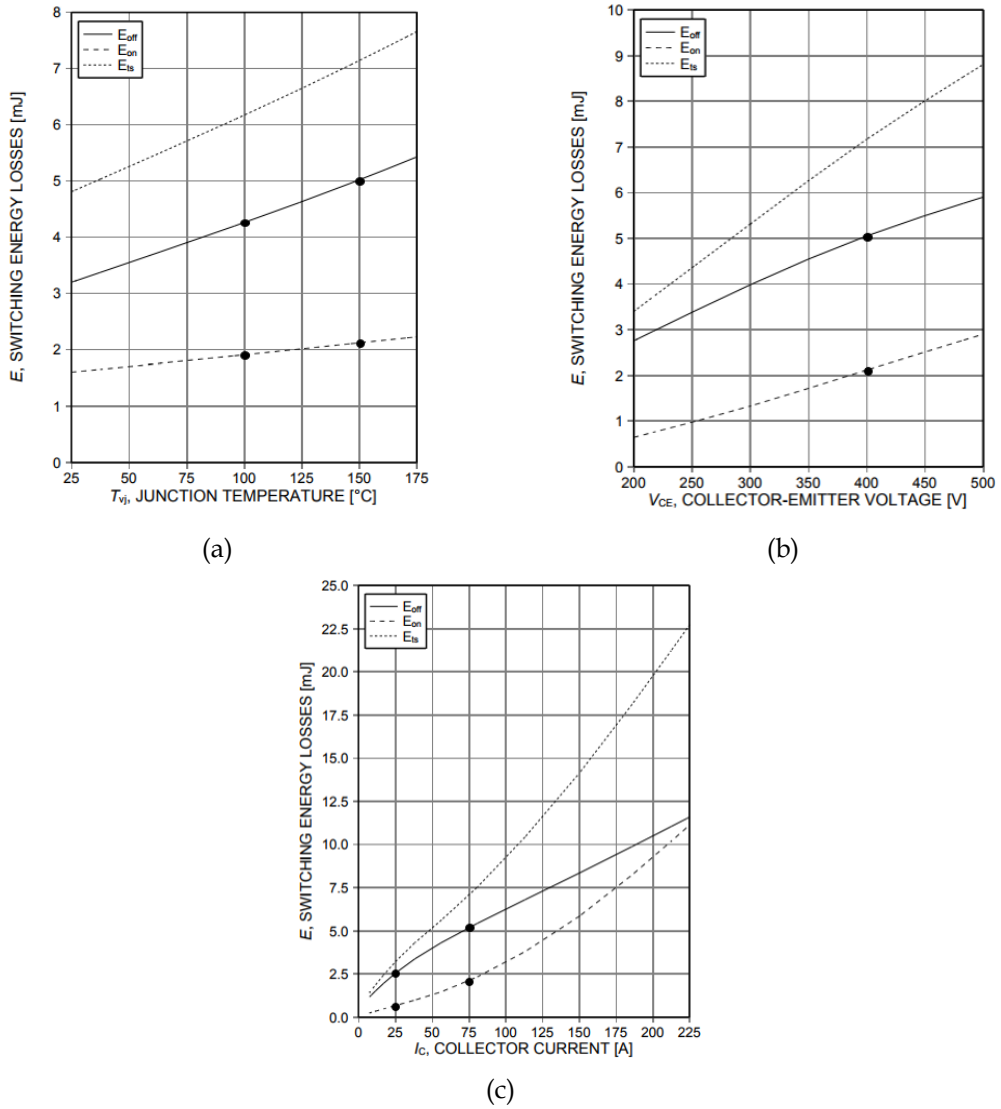


Fig. 189. (a) Switching energy vs T_{vj}; (b) Switching energy vs V_{CE}; (c) Switching energy vs I_C.

Table 54. Switching losses S_{Ia11} (or S_{Ia31}) versus output power.		
P_{out} [kW]	$I_{OUT\text{-}leg}$ [A]	Switching losses [W]
20	20,50	0,59
15	15,37	0,44
10	10,25	0,29
5	5,12	0,15
3	3,07	0,09

12.4.3 Freewheeling Diode Losses

The conduction losses of the anti-parallel diode can be estimated using the output characteristic approximation depicted in Fig. 190.

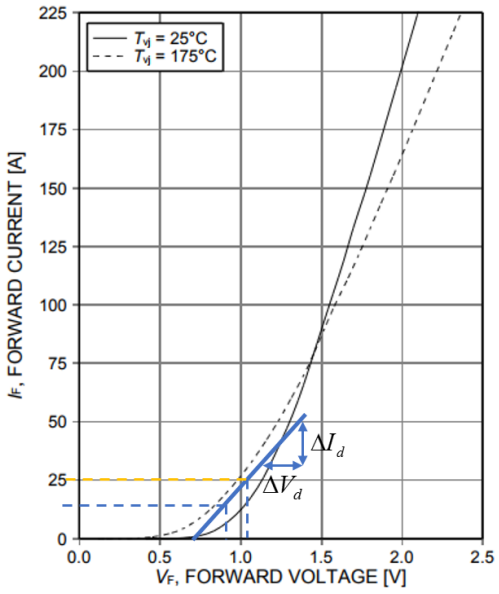


Fig. 190. Freewheeling Diode output characteristic.

On-state voltage V_{d0} and resistance r_d values are given in (226).

$$V_{d0}(@100°C) = 0.75\ \text{V}\,,\quad r_d(@100°C) = \frac{1.075 - 0.91}{25 - 12.5} = 0.013\ \Omega \tag{226}$$

The reverse recovery energy E_{rr} can be achieved starting from the reverse recovery charge Q_{rr}. The reverse recovery charge as a function of the junction temperature is given from datasheet of the IGBT manufacturer. In order to obtain the reverse recovery charge at T_j=100°C, it can be used a linear approximation as in (227). The reverse recovery charge can be calculated as in (228).

$$\frac{Q_{rr}(T_{j2}) - Q_{rr}(T_j)}{T_{j2} - T_j} = \frac{Q_{rr}(T_{j2}) - Q_{rr}(T_{j1})}{T_{j2} - T_{j1}} \tag{227}$$

$$Q_{rr}(T_j, V_{sw}) = \left(\frac{175}{400}\right) Q_{rr}(@100°C) = \left(\frac{175}{400}\right) \cdot 2.006 \cdot 10^{-6} = 0.87\,\mu C \quad (228)$$

Thus, recovery energy E_{rr} is given in (229).

$$E_{rr}\left(T_j, V_{sw}\right) = \left(\frac{V_{BUS}}{4}\right) Q_{rr}(T_j, V_{sw}) = 175.25\,\mu J \quad (229)$$

Using the equation (97) and (103), the conduction and switching losses can be obtained. If the power factor is close to 1 the losses related to the freewheeling diode D_{Ia31} are equal to zero.

12.5 IGBT - IKW20N60T

The conduction and switching losses related to the IGBT IKW20N60T can be calculated in the similar manner of the IGBT IKW75N65EL5.

12.5.1 Conduction Losses

The output characteristics I_C-V_{CE} from the device datasheet is depicted in Fig. 191.

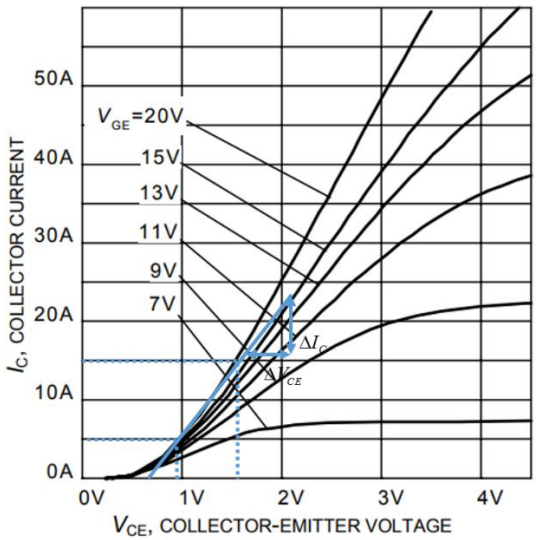


Fig. 191. IGBT output characteristic, T_{vj}=175°C.

The V_{CE0} and R_{CE0} values are given in (230).

$$V_{CE0}(@100°C) = 0.8\ \text{V}, \quad r_{CE}(@100°C) = \frac{1.375 - 0.99}{15 - 5} = 0.038\ \Omega \quad (230)$$

Considering the equation (97), the conduction losses versus output power related to the single-leg device S_{Ia21} (or S_{Ia22}) are shown in Table 55.

Table 55. Conduction losses S_{Ia21} (or S_{Ia22}) versus output power.				
P_{out} [kW]	$I_{OUT\text{-}leg}$ [A]	I_{AVG} [A]	I_{RMS} [A]	Conduction losses [W]
20	20,50	0,33	1,36	0,33
15	15,37	0,25	1,02	0,24
10	10,25	0,17	0,68	0,15
5	5,12	0,08	0,34	0,07
3	3,07	0,05	0,20	0,04

12.5.2 Switching Losses

With reference to the Fig. 193a and Fig. 193b, the energy coefficients are given in (231) and (232), respectively.

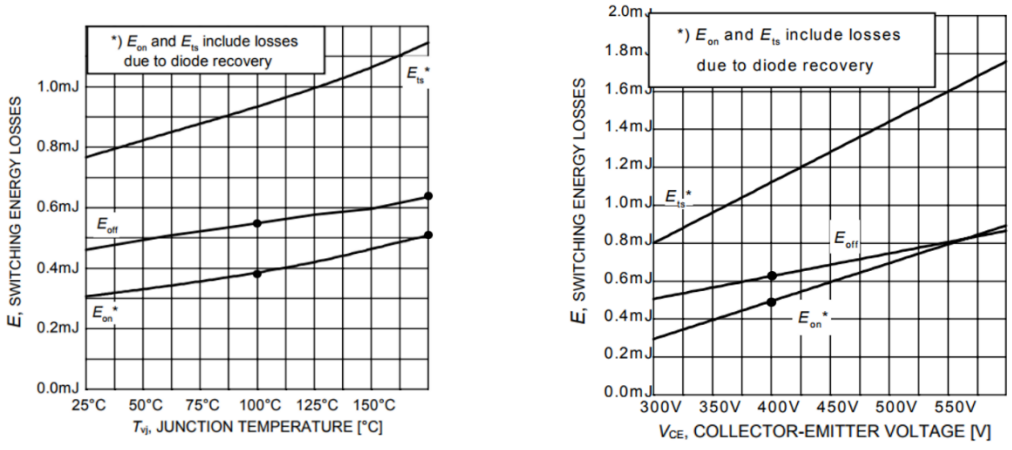
$$k_{on}(T_j)=\frac{E_{on}(@100°C)}{E_{on}(@175°C)}=\frac{0.38}{0.51}=0.75,\quad k_{off}(T_j)=\frac{E_{off}(@100°C)}{E_{off}(@175°C)}=\frac{0.55}{0.64}=0.86 \tag{231}$$

$$k_{on}(V_{CE})=\frac{E_{on}(@175V)}{E_{on}(@400V)}=\frac{0.21}{0.5}=0.42,\quad k_{off}(V_{CE})=\frac{E_{off}(@175V)}{E_{off}(@400V)}=\frac{0.41}{0.63}=0.65 \tag{232}$$

From the Fig. 193a, the turn-on and turn-off energy can be written in

$$\begin{aligned} E_{on}\left(T_j,V_{CE},I_C\right)&=k_{on}(T_j)\cdot k_{on}(V_{CE})\cdot\left(\frac{0.67-0.15}{25-5}\right)10^{-3}=0.008mJ,\\ E_{off}\left(T_j,V_{CE},I_C\right)&=k_{off}(T_j)\cdot k_{off}(V_{CE})\cdot\left(\frac{0.77-0.25}{25-5}\right)10^{-3}=0.015mJ \end{aligned} \tag{233}$$

During the positive half-wave of the modulating signal, S_{Ia21} is always on. Consequently, the switching losses related to the S_{Ia21} device is equal to zero.



(a) (b)

Fig. 192. (a) Switching energy vs T_{vj}; (b) Switching energy vs V_{CE}.

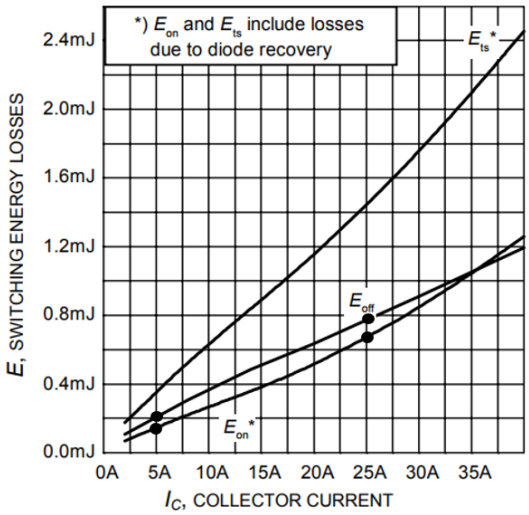


Fig. 193. Switching energy vs I_C.

12.5.3 Freewheeling Diode losses

With reference to Fig. 194, the on-state voltage V_{d0} and the resistance r_d values are given in (234).

$$V_{d0}(@100°C) = 0.85\ \text{V},\quad r_d(@100°C) = \frac{1.64 - 1.2}{15 - 5} = 0.044\ \Omega \tag{234}$$

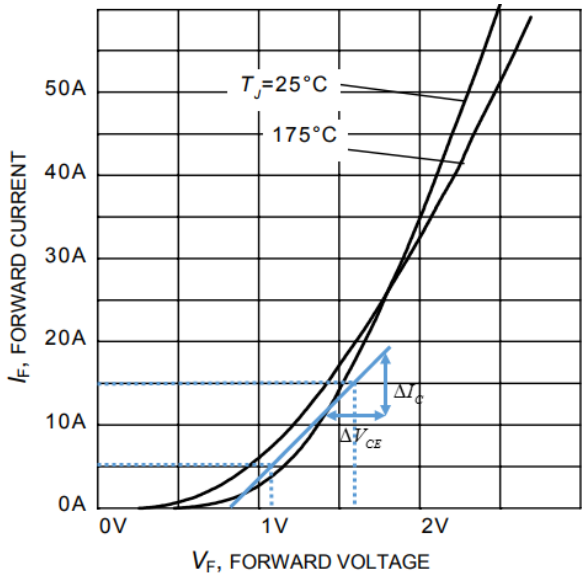


Fig. 194. Freewheeling Diode output characteristic.

Reverse recovery charge Q_{rr} and reverse recovery energy E_{rr} at T_j=100°C can be calculated as in (235) and (236), respectively.

$$Q_{rr}(T_j, V_{sw}) = \left(\frac{175}{400}\right) Q_{rr}(@100°C) = \left(\frac{175}{400}\right) \cdot 0.885 \cdot 10^{-6} = 0.387\,\mu C \tag{235}$$

$$E_{rr}(T_j, V_{sw}) = \left(\frac{V_{BUS}}{4}\right) Q_{rr}(T_j, V_{sw}) = 67.73\,\mu J \tag{236}$$

Using the equation (97) and (103), the conduction and switching losses have been reported in Table 56.

Table 56. Conduction losses D_{Ia21} (or D_{Ia22}) versus output power.

P_{out} [kW]	$I_{OUT\text{-}leg}$ [A]	I_{AVG} [A]	I_{RMS} [A]	Conduction losses [W]	Switching losses [W]
20	20,50	0,33	1,36	0,25	0,08
15	15,37	0,25	1,02	0,17	0,06
10	10,25	0,17	0,68	0,10	0,04
5	5,12	0,08	0,34	0,05	0,02
3	3,07	0,05	0,20	0,03	0,01